DATASHEET

FOR

512M BIT Parallel NOR FLASH

BY29G512FS

Distinctive Characteristics

- Single 3V read/program/erase (2.7-3.6 V)
- Enhanced VersatileI/O™ control
  - All input levels (address, control, and DQ input levels) and outputs are determined by voltage on V_{IO} input. V_{IO} range is 1.65 to V_{CC}
- 8-word/16-byte page read buffer
- 32-word/64-byte write buffer reduces overall programming time for multiple-word updates
- Secured Silicon Sector region
  - 128-word/256-byte sector for permanent, secure identification through an 8-word/16-byte random Electronic Serial Number
  - Can be programmed and locked at the factory or by the customer
- Uniform 64 Kword/128 Kbyte Sector Architecture
  - One thousand twenty-four sectors
- 100,000 erase cycles per sector typical
- 20-year data retention typical
- Offered Packages
  - 56-pin TSOP
  - 64-ball Fortified BGA
- Write operation status bits indicate program and erase operation completion
- Unlock Bypass Program instruction to reduce programming time
- Support for CFI (Common Flash Interface)
- Persistent and Password methods of Advanced Sector Protection
- WP#/ACC input
- Hardware reset input (RESET#) resets device
- Ready/Busy# output (RY/BY#) detects program or erase cycle completion

Performance Characteristics

Maximum Read Access Times (ns)					
Density	**Voltage Range (1)**	**Random Access Time (t_{ACC})**	**Page Access Time (t_{PACC})**	**CE# Access Time (t_{CE})**	**OE# Access Time (t_{OE})**
512Mb	Regulated V_{CC}	110	25	110	25
	Full V_{CC}	120		120	
	VersatileIO V_{IO}	130		130	

Note

1. *Access times are dependent on V_{CC} and V_{IO} operating ranges. See Order Information for further details.*
   Regulated V_{CC}: V_{CC} = 3.0–3.6 V.
   Full V_{CC}: V_{CC} = V_{IO} = 2.7–3.6 V.
   VersatileIO V_{IO}: V_{IO} = 1.65–V_{CC}, V_{CC} = 2.7–3.6 V.
2. *Contact a sales representative for availability*

Current Consumption (typical values)	
Random Access Read (*f* = 5 MHz)	30 mA
8-Word Page Read (*f* = 10 MHz)	1 mA
Program/Erase	50 mA
Standby	100 µA

Program & Erase Times (typical values)	
Single Word/Byte Programming	60 µs
Effective Write Buffer Programming (V_{CC}) Per Word	15 µs
Effective Write Buffer Programming (V_{HH}) Per Word	13.5 µs
Sector Erase Time (64 Kword Sector)	0.5 s

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1. DESCRIPTION

The **BY29G512FS** is flash product fabricated on ETOX 50 nm process technology. These devices offer a fast page access time of 25 ns with a corresponding random access time as fast as 110 ns. They feature a Write Buffer that allows a maximum of 32 words/64 bytes to be programmed in one operation, resulting in faster effective programming time than standard programming algorithms. This makes these devices ideal for today's embedded applications that require higher density, better performance and lower power consumption.

Figure 1. Logic diagram

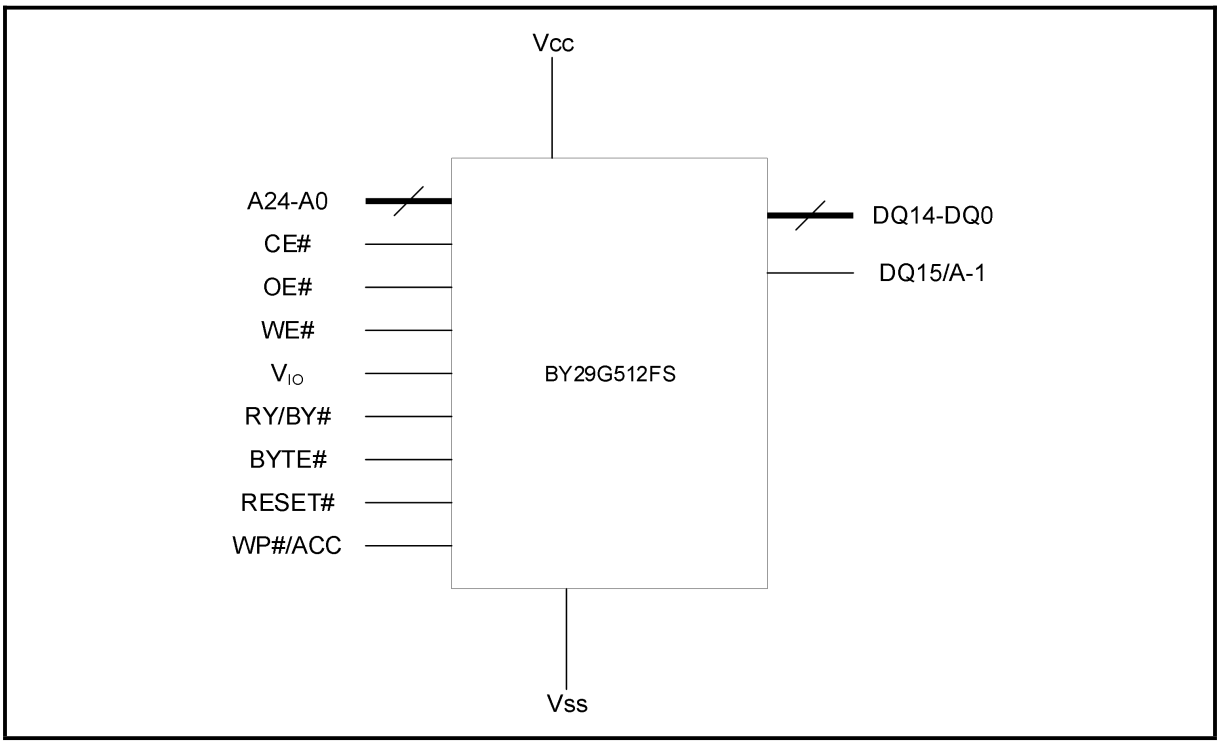


Figure 2.1. Pin Configuration for TFBGA11*13-64BALL

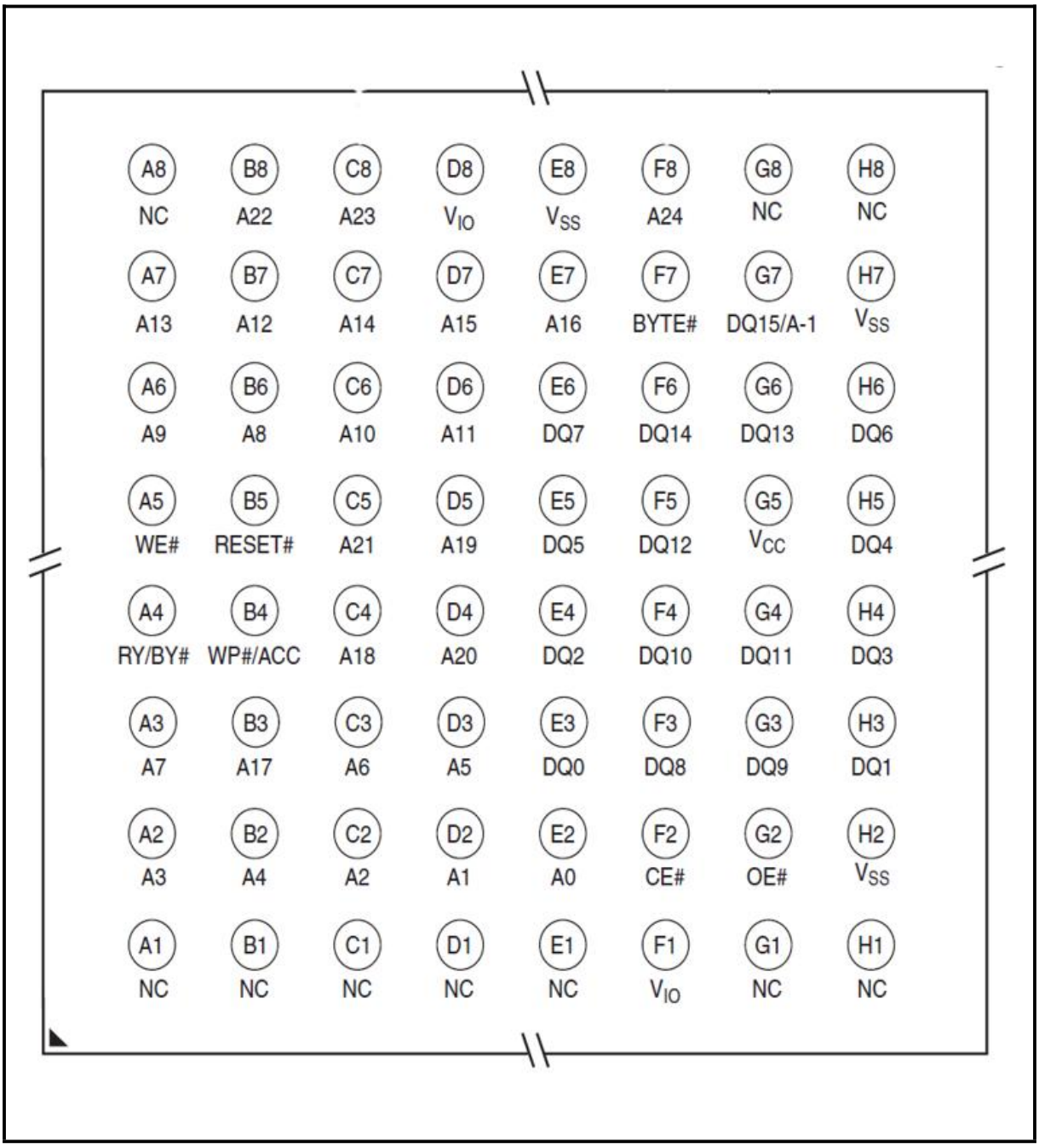
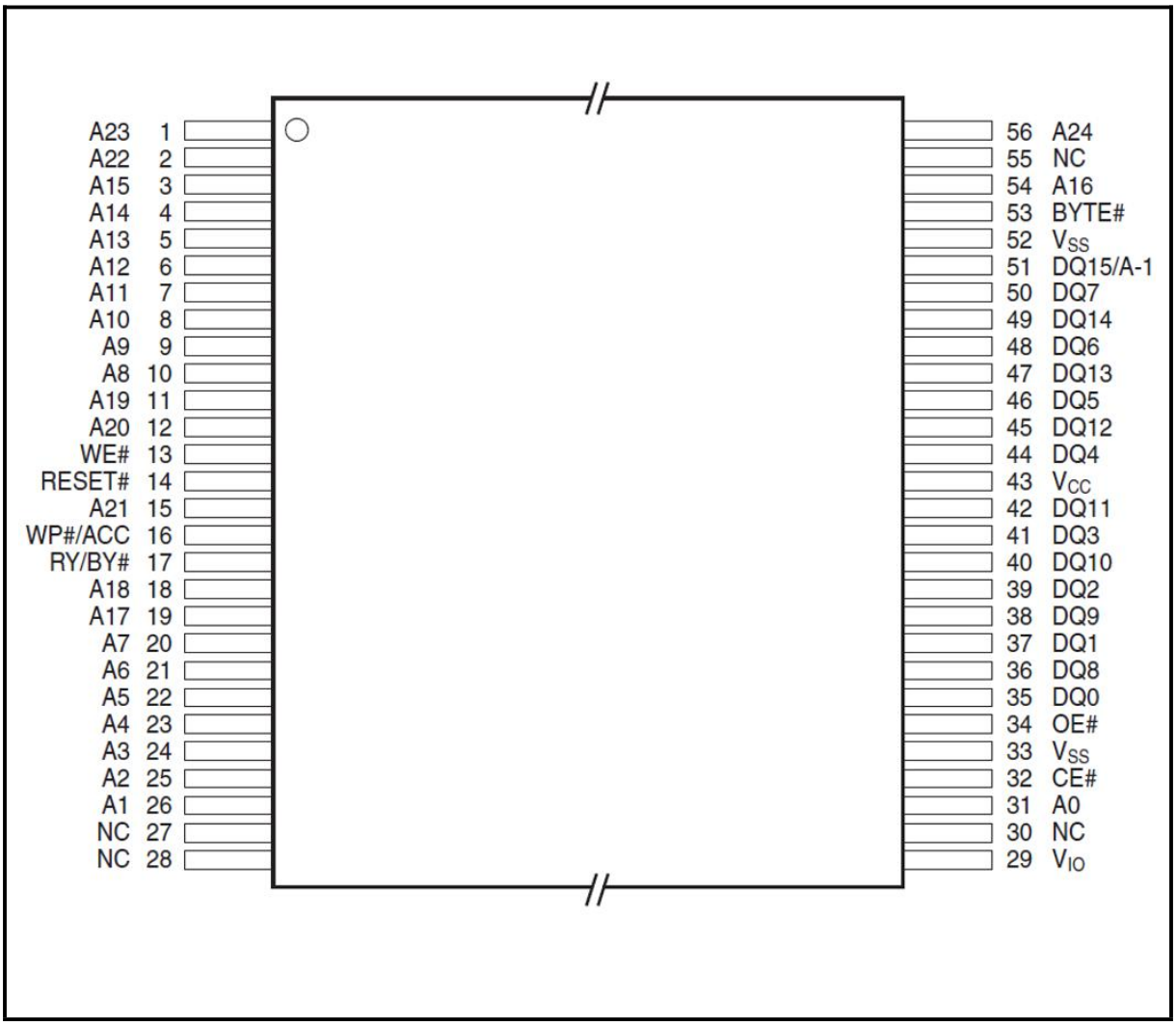


Figure 3.2. Pin Configuration for TSOP56 14*20mm



2. SIGNAL DESCRIPTION

Table 1. Signal Names

Symbol	Type	Description
A24-A0	Input	Address lines for BY29G512FS
DQ14–DQ0	I/O	Data input/output
DQ15/A-1	I/O	DQ15: Data input/output in word mode A-1: LSB address input in byte mode
CE#	Input	Chip Enable
OE#	Input	Output Enable
WE#	Input	Write Enable
V_{CC}	Supply	Device Power Supply
V_{IO}	Supply	Versatile IO Input
V_{SS}	Supply	Ground
NC	No Connect	Not connected internally
RY/BY#	Output	Ready/Busy. Indicates whether an Embedded Algorithm is in progress or complete. At V_{IL}, the device is actively erasing or programming. At High Z, the device is in ready
BYTE#	Input	Selects data bus width. At V_{IL}, the device is in byte configuration and data I/O pins DQ0-DQ7 are active and DQ15/A-1 becomes the LSB address input. At V_{IH}, the device is in word configuration and data I/O pins DQ0-DQ15 are active
RESET#	Input	Hardware Reset. Low = device resets and returns to reading array data
WP#/ACC	Input	Write Protect/Acceleration Input. At V_{IL}, disables program and erase functions in the sertor0. At V_{HH}, accelerates programming; automatically places device in unlock bypass mode. Should be at V_{IH} for all other conditions. WP# has an internal pull-up; when unconnected, WP# is at V_{IH}

3. SECTOR ADDRESSES

Table 2. Sector Addresses of BY29G512FS

Memory Density	Big Block (256Kword/512Kbyte)	Sector (64Kword/128Kbyte)	Address Range
512Mbit	Big Block 0	Sector 0	0000000h-000FFFFh
		:	:
		Sector 3	0030000h-003FFFFh
	:	:	:
	Big Block 127	Sector 508	1FC0000h-1FCFFFFh
		:	:
		Sector 511	1FF0000h-1FFFFFFh

Note:

1. *Big Block = Uniform Big Block, and the size is 256 Kword/ 512Kbyte.*
2. *Sector = Uniform Sector, and the size is 64K word/128K byte.*

4. OPERATION FEATURES

4.1 Power Conservation Modes

4.1.1 Standby Mode

When the system is not reading or writing to the device, it can place the device in the standby mode. In this mode, current consumption is greatly reduced, and the outputs are placed in the high impedance state, independent of the OE# input. The device enters the standby mode when the CE# and RESET# inputs are both held at V_{CC} ± 0.3 V. The device requires standard access time (t_{CE}) for read access, before it is ready to read data. If the device is deselected during erasure or programming, the device draws active current until the operation is completed. ICC4 in "***DC Characteristics***" represents the standby current specification.

4.1.2 Automatic Sleep Mode

The automatic sleep mode minimizes Flash device energy consumption. The device automatically enables this mode when addresses remain stable for t_{ACC} + 30 ns. The automatic sleep mode is independent of the CE#, WE#, and OE# control signals. Standard address access timings provide new data when addresses are changed. While in sleep mode, output data is latched and always available to the system. ICC6 in "***DC Characteristics***" represents the automatic sleep mode current specification.

4.1.3 Hardware RESET# Input Operation

The RESET# input provides a hardware method of resetting the device to reading array data. When RESET# is driven low for at least a period of t_{RP}, the device immediately terminates any operation in progress, tristates all outputs, and ignores all read/write instructions for the duration of the RESET# pulse. The device also resets the internal state machine to reading array data. The operation that was interrupted should be reinitiated once the device is ready to accept another instruction sequence to ensure data integrity.

When RESET# is held at V_{SS} ± 0.3 V, the device draws ICC reset current (ICC5). If RESET# is held at V_{IL} but not within V_{SS} ± 0.3 V, the standby current is greater.

RESET# may be tied to the system reset circuitry and thus, a system reset would also reset the Flash memory, enabling the system to read the boot-up firmware from the Flash memory.

4.1.4 Output Disable (OE#)

When the OE# input is at V_{IH}, output from the device is disabled. The outputs are placed in the high impedance state. (With the exception of RY/BY#.)

4.2 Word/Byte Configuration

The BYTE# pin controls whether the device data I/O pins operate in the byte or word configuration. If the BYTE# pin is set at logic '1', the device is in word configuration, DQ0-DQ15 are active and controlled by CE# and OE#.

If the BYTE# pin is set at logic '0', the device is in byte configuration, and only data I/O pins DQ0-DQ7 are active and controlled by CE# and OE#. The data I/O pins DQ8-DQ14 are tri-stated, and the DQ15 pin is used as an input for the LSB (A-1) address function.

4.3 Versatile IOTM (VIO) Control

The VersatileIO™ (V_{IO}) control allows the host system to set the voltage levels that the device generates and tolerates on all inputs and outputs (address, control, and DQ signals). V_{IO} range is 1.65 to V_{CC}. See ***Order Information*** for V_{IO} options on this device.

For example, a V_{IO} of 1.65-3.6 volts allows for I/O at the 1.8 or 3 volt levels, driving and receiving signals to and from other 1.8 or 3V devices on the same data bus.

4.4 RY/BY#

The RY/BY# is a dedicated, open-drain output pin that indicates whether an Embedded Algorithm is in progress or complete. The RY/BY# status is valid after the rising edge of the final WE# pulse in the instruction sequence. Since RY/BY# is an open-drain output, several RY/BY# pins can be tied together in parallel with a pull-up resistor to V_{CC}. This feature allows the host system to detect when data is ready to be read by simply monitoring the RY/BY# pin, which is a dedicated output.

When the RY/BY# changes from V_{IL} to High Z, that is, the Embedded Algorithm is completed, but the Embedded Algorithm cannot be judged to be successful, and it needs to be combined with the status judgment of DQ5. Unlike RY/BY#, when DQ6 stops toggle, it means the Embedded Algorithm is completed and the Embedded Algorithm is successful.

4.5 Hardware Data Protection Methods

The device offers the main type of data protection at the sector level via hardware control: When WP#/ACC is at V_{IL}, the lowest sector is locked (device specific).

There are additional methods by which intended or accidental erasure of any sectors can be prevented via hardware means. The following subsections describes these methods:

4.5.1 WP#/ACC Method

The Write Protect feature provides a hardware method of protecting one outermost sector. This function is provided by the WP#/ACC pin and overrides the previously discussed Sector Protection/Unprotection method.

If the system asserts V_{IL} on the WP#/ACC pin, the device disables program and erase functions in the highest or lowest sector independently of whether the sector was protected or unprotected using the method described in ***Figure 44***.

If the system asserts V_{IH} on the WP#/ACC pin, the device reverts to whether the boot sectors were last set to be protected or unprotected. That is, sector protection or unprotection for these sectors depends on whether they were last protected or unprotected.

The WP#/ACC pin must be held stable during a instruction sequence execution. WP# has an internal pull-up; when unconnected, WP# is set at V_{IH}.

Note

If WP#/ACC is at V_{IL} when the device is in the standby mode, the maximum input load current is increased.

4.5.2 Low VCC Write Inhibit

When V_{CC} is less than V_{LKO}, the device does not accept any write cycles. This protects data during V_{CC} power-up and power-down.

The instruction register and all internal program/erase circuits are disabled, and the device resets to reading array data. Subsequent writes are ignored until V_{CC} is greater than V_{LKO}. The system must provide the proper signals to the control inputs to prevent unintentional writes when V_{CC} is greater than V_{LKO}.

4.5.3 Write Pulse "Glitch Protection"

Noise pulses of less than 5 ns (typical) on OE#, CE# or WE# do not initiate a write cycle.

4.5.4 Power-Up Write Inhibit

If WE# = CE# = RESET# = V_{IL} and OE# = V_{IH} during power up, the device does not accept instructions on the rising edge of WE#. The internal state machine is automatically reset to the read mode on power-up.

4.6 Write Operation Status

The device provides several bits to determine the status of a program, erase operation or Password Unlock. The following subsections describe the function of DQ1, DQ2, DQ3, DQ5, DQ6, and DQ7.

Table 3. Write Operation Status

Status			DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	RY/BY#
Standard Mode	Embedded Program Algorithm		DQ7#	Toggle (Note 1)	0	N/A	N/A	N/A	0	N/A	0
	Embedded Erase Algorithm		0	Toggle	0	N/A	1	Toggle	N/A	N/A	0
	Program Algorithm Error(Note 2)		DQ7#	Toggle	1	N/A	N/A	N/A	0	N/A	1
	Erase Algorithm Error		0	Toggle	1	N/A	1	Toggle	N/A	N/A	1
Program Suspend Mode	Program-Suspend Read	Program-Suspended Sector	Invalid (not allowed)								1
		Non-Program Suspended Sector	Data								1
Erase Suspend Mode	Erase-Suspend Read	Erase-Suspended Sector	1	No toggle	0	N/A	N/A	Toggle	N/A	N/A	1
		Non-Erase Suspended Sector	Data								1
	Erase-Suspend-Program (Embedded Program)		DQ7#	Toggle	0	N/A	N/A	N/A	N/A	N/A	0
Write-to-Buffer	Busy		DQ7#	Toggle	0	N/A	N/A	N/A	0	N/A	0
	Abort		DQ7#	Toggle	0	N/A	N/A	N/A	1	N/A	0
	Error		DQ7#	Toggle	1	N/A	N/A	N/A	0	N/A	1
Password Unlock	valid/ invalid		N/A	Toggle	N/A	N/A	N/A	N/A	N/A	N/A	0

Note

1. *Toggle = 0 to 1, 1 to 0, and so on.*
2. *Error means the program or erase time has exceeded a specified internal pulse count limit.*

4.6.1 DQ7: Data# Polling

The Data# Polling bit, DQ7, indicates to the host system whether an Embedded Program or Erase algorithm is in progress or completed, or whether the device is in Erase Suspend.

During the Embedded Program algorithm, the device outputs on DQ7 the inverted value of the datum programmed to DQ7. This DQ7 status also applies to programming during Erase Suspend. When the Embedded Program algorithm is complete, the device outputs the datum programmed to DQ7. The system must provide the program address to read valid status information on DQ7. If a program address falls within a protected sector, Data# polling on DQ7 is active, then that sector returns to the read mode.

During the Embedded Erase Algorithm, Data# polling produces a "0" on DQ7. When the Embedded Erase algorithm is complete, or if the device enters the Erase Suspend mode, Data# Polling produces a "1" on DQ7. The system must provide an address within any of the sectors selected for erasure to read valid status information on DQ7.

After an erase instruction sequence is written, if all sectors selected for erasing are protected, Data# Polling on DQ7 is active for approximately 100 μs, then the device returns to the read mode. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected. However, if the system reads DQ7 at an address within a protected sector, the status may not be valid.

4.6.2 DQ6: Toggle Bit I

Toggle Bit I on DQ6 indicates whether an Embedded Program, Erase algorithm or Password Unlock is in progress. Toggle Bit I may be read at any address, and is valid after the rising edge of the final WE# pulse in the instruction sequence (prior to the program or erase operation), and during the sector erase time-out.

During an Embedded Program or Erase algorithm operation, successive read cycles to any address that is being programmed or erased causes DQ6 to toggle. When the operation is complete or has entered the Erase Suspend mode DQ6 stops toggling.

DQ6 also toggles during the erase-suspend-program mode, and stops toggling once the Embedded Program Algorithm or Password Unlock is complete.

4.6.3 DQ2: Toggle Bit II

The “Toggle Bit II” on DQ2 indicates whether a particular sector is actively erasing (that is, the Embedded Erase algorithm is in progress), or whether that sector is erase-suspended. Toggle Bit II is valid after the rising edge of the final WE# pulse in the instruction sequence. DQ2 toggles when the system reads at addresses within those sectors that have been selected for erasure. But DQ2 cannot distinguish whether the sector is actively erasing or is erase-suspended.

4.6.4 DQ5: Exceeded Timing Limits

DQ5 indicates whether the program or erase time has exceeded a specified internal pulse count limit. Under these conditions DQ5 produces a “1,” indicating that the program or erase cycle was not successfully completed. Under valid DQ5 conditions, the system must write the reset instruction to return to the read mode (or to the erase-suspend-read mode if a sector was previously in the erase-suspend-program mode).

4.6.5 DQ3: Sector Erase Timeout State Indicator

After writing a sector erase instruction sequence, the system may read DQ3 to determine whether or not erasure has begun. (The sector erase timer does not apply to the chip erase instruction.) If additional sectors are selected for erasure, the entire time-out also applies after each additional sector erase instruction. When the time-out period is complete, DQ3 switches from a “0” to a “1”. To ensure the instruction has been accepted, the system software should check the status of DQ3 prior to and following each sub-sequent sector erase instruction. If DQ3 is high on the second status check, the last instruction might not have been accepted. If the time between additional sector erase instructions from the system can be assumed to be less than t_{SEA}, then the system need not monitor DQ3. See ***Erase Operations*** for more details.

4.6.6 DQ1: Write to Buffer Abort

DQ1 indicates whether a Write to Buffer operation was aborted. Under these conditions DQ1 produces a “1”. The system must issue the “Write to Buffer Abort Reset” instruction sequence to return the device to reading array data. See Write Buffer Program for more details.

4.7 Device Operation Table

The device must be setup appropriately for each operation. ***Table 4*** describes the required state of each control pin for any particular operation.

Table 4. Device Operations

Operation	CE#	OE#	WE#	RESET#	WP#/ACC	Addresses (Note 1)	DQ0–DQ7	DQ8–DQ15	
								BYTE#= V_{IH}	BYTE#= V_{IL}
Read	L	L	H	H	X	A_{IN}	D_{OUT}	D_{OUT}	DQ8–DQ14 = High-Z, DQ15 = A-1
Write (Program/ Erase)	L	H	L	H	(Note 2)	A_{IN}	(Note 3)	(Note 3)	
Accelerated Program	L	H	L	H	V_{HH}	A_{IN}	(Note 3)	(Note 3)	
Standby	V_{CC} ± 0.3 V	X	X	V_{CC} ± 0.3 V	H	X	High-Z	High-Z	High-Z
Output Disable	L	H	H	H	X	X	High-Z	High-Z	High-Z
Reset	X	X	X	L	X	X	High-Z	High-Z	High-Z

Legend

L = Logic Low = V_{IL}, H = Logic High = V_{IH}, V_{HH} = 11.5–12.5V, X = Don't Care, A_{IN} = Address In, D_{IN} = Data In, D_{OUT} = Data Out.

Note

1. Addresses are A_{Max}: A0 in word mode; A_{Max}:A-1 in byte mode.
2. If WP# = V_{IL}, the sector0 remains protected. If WP# = V_{IH}, the outermost sector is unprotected. WP# has an internal pull-up; when unconnected, WP# is at V_{IH}. All sectors are unprotected when shipped from the factory (The Secured Silicon Sector can be factory protected depending on version ordered.)
3. DIN or DOUT as required by instruction sequence, data polling, or sector protect algorithm.

5. INSTRUCTIONS DESCRIPTION

5.1 Instruction Definitions

5.1.1 Memory Array Instruction Definitions, x16

Instruction (Notes)		Cycles	Bus Cycles (Notes 1–5)											
			First		Second		Third		Fourth		Fifth		Sixth	
			Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read (6)		1	RA	RD										
Single Word/Byte Program		4	555	AA	2AA	55	555	A0	PA	PD				
Write to Buffer (7)		6	555	AA	2AA	55	SA	25	SA	WC	WBL	PD	WBL	PD
Program Buffer to Flash (Confirm)		1	SA	29										
Write-to-Buffer-Abort Reset		3	555	AA	2AA	55	555	F0						
Chip Erase		6	555	AA	2AA	55	555	80	555	AA	2AA	55	555	10
Sector Erase		6	555	AA	2AA	55	555	80	555	AA	2AA	55	SA	30
Erase Suspend/Program Suspend		1	XXX	B0										
Erase Resume/Program Resume		1	XXX	30										
Reset		1	XXX	F0										
Unlock Bypass	Enter	3	555	AA	2AA	55	555	20						
	Read (6)	1	RA	RD										
	Single Word/Byte Program	2	XXX	A0	PA	PD								
	Write to Buffer (7)	6	SA	25	SA	WC	WBL	PD						
	Program Buffer to Flash (Confirm)	1	SA	29										
	Write-to-Buffer-Abort Reset	3	555	AA	2AA	55	555	F0						
	Sector Erase	2	XXX	80	SA	30								
	Chip Erase	2	XXX	80	XXX	10								
	Reset	2	XXX	90	XXX	00								
Secured Silicon Sector	Secured Silicon Sector Entry	3	555	AA	2AA	55	555	88						
	Read (6)	1	RA	RD										
	Single Word/Byte Program	4	555	AA	2AA	55	555	A0	PA	PD				
	Write to Buffer (7)	6	555	AA	2AA	55	SA	25	SA	WC	WBL	PD	WBL	PD
	Program Buffer to Flash (Confirm)	1	SA	29										
	Write-to-Buffer-Abort Reset	3	555	AA	2AA	55	555	F0						
	Secured Silicon Sector Exit	4	555	AA	2AA	55	555	90	XX	00				
Autoselect (8)	Manufacturer ID	4	555	AA	2AA	55	555	90	X00	01				
	Device ID	6	555	AA	2AA	55	555	90	X01	227E	X0E		X0F	
	Sector Protect Verify	4	555	AA	2AA	55	555	90	[SA]X 02					
	Secure Device Verify	4	555	AA	2AA	55	555	90	X03					
	Reset	1	XXX	F0										
CFI	CFI Query (9)	1	55	98										
	Read (6)	1	RA	RD										
	Reset	1	XXX	F0										

Legend

X = Don't care
RA = Address of the memory to be read.
RD = Data read from location RA during read operation.
PA = Address of the memory location to be programmed. Addresses latch on the falling edge of the WE# or CE# pulse, whichever happens later.
PD = Data to be programmed at location PA. Data latches on the rising edge of the WE# or CE# pulse, whichever happens first. SA = Address of the sector to be verified (in autoselect mode) or erased. Address bits Amax–A16 uniquely select any sector.
WBL = Write Buffer Location. The address must be within the same write buffer page as PA.
WC = Word Count is the number of write buffer locations to load minus 1.

Note

1. See ***Table 4*** for description of bus operations.
2. All values are in hexadecimal.
3. All bus cycles are write cycles unless otherwise noted.
4. Data bits DQ15-DQ8 are don't cares for unlock and instruction cycles.
5. Address bits A_{MAX}:A12 are don't cares for unlock and instruction cycles, unless SA or PA required. (A_{MAX} is the Highest Address pin.).
6. No unlock or instruction cycles required when reading array data.
7. Depending on the number of words written, the total number of cycles may be from 6 to 37.
8. The fourth, fifth, and sixth cycles of the autoselect instruction sequence are read cycles.
9. Instruction is valid when device is ready to read array data or when device is in autoselect mode.

5.1.2 Sector Protection Instruction Definitions, x16

	Instruction (Notes)	Cycles	Bus Cycles (Notes 1–5)											
			First/ Seventh		Second		Third		Fourth		Fifth		Sixth	
			Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Lock Register	Instruction Set Entry	3	555	AA	2AA	55	555	40						
	Program	2	XXX	A0	XXX	DATA								
	Read	1	00	RD										
	Instruction Set Exit	2	XXX	90	XXX	00								
Password Protection	Instruction Set Entry	3	555	AA	2AA	55	555	60						
	Password Program (6)	2	XXX	A0	PWAx	PWDx								
	Password Read (7)	4	00	PWD 0	01	PWD 1	02	PWD 2	03	PWD 3				
	Password Unlock (7)	7	00	25	00	03	00	PWD 0	01	PWD 1	02	PWD 2	03	PWD 3
			00	29										
	Instruction Set Exit	2	XXX	90	XXX	00								
Global Non-Volatile	PPB Instruction Set Entry	3	555	AA	2AA	55	555	C0						
	PPB Program	2	XXX	A0	SA	00								
	All PPB Erase	2	XXX	80	00	30								
	PPB Status Read	1	SA	RD (0)										
	PPB Instruction Set Exit	2	XXX	90	XXX	00								
Global Volatile Freeze	PPB Lock Instruction Set Entry	3	555	AA	2AA	55	555	50						
	PPB Lock Set	2	XXX	A0	XXX	00								
	PPB Lock Status Read	1	XXX	RD (0)										
	PPB Lock Instruction Set Exit	2	XXX	90	XXX	00								
Volatile	DYB Instruction Set Entry	3	555	AA	2AA	55	555	E0						
	DYB Set	2	XXX	A0	SA	00								
	DYB Clear	2	XXX	A0	SA	01								
	DYB Status Read	1	SA	RD (0)										
	DYB Instruction Set Exit	2	XXX	90	XXX	00								

Legend

X = Don't care RD(0) = Read data.
SA = Sector Address. Address bits Amax–A16 uniquely select any sector. PWD = Password
PWDx = Password word0, word1, word2, and word3.
Data = Lock Register Contents: PD(0) = Secured Silicon Sector Protection Bit, PD(1) = Persistent Protection Mode Lock Bit, PD(2) = Password Protection Mode Lock Bit.

Note

1. See ***Table 4*** for description of bus operations.
2. All values are in hexadecimal.
3. All bus cycles are write cycles unless otherwise noted.
4. Data bits DQ15-DQ8 are don't cares for unlock and instruction cycles.

5. Address bits A_{MAX}: A12 are don't cares for unlock and instruction cycles, unless SA or PA required. (A_{MAX} is the Highest Address pin.)
6. For PWDx, only one portion of the password can be programmed per each "A0" instruction.
7. Note that the password portion can be entered or read in any order as long as the entire 64-bit password is entered or read.

5.1.3 Memory Array Instruction Definitions, x8

Instruction (Notes)		Cycles	Bus Cycles (Notes 1–5)											
			First		Second		Third		Fourth		Fifth		Sixth	
			Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read (6)		1	RA	RD										
Single byte program		4	AAA	AA	555	55	AAA	A0	PA	PD				
Write to Buffer (7)		6	AAA	AA	555	55	SA	25	SA	BC	WBL	PD	WB L	PD
Program Buffer to Flash (confirm)		1	SA	29										
Write-to-Buffer-Abort Reset		3	AAA	AA	555	55	AAA	F0						
Chip Erase		6	AAA	AA	555	55	AAA	80	AAA	AA	555	55	AA A	10
Sector Erase		6	AAA	AA	555	55	AAA	80	AAA	AA	555	55	SA	30
Erase Suspend/Program Suspend		1	XXX	B0										
Erase Resume/Program Resume		1	XXX	30										
Reset		1	XXX	F0										
Unlock Bypass	Enter	3	AAA	AA	555	55	AAA	20						
	Read (6)	1	RA	RD										
	Single Word/Byte Program	2	XXX	A0	PA	PD								
	Write to Buffer (7)	6	SA	25	SA	WC	WBL	PD						
	Program Buffer to Flash (confirm)	1	SA	29										
	Write-to-Buffer-Abort Reset	3	AAA	AA	555	55	AAA	F0						
	Sector Erase	2	XXX	80	SA	30								
	Chip Erase	2	XXX	80	XXX	10								
	Reset	2	XXX	90	XXX	00								
Secured Silicon Sector	Secured Silicon Sector Entry	3	AAA	AA	555	55	AAA	88						
	Read (6)	1	RA	RD										
	Single Word/Byte Program	4	AAA	AA	555	55	AAA	A0	PA	PD				
	Write to Buffer(7)	6	AAA	AA	555	55	SA	25	SA	BC	WBL	PD	WB L	PD
	Program Buffer to Flash (confirm)	1	SA	29										
	Write-to-Buffer-Abort Reset	3	AAA	AA	555	55	AAA	F0						
	Secured Silicon Sector Exit	4	AAA	AA	555	55	AAA	90	XX	00				
Autoselect (8)	Manufacturer ID	4	AAA	AA	555	55	AAA	90	X00	01				
	Device ID	6	AAA	AA	555	55	AAA	90	X02	XX7 E	X1C		X1E	(8)
	Sector Protect Verify	4	AAA	AA	555	55	AAA	90	[SA]X04					
	Secure Device Verify	4	AAA	AA	555	55	AAA	90	X06					
	Reset	1	XXX	F0										
CFI	CFI Query (9)	1	AA	98										
	Read (6)	1	RA	RD										
	Reset	1	XXX	F0										

Legend
X = Don't care
RA = Address of the memory to be read.
RD = Data read from location RA during read operation.
PA = Address of the memory location to be programmed. Addresses latch on the falling edge of the WE# or CE# pulse, whichever happens later.

PD = Data to be programmed at location PA. Data latches on the rising edge of the WE# or CE# pulse, whichever happens first. SA = Address of the sector to be verified (in autoselect mode) or erased. Address bits Amax–A16 uniquely select any sector.
WBL = Write Buffer Location. The address must be within the same write buffer page as PA.
BC = Byte Count is the number of write buffer locations to load minus 1.

Note

1. See ***Table 4*** for description of bus operations.
2. All values are in hexadecimal.
3. All bus cycles are write cycles unless otherwise noted.
4. Data bits DQ15-DQ8 are don't cares for unlock and instruction cycles.
5. Address bits A_{MAX}:A12 are don't cares for unlock and instruction cycles, unless SA or PA required. (A_{MAX} is the Highest Address pin.).
6. No unlock or instruction cycles required when reading array data.
7. Depending on the number of words written, the total number of cycles may be from 6 to 69
8. The fourth, fifth, and sixth cycles of the autoselect instruction sequence are read cycles.
9. Instruction is valid when device is ready to read array data or when device is in autoselect mode.

5.1.4 Sector Protection Instruction Definitions, x8

	Instruction (Notes)	Cycles	Bus Cycles (Notes 1–5)											
			First/ Seventh		Second/ Eighth		Third		Fourth		Fifth		Sixth	
			Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Lock Register	Instruction Set Entry	3	AAA	AA	555	55	AAA	40						
	Bits Program	2	XXX	A0	XXX	DATA								
	Read	1	00	RD										
	Instruction Set Exit	2	XXX	90	XXX	00								
Password Protection	Instruction Set Entry	3	AAA	AA	555	55	AAA	60						
	Password Program (6)	2	XXX	A0	PWAx	PWDx								
	Password Read (7)	8	00	PWD 0	01	PWD 1	02	PWD 2	03	PWD 3	04	PWD 4	05	PWD 5
			06	PWD 6	07	PWD 7								
	Password Unlock (7)	11	00	25	00	03	00	PWD 0	01	PWD 1	02	PWD 2	03	PWD 3
			04	PWD 4	05	PWD 5	06	PWD 6	07	PWD 7	00	29		
	Instruction Set Exit	2	XXX	90	XXX	00								
Global	PPB Instruction Set Entry	3	AAA	AA	55	55	AAA	C0						
	PPB Program	2	XXX	A0	SA	00								
	All PPB Erase	2	XXX	80	00	30								
	PPB Status Read	1	SA	RD(0)										
	PPB Instruction Set Exit	2	XXX	90	XXX	00								
Global	PPB Lock Instruction Set Entry	3	AAA	AA	555	55	AAA	50						
	PPB Lock Bit Set	2	XXX	A0	XXX	00								
	PPB Lock Status Read	1	XXX	RD(0)										
	PPB Lock Instruction Set Exit	2	XXX	90	XXX	00								
Volatile	DYB Instruction Set Entry	3	AAA	AA	555	55	AAA	E0						
	DYB Set	2	XXX	A0	SA	00								
	DYB Clear	2	XXX	A0	SA	01								
	DYB Status Read	1	SA	RD(0)										
	DYB Instruction Set Exit	2	XXX	90	XXX	00								

Legend
X = Don't care RD(0) = Read data.
SA = Sector Address. Address bits Amax–A16 uniquely select any sector. PWD = Password
PWDx = Password word0, word1, word2, and word3.
Data = Lock Register Contents: PD(0) = Secured Silicon Sector Protection Bit, PD(1) = Persistent Protection Mode Lock Bit, PD(2) = Password Protection Mode Lock Bit.

Note
1. See ***Table 4*** for description of bus operations.
2. All values are in hexadecimal.

3. All bus cycles are write cycles unless otherwise noted.
4. Data bits DQ15-DQ8 are don't cares for unlock and instruction cycles.
5. Address bits A_{MAX}:A12 are don't cares for unlock and instruction cycles, unless SA or PA required. (A_{MAX} is the Highest Address pin.)
6. For PWDx, only one portion of the password can be programmed per each "A0" instruction.
7. Note that the password portion can be entered or read in any order as long as the entire 64-bit password is entered or read.

5.2 Read Operations

5.2.1 Read

All memories require access time to output array data. In a read operation, data is read from one memory location at a time. Addresses are presented to the device in random order, and the propagation delay through the device causes the data on its outputs to arrive with the address on its inputs.

The device defaults to reading array data after device power-up or hardware reset. To read data from the memory array, the system must first assert a valid address on A_{max}-A0, while driving OE# and CE# to V_{IL}. WE# must remain at V_{IH}. All addresses get ready on the falling edge of CE#. t_{CE} is equal to the delay from the falling edge of CE# to valid output data. Data is output on DQ15-DQ0 pins after the access time (t_{OE}) has elapsed from the falling edge of OE#, assuming the t_{CE} access time has been meet.

Figure 4. read function (word mode)

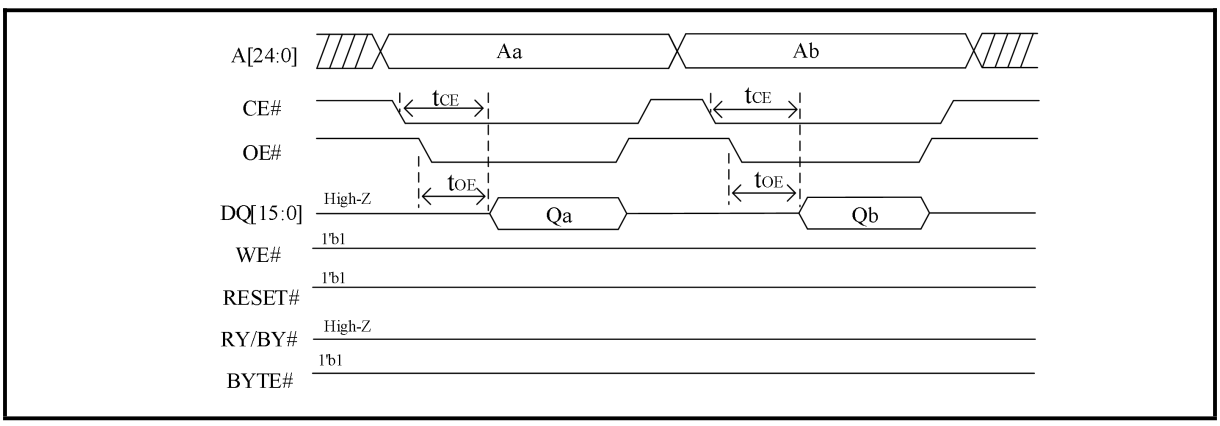
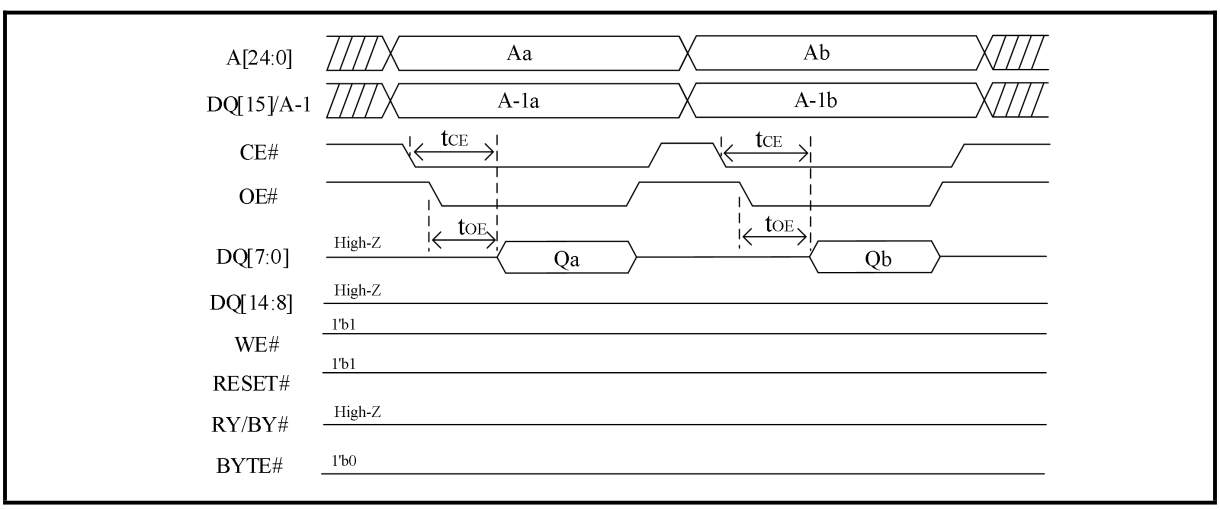


Figure 5. read function (byte mode)



5.2.2 Page Read Mode

The device is capable of fast page mode read and is compatible with the page mode Mask ROM read operation. This mode provides faster read access speed for random locations within a page. The page size of the device is 8 words/16 bytes. The appropriate page is selected by the higher address bits A(max)-A3. Address bits A2-A0 in word mode (A2 to A-1 in byte mode) determine the specific word within a page. The microprocessor supplies the specific word location.

The random or initial page access is equal to t_{ACC} or t_{CE} and subsequent page read accesses (as long as the locations specified by the microprocessor falls within that page) is equivalent to t_{PACC}. When CE# is de-asserted and reasserted for a subsequent access, the access time is t_{ACC} or t_{CE}. Fast page mode accesses are obtained by keeping the “read-page addresses” constant and changing the “intra-read page” addresses.

Figure 6. page read mode function(word mode)

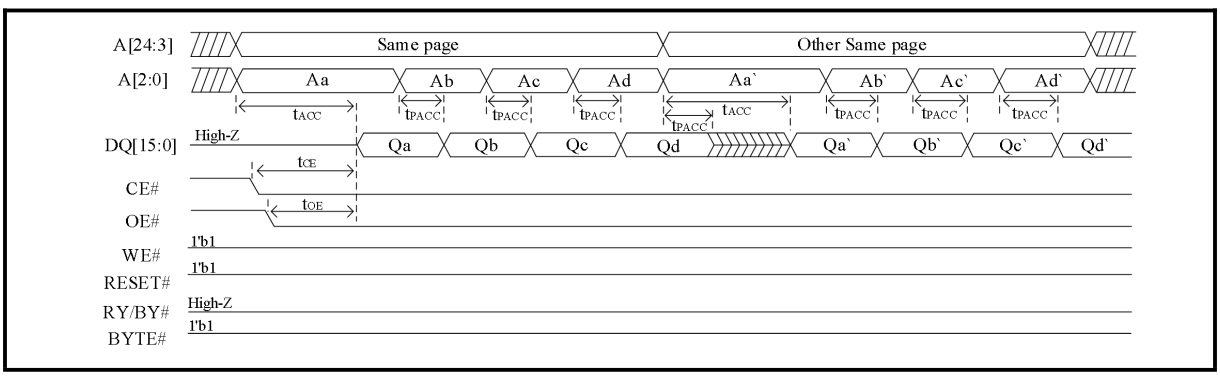
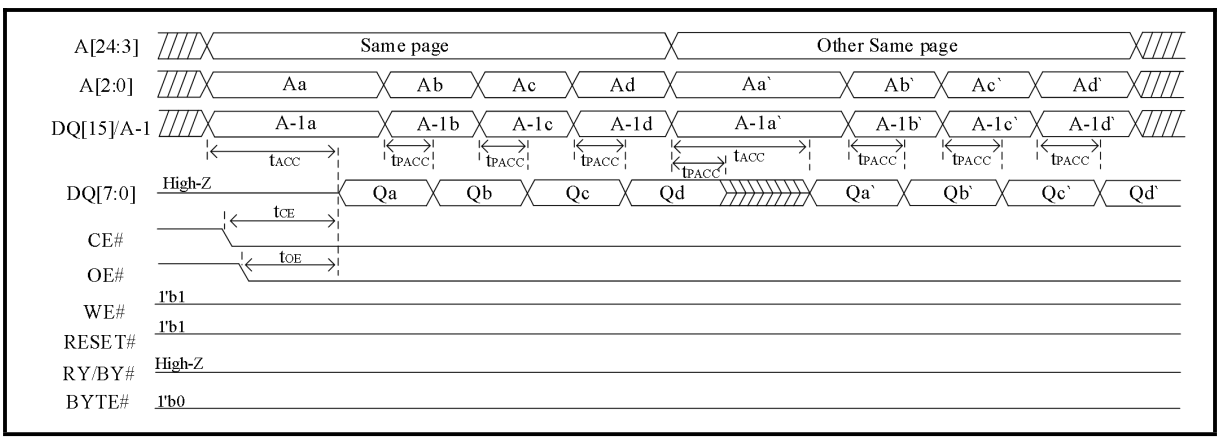


Figure 7. page read mode function(byte mode)



5.3 Program Operations

5.3.1 Single Word/Byte Program

Single Word/Byte Programming mode is one method of programming the Flash. In this mode, four Flash instruction write cycles are used to program an individual Flash address. The data for this programming operation could be 8 (Byte) or 16-bits (Word) wide.

During Single Word/Byte Programming operation, the system must drive CE# and WE# to V_{IL} and OE# to V_{IH} when providing address, instruction, and data. Addresses are latched on the last falling edge of WE# or CE#, while data is latched on the 1st rising edge of WE# or CE#. And CE # can be kept low or pulled high again for each cycle.

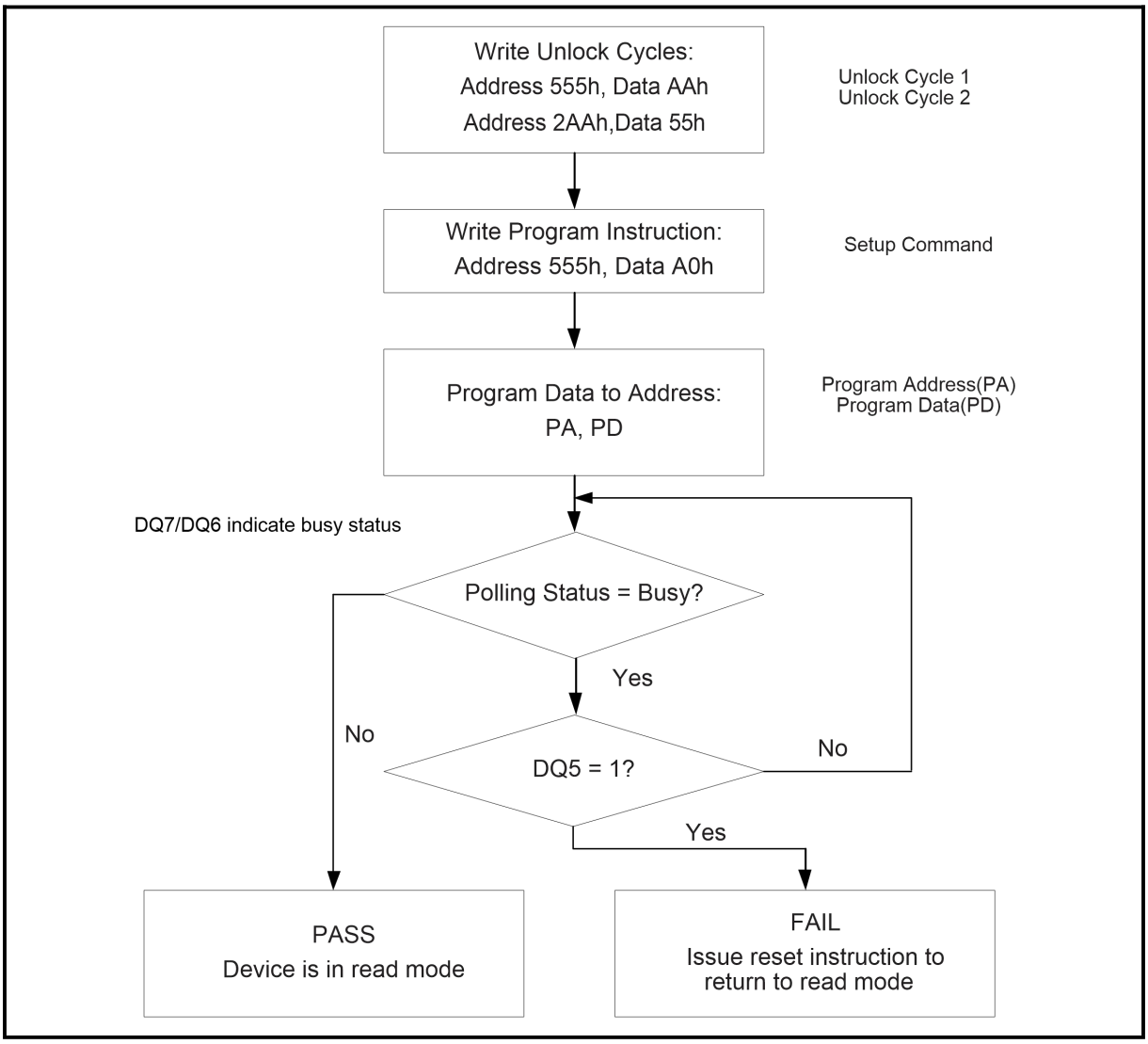
The Unlock Bypass feature allows the host system to send program instructions to the Flash device without first writing unlock cycles within the instruction sequence. See ***Unlock Bypass*** for details on the Unlock Bypass function.

When the Embedded Program algorithm is complete, the device then returns to the read mode and addresses are no longer latched.

Note

1. During programming, any instruction (except the Suspend Program instruction) is ignored.
2. The system can determine the status of the program operation by reading the DQ status bits. Refer to ***Write Operation Status*** for information on these status bits.
3. BUSY can be detected after the program data in the fourth cycle “Program” is sent normally.
4. The Secured Silicon Sector, Autoselect, and CFI functions are unavailable when a program operation is in progress.
5. A hardware reset immediately terminates the program operation. The program instruction sequence should be reinitiated once the device has returned to the read mode, to ensure data integrity.
6. When the Embedded Program algorithm is complete, the device returns to the read mode.
7. An “0” cannot be programmed back to a “1”. A succeeding read shows that the data is still “0”.
8. Only erase operations can convert a “0” to a “1”.
9. Any instructions written to the device during the Embedded Program are ignored except the Suspend instructions.
10. A hardware reset and/or power removal immediately terminates the Program operation and the Program instruction sequence should be reinitiated once the device has returned to the read mode to ensure data integrity.
11. Programming to the same word address multiple times without intervening erases is permitted.

Figure 8. Single Word/Byte Program



Software Functions and Sample Code

Single Word/Byte Program

Cycle	Operation	Byte Address	Word Address	Data
Unlock Cycle 1	Write	AAAh	555h	00AAh
Unlock Cycle 2	Write	555h	2AAh	0055h
Program Setup	Write	AAAh	555h	00A0h
Program	Write	Byte Address	Word Address	Data

Figure 9. Single Word/Byte Program (word mode)

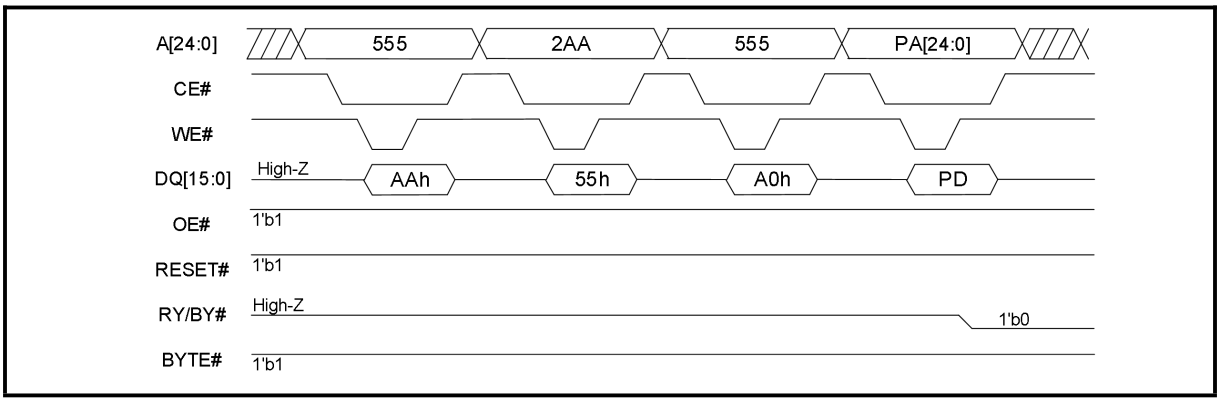
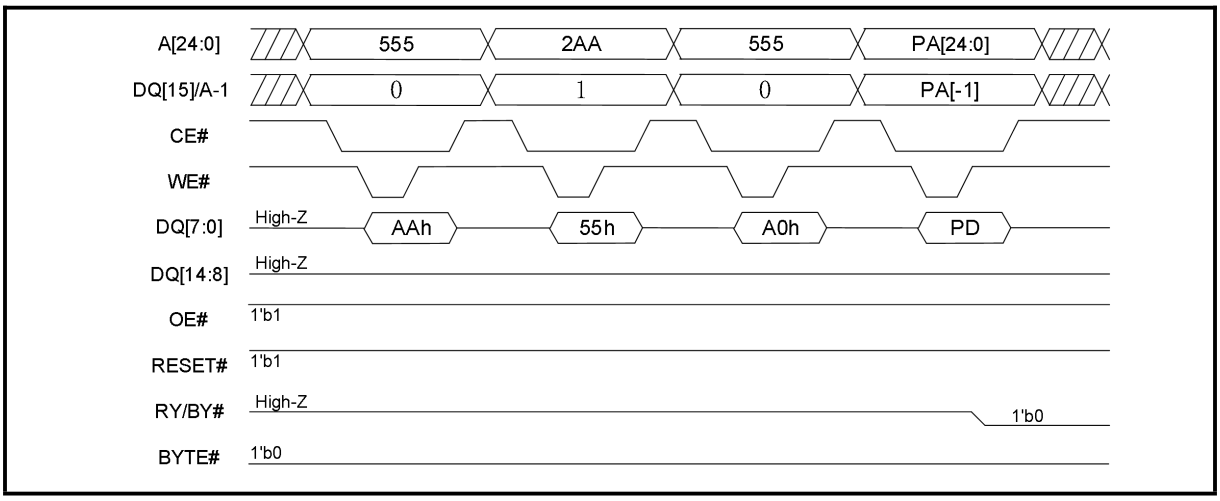


Figure 10. Single Word/Byte Program (byte mode)



5.3.2 Write Buffer Program

Write Buffer Programming allows the system to write a maximum of 32 words in one programming operation. This results in a faster effective word programming time than the standard “word” programming algorithms. The Write Buffer Programming instruction sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle containing the Write Buffer Load instruction written at the Sector Address in which programming occurs.

During Write Buffer Programming operation, the system must drive CE# and WE# to V_{IL} and OE# to V_{IH} when providing address, instruction, and data. Addresses are latched on the last falling edge of WE# or CE#, while data is latched on the 1st rising edge of WE# or CE#. And CE # can be kept low or pulled high again for each cycle.

The Unlock Bypass feature allows the host system to send program instructions to the Flash device without first writing unlock cycles within the instruction sequence. See ***Unlock Bypass*** for details on the Unlock Bypass function.

At this point, the system writes the number of “word locations minus 1” that are loaded into the page buffer at the Sector Address in which programming occurs. This tells the device how many write buffer addresses are loaded with data and therefore when to expect the “Program Buffer to Flash” confirm instruction. The number of locations to program cannot exceed the size of the write buffer or the operation aborts. (Number loaded = the number of locations to program minus 1. For example, if the system programs 6 address locations, then 05h should be written to the device.)

The system then writes the starting address/data combination. This starting address is the first address/data pair to be programmed, and selects the “write-buffer-page” address. All subsequent address/data pairs must fall within the elected write-buffer-page.

The “write-buffer-page” is selected by using the addresses A_{MAX}–A5.

The “write-buffer-page” addresses must be the same for all address/data pairs loaded into the write buffer. (This means Write Buffer Programming cannot be performed across multiple “write-buffer-pages”. This also means that Write Buffer Programming cannot be performed across multiple sectors. If the system attempts to load programming data outside of the selected “write-buffer-page”, the operation ABORTs.)

After writing the Starting Address/Data pair, the system then writes the remaining address/data pairs into the write buffer.

Note that if a Write Buffer address location is loaded multiple times, the “address/data pair” counter is decremented for every data load operation. Also, the last data loaded at a location before the “Program Buffer to Flash” confirm instruction is the data programmed into the device. It is the software's responsibility to comprehend ramifications of loading a write-buffer location more than once. The counter decrements for each data load operation, NOT for each unique write-buffer-address location. Once the specified number of write buffer locations have been loaded, the system must then write the “Program Buffer to Flash” instruction at the Sector Address. Any other address/data write combinations abort the Write Buffer Programming operation. The Write Operation Status bits should be used while monitoring the last address location loaded into the write buffer. This eliminates the need to store an address in memory because the system can load the last address location, issue the program confirm instruction at the last loaded address location, and then check the write operation status at that same address. DQ7, DQ6, DQ5, and DQ1 should be monitored to determine the device status during Write Buffer Programming.

The write-buffer “embedded” programming operation can be suspended using the standard suspend/resume instructions. Upon successful completion of the Write Buffer Programming operation, the device returns to READ mode.

The Write Buffer Programming Sequence is ABORTED under any of the following conditions:

1. Load a value that is greater than the page buffer size during the “Number of Locations to Program” step.
2. Write to an address in a sector different than the one specified during the Write-Buffer-Load instruction.

3. Write an Address/Data pair to a different write-buffer-page than the one selected by the “Starting Address” during the “write buffer data loading” stage of the operation.
4. Writing anything other than the Program to Buffer Flash Instruction after the specified number of “data load” cycles.

The ABORT condition is indicated by DQ1 = 1, DQ7 = DATA# (for the “last address location loaded”), DQ6 = TOGGLE, DQ5 = 0. This indicates that the Write Buffer Programming Operation was ABORTED. A “Write-to-Buffer-Abort reset” instruction sequence is required when Write Buffer Programming Operation was ABORTED.

Write buffer programming is allowed in any sequence of memory (or address) locations. These flash devices are capable of handling multiple write buffer programming operations on the same write buffer address range without intervening erases.

Note

1. During programming, any instruction (except the Suspend Program instruction) is ignored.
2. The system can determine the status of the program operation by reading the DQ status bits. Refer to ***Write Operation Status*** for information on these status bits.
3. BUSY can be detected after the “0029h” in the last cycle “Write Buffer to Flash” is sent normally or after ABORT condition.
4. The Secured Silicon Sector, Autoselect, and CFI functions are unavailable when a program operation is in progress.
5. A hardware reset immediately terminates the program operation. The program instruction sequence should be reinitiated once the device has returned to the read mode, to ensure data integrity.
6. When the Embedded Program algorithm is complete, the device returns to the read mode.
7. An “0” cannot be programmed back to a “1”. A succeeding read shows that the data is still “0”.
8. Only erase operations can convert a “0” to a “1”.
9. Any instructions written to the device during the Embedded Program are ignored except the Suspend instructions.
10. A hardware reset and/or power removal immediately terminates the Program operation and the Program instruction sequence should be reinitiated once the device has returned to the read mode to ensure data integrity.
11. Programming to the same word address multiple times without intervening erases is permitted.

Software Functions and Sample Code

Write Buffer Program

Cycle	Description	Operation	Byte Address	Word Address	Data
1	Unlock	Write	AAAh	555h	00AAh
2	Unlock	Write	555h	2AAh	0055h
3	Write Buffer Load Instruction	Write	Sector Address		0025h
4	Write Word Count	Write	Sector Address		Word/Byte Count (N–1)
5	Load Buffer Word/Byte N	Write	PA_1		Word/Byte 1
⋮	⋮	⋮	⋮		⋮
N+4	Load Buffer Word/Byte N	Write	PA_N		Word/Byte N
Last	Write Buffer to Flash	Write	Sector Address		0029h

Note

1. *PA = Address of the memory location to be programmed.*
2. *Number of words (Word N) loaded into the write buffer can be from 1 to 32 words (1 to 64 bytes).*
3. *Last = Last cycle of write buffer program operation; depending on number of words written, the total number of cycles may be from 6 to 37(x16) or 6 to 69(x8).*
4. *For maximum efficiency, it is recommended that the write buffer be loaded with the highest number of words or bytes (N words or N bytes) possible.*

Figure 11. Write Buffer Programming Operation

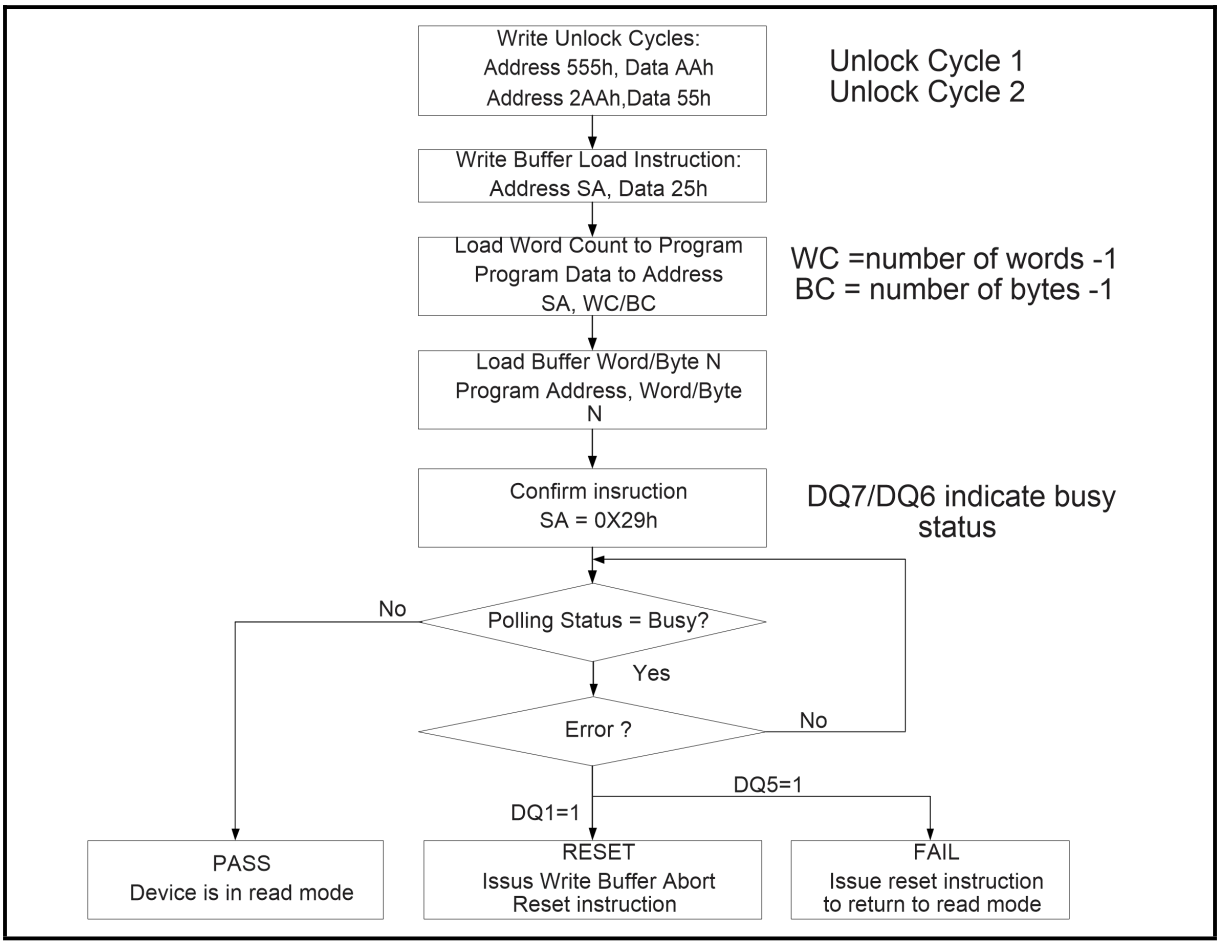


Figure 12. Write Buffer Programming (word mode)

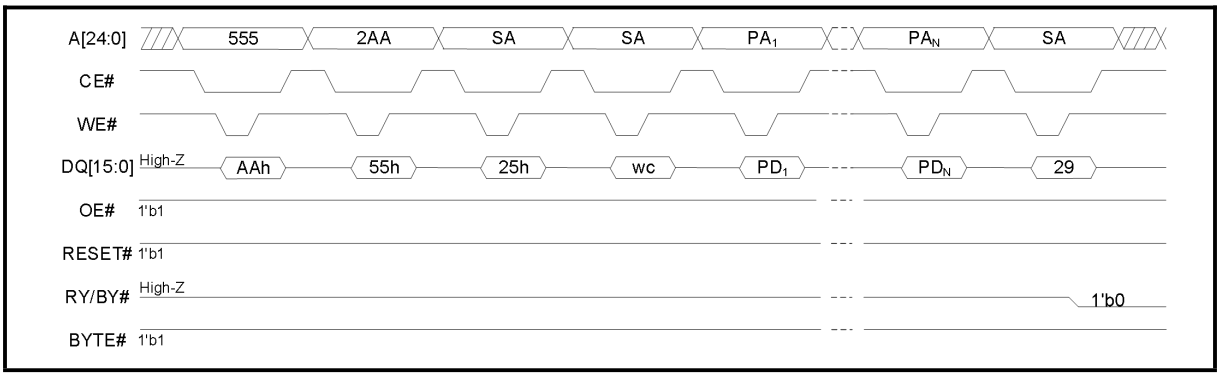
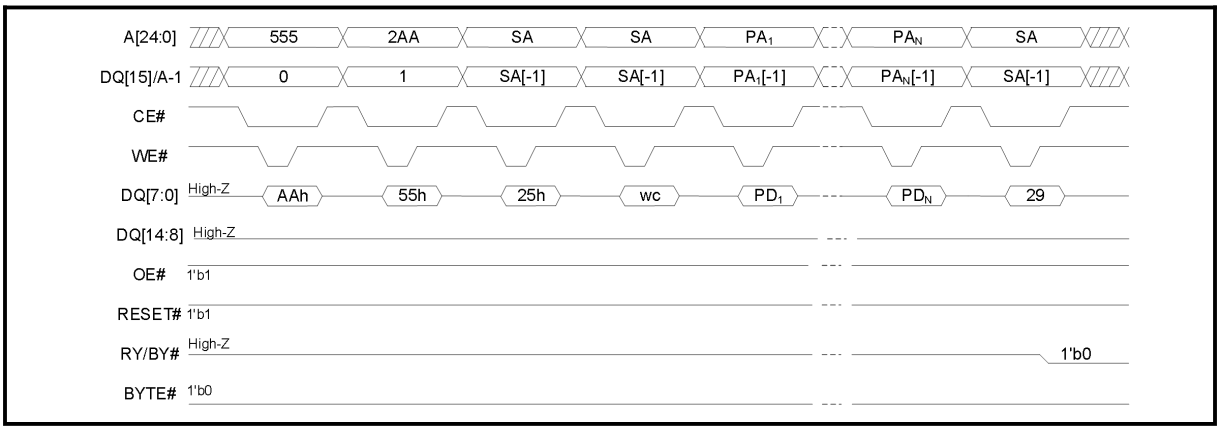


Figure 13. Write Buffer Programming (byte mode)



5.3.3 Accelerated Program

Accelerated Single Word/Byte Programming and write buffer programming operations are enabled through the WP#/ACC pin. This method is faster than the standard program instruction sequences.

Note

1. If the system asserts V_{HH} on this input, the device automatically enters the aforementioned Unlock Bypass mode and uses the higher voltage on the input to reduce the time required for program operations. The system can then use the Write Buffer Load instruction sequence provided by the Unlock Bypass mode. Note that if a “Write-to-Buffer-Abort Reset” is required while in Unlock Bypass mode, the full 3-cycle RESET instruction sequence must be used to reset the device. Removing V_{HH} from the ACC input, upon completion of the embedded program operation, returns the device to normal operation.
2. Sectors must be unlocked prior to raising WP#/ACC to V_{HH}.
3. The WP#/ACC pin must not be at V_{HH} for operations other than accelerated programming, or device damage may result.
4. It is recommended that WP#/ ACC apply V_{HH} after power-up sequence is completed. In addition, it is recommended that WP#/ ACC apply from V_{HH} to V_{IH}/V_{IL} before powering down V_{CC}/V_{IO}.

5.4 Erase Operations

5.4.1 Sector Erase

The sector erase function erases one or more sectors in the memory array. After a successful sector erase, all locations within the erased sector contain FFFFh. During sector erase operation, the system must drive CE# and WE# to V_{IL} and OE# to V_{IH} when providing address, instruction, and data. Addresses are latched on the last falling edge of WE# or CE#, while data is latched on the 1st rising edge of WE# or CE#. And CE # can be kept low or pulled high again for each cycle.

The Unlock Bypass feature allows the host system to send program instructions to the Flash device without first writing unlock cycles within the instruction sequence. See ***Unlock Bypass*** for details on the Unlock Bypass function.

After the instruction sequence is written, the sector erase time-out t_{SEA} (50 μs) occurs. During the time-out period, additional sector addresses may be written. Loading the sector erase buffer may be done in any sequence, and the number of sectors may be from one sector to all sectors. The time between these additional cycles must be less than 50 μs. Any sector erase address and instruction following the exceeded time-out (50 μs) may or may not be accepted. Any instruction other than Sector Erase or Erase Suspend during the time-out period resets that sector to the read mode. The system can monitor DQ3 to determine if the sector erase timer has timed out The time-out begins from the rising edge of the final WE# pulse in the instruction sequence.

When the Embedded Erase algorithm is complete, the sector returns to reading array data and addresses are no longer latched. The system can determine the status of the erase operation by reading DQ7/DQ5/DQ6/DQ2 in the erasing sector.

Once the sector erase operation has begun, only the Erase Suspend instruction is valid. All other instructions are ignored. However, note that a hardware reset immediately terminates the erase operation. If that occurs, the sector erase instruction sequence should be reinitiated once that sector has returned to reading array data, to ensure the sector is properly erased.

The Unlock Bypass feature allows the host system to send erase instructions to the Flash device without first writing unlock cycles within the instruction sequence.

If not all selected sectors are protected, the sector erase function erases the unprotected sectors, and ignores the selected sectors that are protected.

Figure 14 illustrates the algorithm for the erase operation.

Table 5. Sector Erase

Cycle	Description	Operation	Byte Address	Word Address	Data
1	Unlock	Write	AAAh	555h	00AAh
2	Unlock	Write	555h	2AAh	0055h
3	Setup Instruction	Write	AAAh	555h	0080h
4	Unlock	Write	AAAh	555h	00AAh
5	Unlock	Write	555h	2AAh	0055h
6	Sector Erase Instruction	Write	SA_0	SA_0	0030h
⋮	⋮	⋮	⋮	⋮	⋮
N+6	Sector Erase Instruction	Write	SA_N	SA_N	0030h

Note

1. *SA = Sector Address.*
2. *Unlimited additional sectors may be selected for erase; instruction(s) must be written within 50 μs.*

Figure 14. Sector Erase Operation

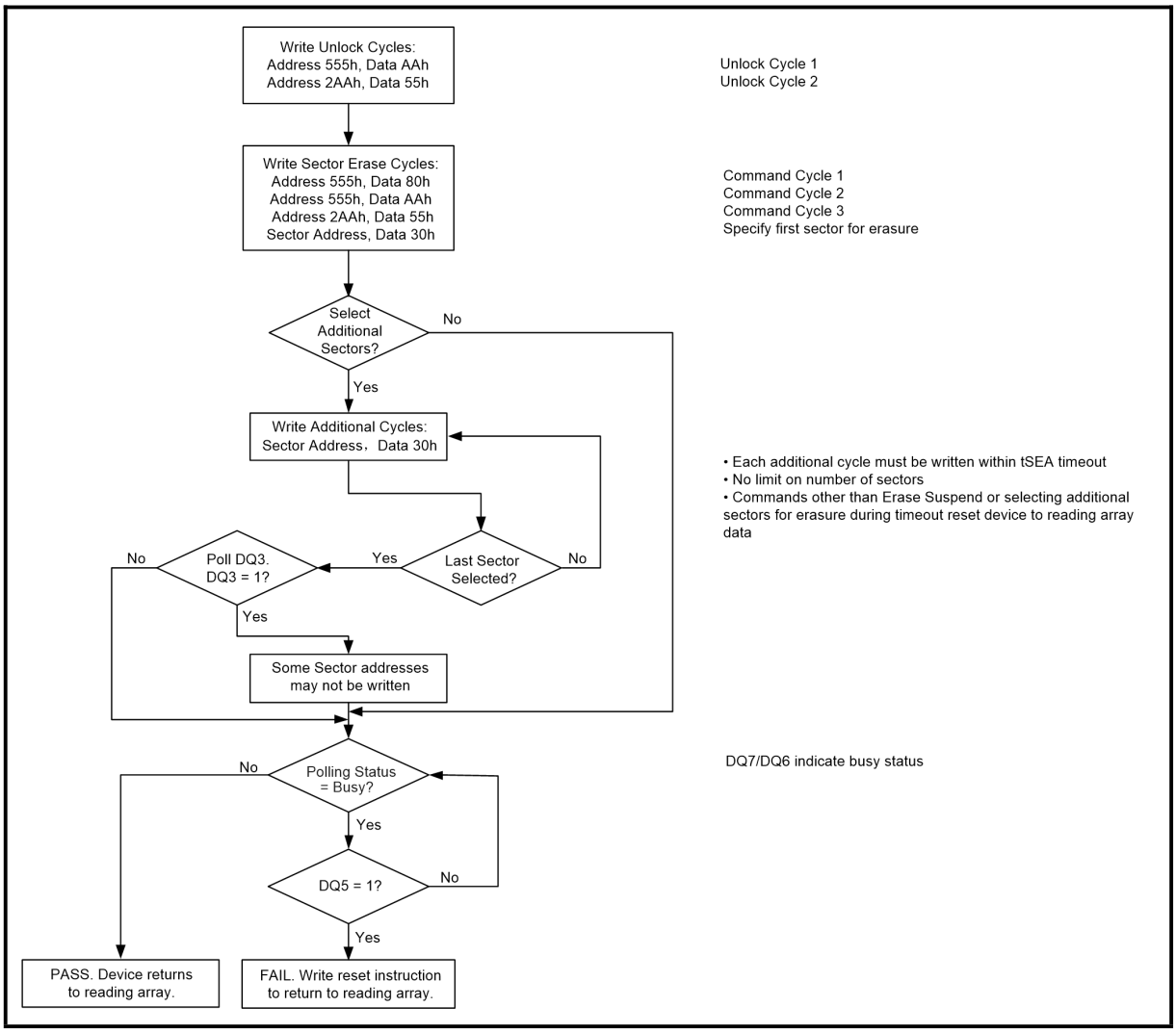


Figure 15. Sector Erase (word mode)

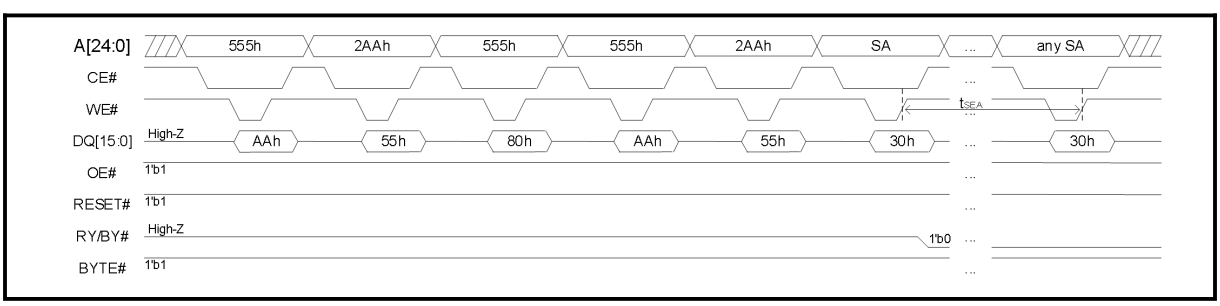
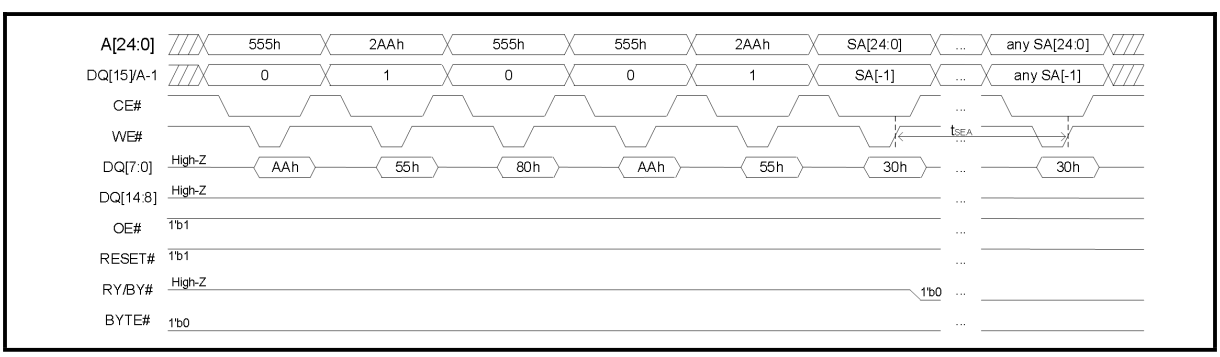


Figure 16. Sector Erase (byte mode)



5.4.2 Chip Erase

After a successful chip erase, all locations of the chip contain FFFFh. The system is not required to provide any controls or timings during these operations. During chip erase operation, the system must drive CE# and WE# to V_{IL} and OE# to V_{IH} when providing address, instruction, and data. Addresses are latched on the last falling edge of WE# or CE#, while data is latched on the 1st rising edge of WE# or CE#. And CE # can be kept low or pulled high again for each cycle.

The Unlock Bypass feature allows the host system to send program instructions to the Flash device without first writing unlock cycles within the instruction sequence. See ***Unlock Bypass*** for details on the Unlock Bypass function.

When the Embedded Erase algorithm is complete, that sector returns to the read mode and addresses are no longer latched. The system can determine the status of the erase operation by using DQ7 or DQ6/DQ2. Refer to “Write Operation Status” for information on these status bits.

The Unlock Bypass feature allows the host system to send program instructions to the Flash device without first writing unlock cycles within the instruction sequence.

Any instructions written during the chip erase operation are ignored. However, note that a hardware reset immediately terminates the erase operation. If that occurs, the chip erase instruction sequence should be reinitiated once that sector has returned to reading array data, to ensure the entire array is properly erased.

If not all selected sectors are protected, the chip erase function erases the unprotected sectors, and ignores the selected sectors that are protected.

Figure 17. Chip Erase Operation

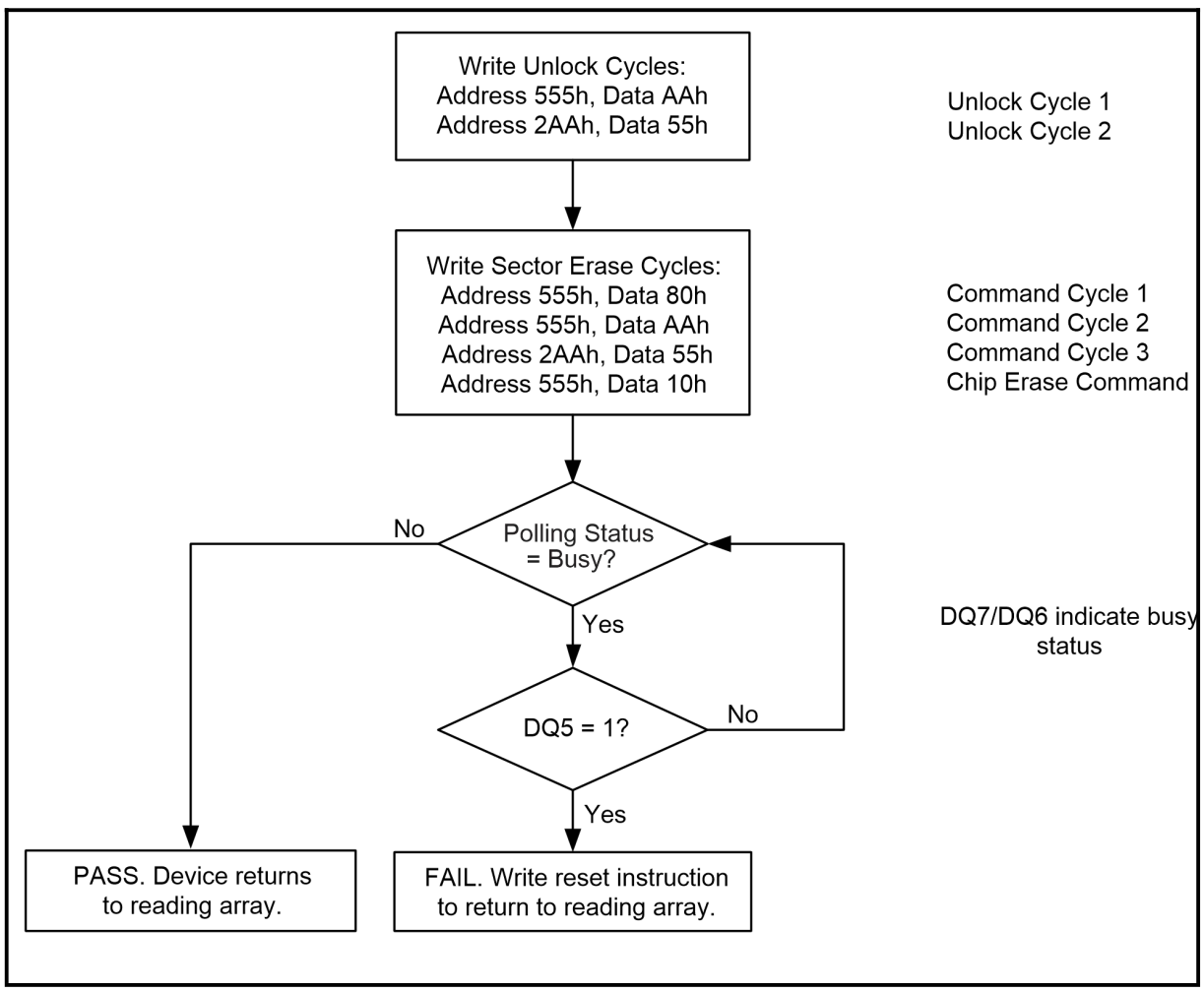


Table 6. Chip Erase

Cycle	Description	Operation	Byte Address	Word Address	Data
1	Unlock	Write	AAAh	555h	00AAh
2	Unlock	Write	555h	2AAh	0055h
3	Setup Instruction	Write	AAAh	555h	0080h
4	Unlock	Write	AAAh	555h	00AAh
5	Unlock	Write	555h	2AAh	0055h
6	Sector Erase Instruction	Write	AAAh	555h	0010h

Figure 18. Chip Erase (word mode)

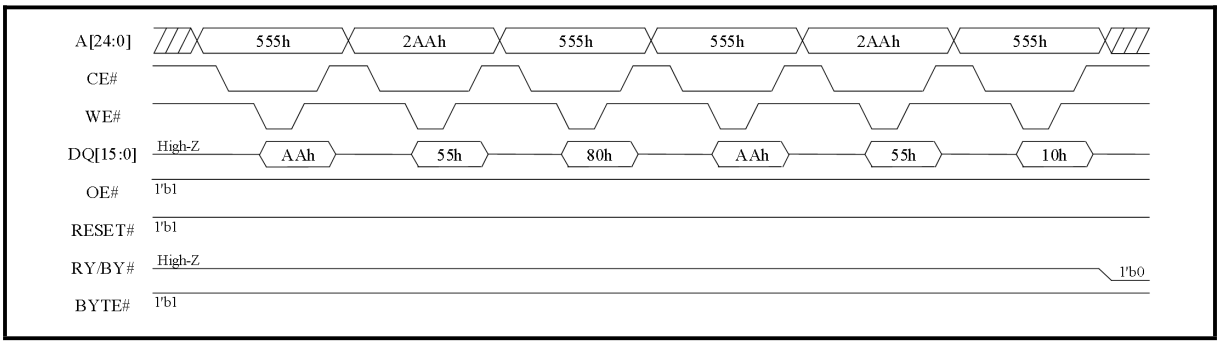
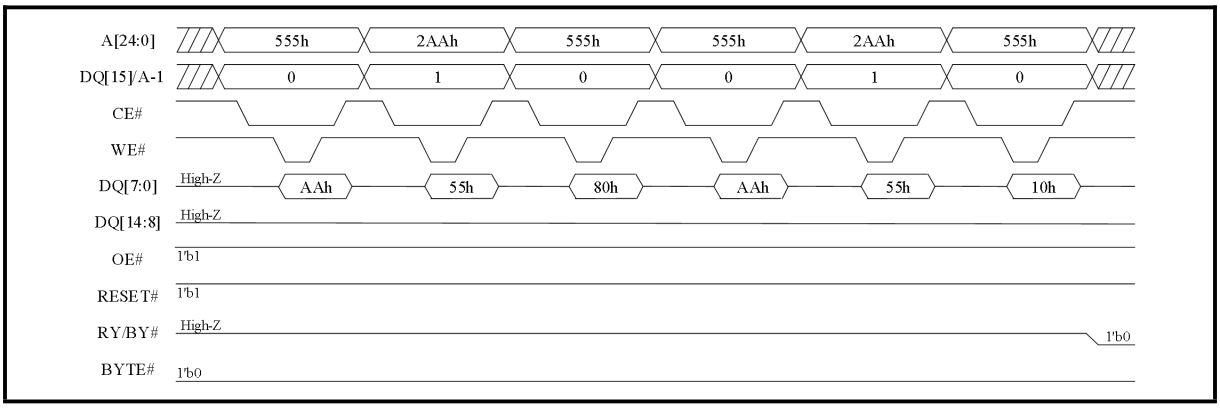


Figure 19. Chip Erase (byte mode)



5.5 Suspend/Resume Operations

5.5.1 Program Suspend/Program Resume Instructions

The Program Suspend instruction allows the system to interrupt an embedded programming operation or a “Write to Buffer” programming operation so that data can read from any non-suspended buffer-page(buffer-page is selected by using the addresses A_{MAX}–A5). When the Program Suspend instruction is written during a programming process, the device halts the programming operation within t_{PSL} (45 μs maximum (20 μs typical)) and updates the status bits. Addresses are “don't-cares” when writing the Program Suspend instruction.

After the programming operation has been suspended, the system can read array data from any non-suspended buffer-page. The Program Suspend instruction may also be issued during a programming operation while an erase is suspended. In this case, data may be read from any addresses not within both a Big block in Erase Suspend and a buffer-page in Program Suspend. while an program is suspended, if a read is needed from the Secured Silicon Sector area, then user must use the proper instruction sequences to enter and exit this region.

The system may also write the Autoselect Instruction Sequence when the device is in Program Suspend mode. The device allows reading Autoselect codes in the suspended sectors, since the codes are not stored in the memory array. When the device exits the Autoselect mode, the device reverts to Program Suspend mode, and is ready for another valid operation. See ***Autoselect*** for more information.

After the Program Resume instruction is written, the device reverts to programming. The system can determine the status of the program operation using the write operation status bits, just as in the standard program operation. See ***Write Operation Status*** for more information.

The system must write the Program Resume instruction (address bits are “don't care”) to exit the Program Suspend mode and continue the programming operation. Further writes of the Program Resume instruction are ignored. Another Program Suspend instruction can be written after the device has resumed programming.

Acceptable instructions During Program Suspend after t_{PSL}

Instruction		Notes
Read		data can read from any non-suspended buffer-page.
Program Resume		
Reset		
Unlock Bypass	Enter	
	Read	data can read from any non-suspended buffer-page.
	Reset	
Secured Silicon Sector	Secured Silicon Sector Entry	
	Read	
	Secured Silicon Sector Exit	
Autoselect ct	Manufacturer ID	
	Device ID	
	Sector Protect Verify	
	Secure Device Verify	
	Reset	
CFI	CFI Query	
	Read	
	Reset	

Figure 20. Program Suspend (word mode)

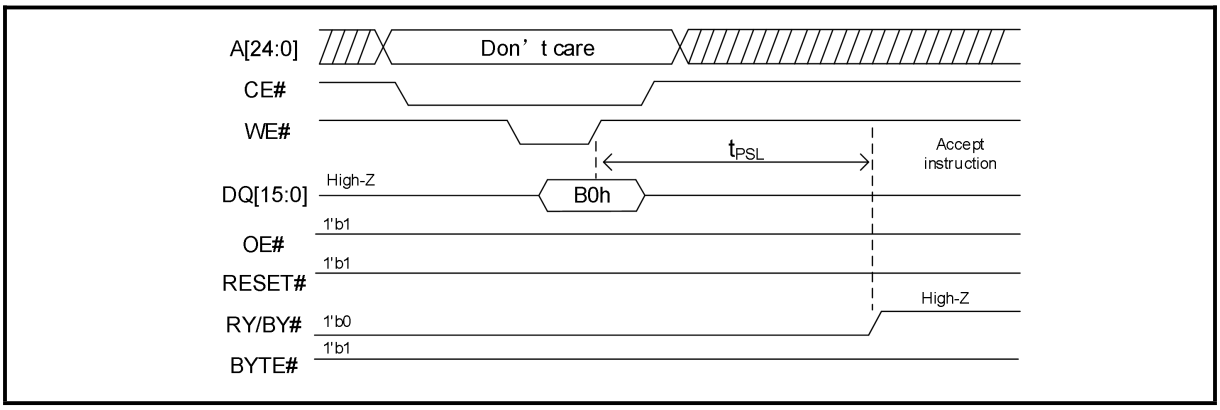


Figure 21. Program Suspend (byte mode)

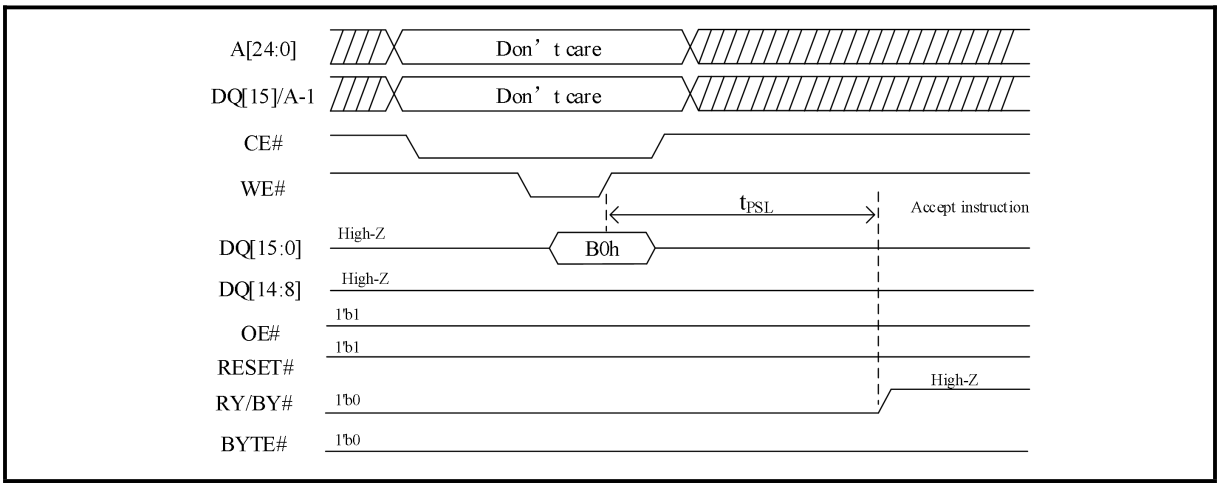


Figure 22. Program Resume (word mode)

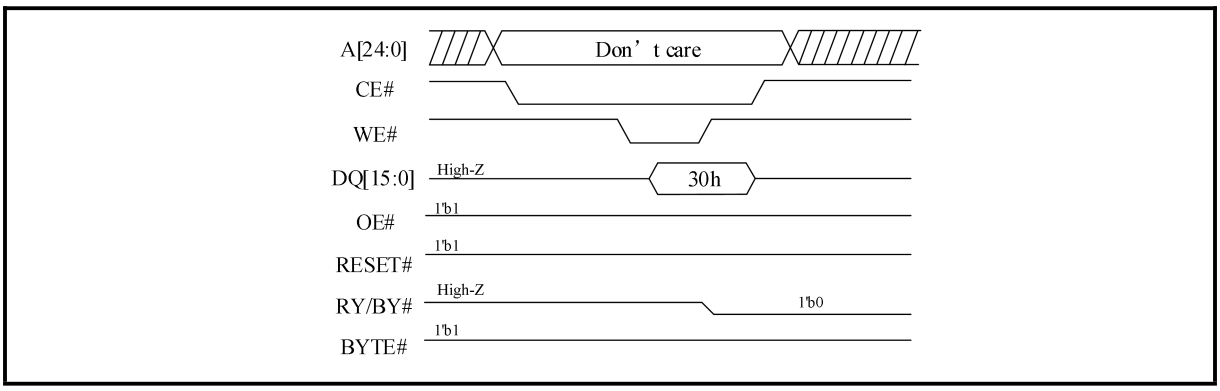
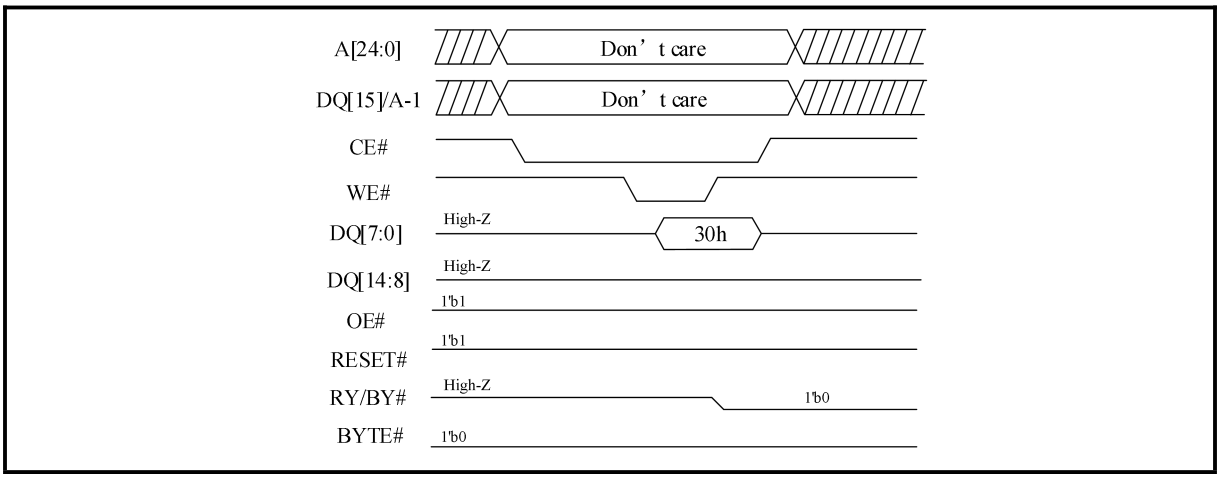


Figure 23. Program Resume (byte mode)



5.5.2 Erase Suspend/Erase Resume Instructions

The Erase Suspend instruction allows the system to interrupt a sector erase operation and then read data from, or program data to, any Big Block not selected for erasure. The sector addresses are “don't-cares” when writing this instruction. This instruction is valid only during the sector erase operation, including the t_{SEA} time-out period during the sector erase instruction sequence. The Erase Suspend instruction is ignored if written during the chip erase operation.

When the Erase Suspend instruction is written during the sector erase operation, the device requires a maximum of t_{ESL} (45μs (20μs typical)) to suspend the erase operation. However, when the Erase Suspend instruction is written during the sector erase time-out, the device immediately terminates the time-out period and suspends the erase operation.

After the erase operation has been suspended, the device enters the erase-suspend-read mode. The system can read data from or program data to Big Block not selected for erasure. (The device “erase suspends” all sectors selected for erasure.) Reading at any address within erase-suspended sectors produces status information on DQ7-DQ0. The system can use DQ7, or DQ6, DQ5, and DQ2 together, to determine if a sector is actively erasing or is erase-suspended.

After an erase-suspended program operation is complete, the device returns to the erase-suspend-read mode. The system can determine the status of the program operation using write operation status bits, just as in the standard program operation.

In the erase-suspend-read mode, the system can also issue the Autoselect instruction sequence.

To resume the sector erase operation, the system must write the Erase Resume instruction. The address of the erase-suspended sector is a “don't-care” when writing this instruction. Further writes of the Resume instruction are ignored. Another Erase Suspend instruction can be written after the chip has resumed erasing.

Acceptable instructions During Erase Suspend after t_{ESL}

Instruction		Notes
Read		read data from any Big Block not selected for sector erase.
Single Word/Byte Program		program data to any Big Block not selected for sector erase.
Write to Buffer		program data to any Big Block not selected for sector erase.
Program Buffer to Flash (Confirm)		
Write-to-Buffer-Abort Reset		
Program Suspend		
Erase Resume		
Reset		
Unlock Bypass	Enter	
	Read	read data from any Big Block not selected for sector erase.
	Single Word/Byte Program	program data to any Big Block not selected for sector erase.
	Write to Buffer	program data to any Big Block not selected for sector erase.
	Program Buffer to Flash (Confirm)	
	Write-to-Buffer-Abort Reset	
	Reset	
Secured Silicon Sector	Secured Silicon Sector Entry	
	Read	
	Single Word/Byte Program	
	Write to Buffer	
	Program Buffer to Flash (Confirm)	
	Write-to-Buffer-Abort Reset	
	Secured Silicon Sector Exit	

Autoselect	Manufacturer ID	
	Device ID	
	Sector Protect Verify	
	Secure Device Verify	
	Reset	
CFI	CFI Query	
	Read	
	Reset	

Figure 24. Erase Suspend (word mode)

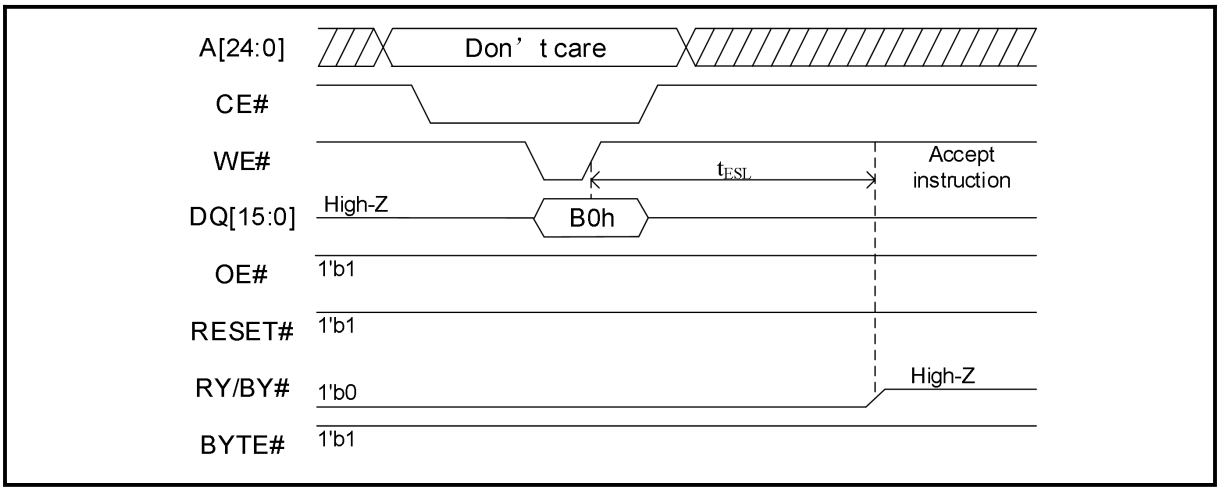


Figure 25. Erase Suspend (byte mode)

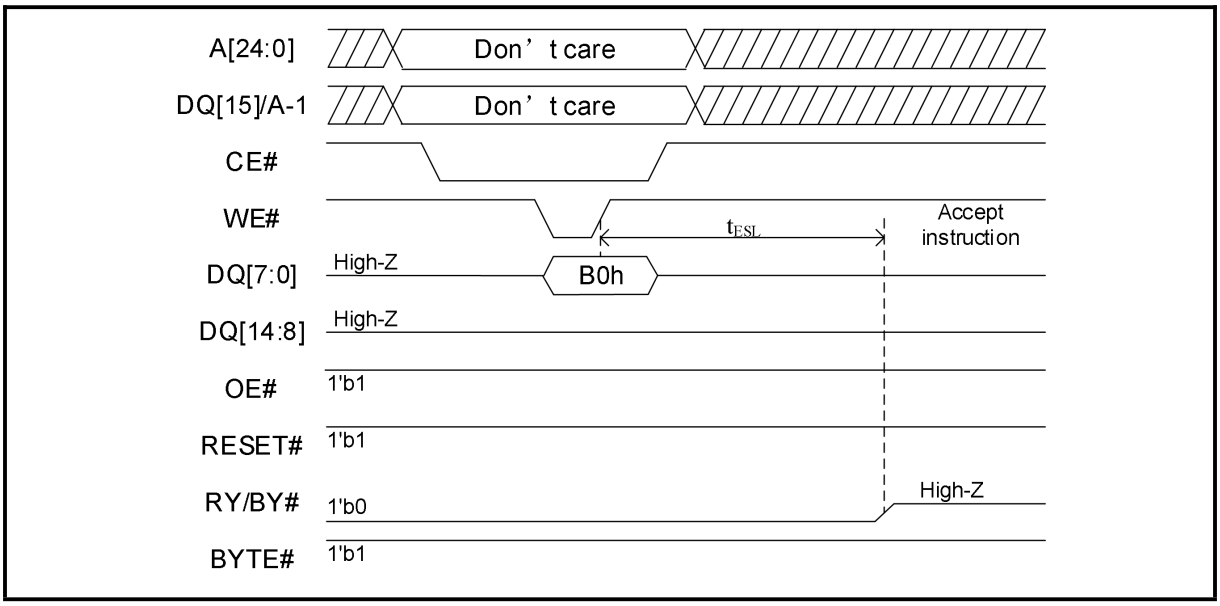


Figure 26. Erase Resume (word mode)

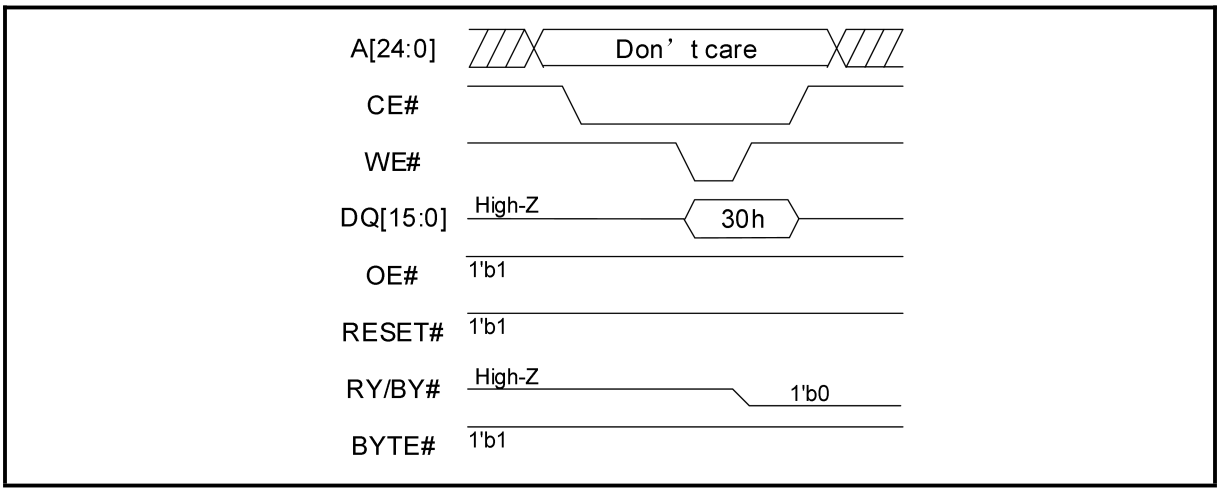
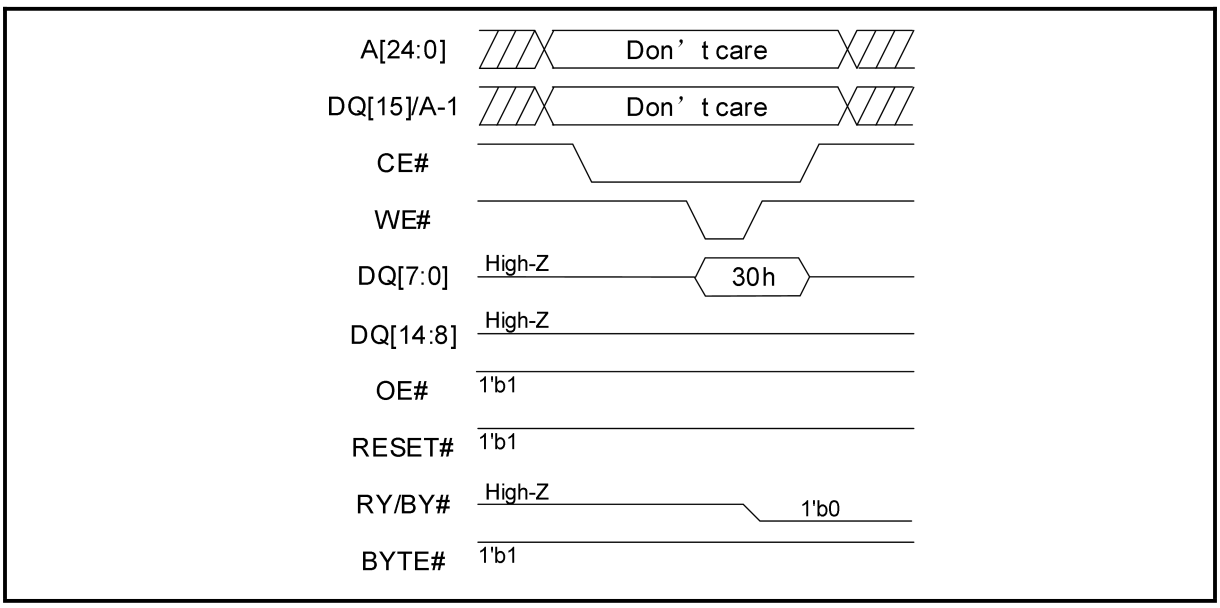


Figure 27. Erase Resume (byte mode)



5.6 Unlock Bypass

This device features an Unlock Bypass mode to facilitate shorter program/erase instructions. Once the device enters the Unlock Bypass mode, only two write cycles are required to program data, instead of the normal four cycles. The ***Instruction Definitions*** shows the requirements for the unlock bypass instruction sequences.

During the unlock bypass mode, only the Read, Program, Write Buffer Programming, Write-to-Buffer-Abort Reset, Unlock Bypass Sector Erase, Unlock Bypass Chip Erase and Unlock Bypass Reset instructions are valid. To exit the unlock bypass mode, the system must issue the two-cycle unlock bypass reset instruction sequence. The first cycle address is “don't care” and the data 90h. The second cycle need only contain the data 00h. The sector then returns to the read mode.

Software Functions and Sample Code

Unlock Bypass Entry

Cycle	Description	Operation	Byte Address	Word Address	Data
1	Unlock	Write	AAAh	555h	00AAh
2	Unlock	Write	555h	2AAh	0055h
3	Entry Instruction	Write	AAAh	555h	0020h

Unlock Bypass Program

Cycle	Description	Operation	Byte Address	Word Address	Data
1	Program Setup	Write	XXXh	XXXh	00A0h
2	Program Instruction	Write	Program Address	Program Address	Program Data

Unlock Bypass Reset

Cycle	Description	Operation	Byte Address	Word Address	Data
1	Reset Cycle 1	Write	XXXh	XXXh	0090h
2	Reset Cycle 2	Write	XXXh	XXXh	0000h

Figure 28. Unlock Bypass Entry (word mode)

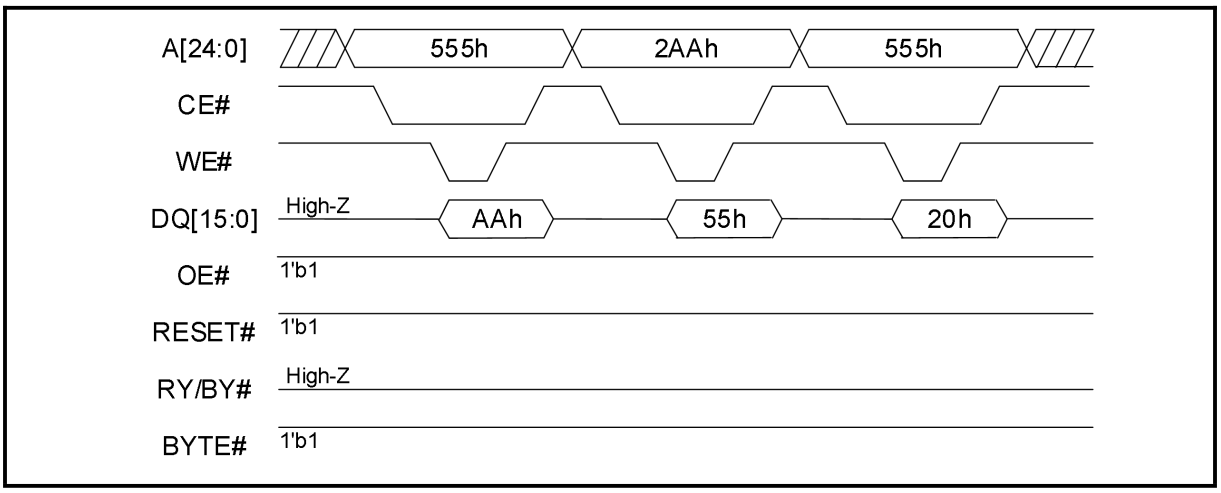


Figure 29. Unlock Bypass Entry (byte mode)

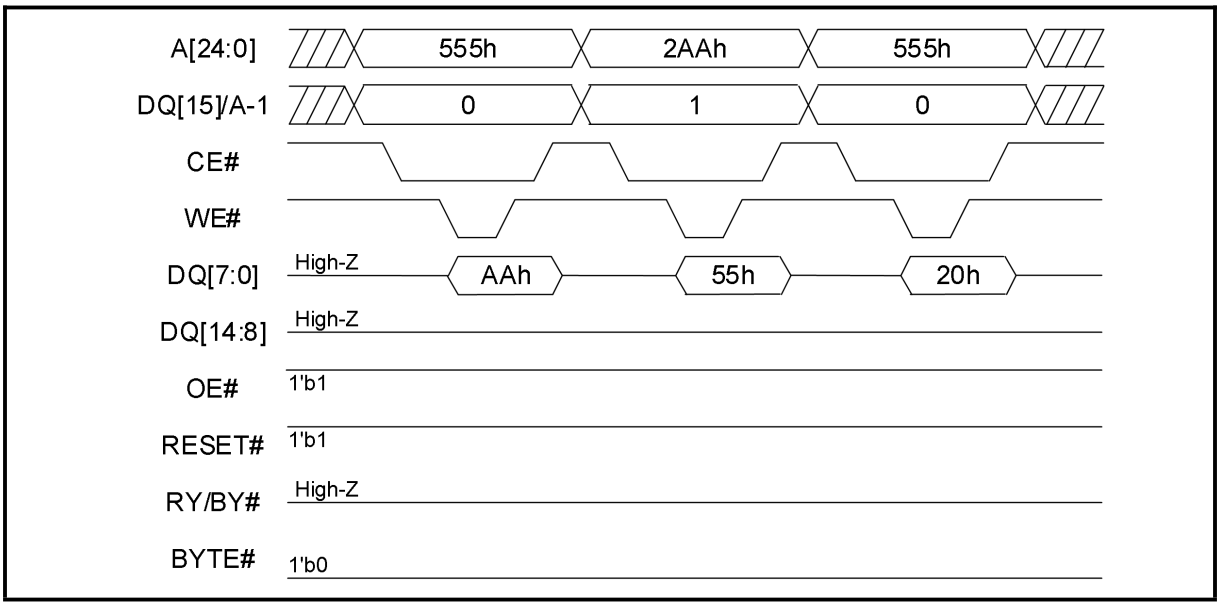


Figure 30. Unlock Bypass Reset (word mode)

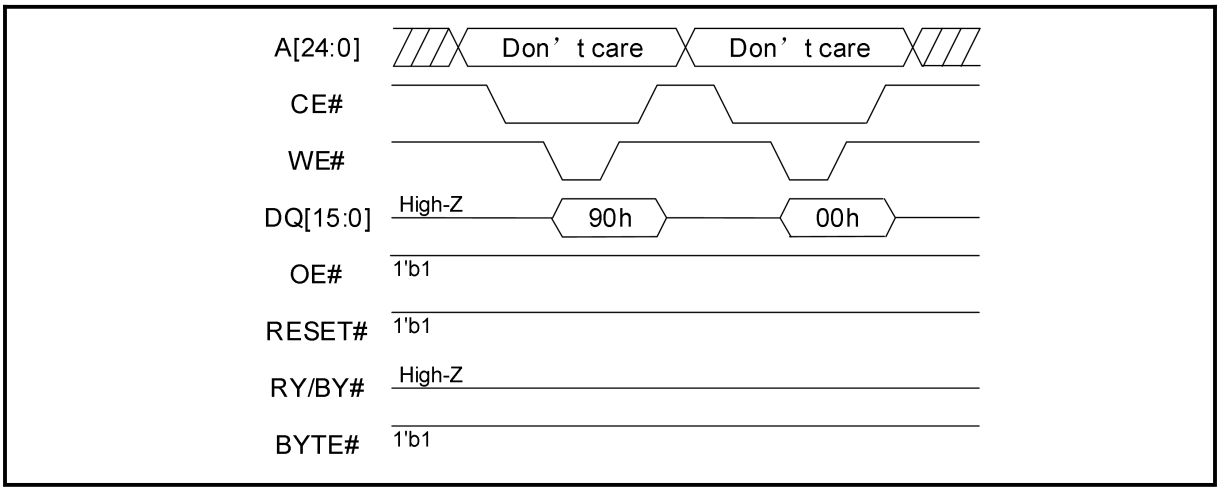
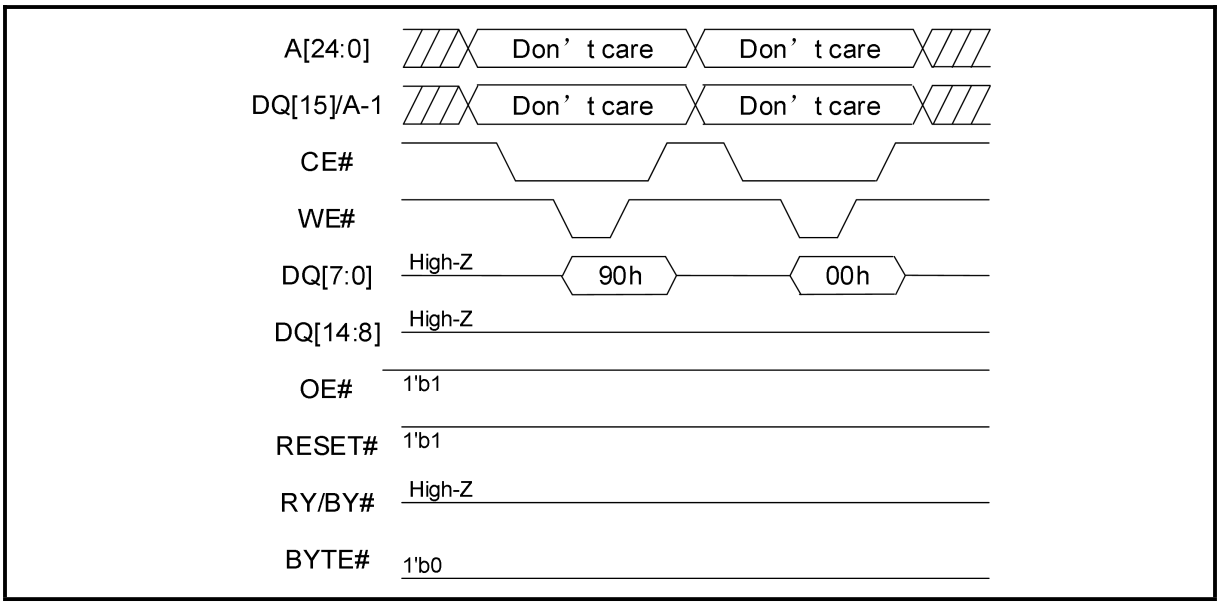


Figure 31. Unlock Bypass Reset (byte mode)



5.7 Secured Silicon Sector Flash Memory Region

The Secured Silicon Sector provides an extra Flash memory region that enables permanent part identification through an Electronic Serial Number (ESN). The Secured Silicon Sector is 128 words in length. It does not care about the high address beyond 128 words, that is, the address sent every time is always within the range of 128 words. The Secured Silicon Sector Protection Bit (DQ0 at Lock Register) and Secured Silicon Sector Indicator Bit (DQ7, at Autoselect address 03h) are used to indicate whether or not the Secured Silicon Sector is locked when shipped from the factory.

Please note the following general conditions:

1. On power-up, or following a hardware reset, the device reverts to sending instructions to the normal address space (memory array).
2. Once the Secured Silicon Sector Entry Instruction is issued, the Secured Silicon Sector Exit instruction must be issued to exit Secured Silicon Sector Mode.
3. The Secured Silicon Sector mode is not accessible when the device is executing an Embedded Program or Embedded Erase algorithm.
4. The accelerated Program and unlock bypass modes are not available when the Secured Silicon Sector is enabled.

Table 7. Secured Silicon Sector Addresses

Secured Silicon Sector Address Range	Customer Lockable	Factory Locked	
		ESN Factory Locked	ExpressFlash Factory Locked
000000h–000007h	Determined by customer	ESN	ESN or determined by customer
000008h–00007Fh		Unavailable	Determined by customer

5.7.1 Factory Locked Secured Silicon Sector

The Factory Locked Secured Silicon Sector is always protected when shipped from the factory and has the Secured Silicon Sector Indicator Bit (DQ7) permanently set to a “1”. This prevents cloning of a factory locked part and ensures the security of the ESN and customer code once the product is shipped to the field. The Factory Locked Secured Silicon Sector includes ESN Factory Locked and ExpressFlash Factory Locked.

These devices are available pre-programmed with one of the following:

1. A random, 8 Word secure ESN only within the Secured Silicon Sector (at addresses 000000H - 000007H) in ESN Factory Locked mode.
2. Both a random, secure ESN and customer code in ExpressFlash Factory Locked mode.

Customers may opt to have their code programmed through the programming services, which program the customer's code, with or without the random ESN. The devices are then shipped from the factory with the Secured Silicon Sector permanently locked. Contact your local representative for details on using programming services.

5.7.2 Customer Lockable Secured Silicon Sector

The Customer Lockable Secured Silicon Sector is always shipped unprotected (DQ7 set to“0”), allowing customers to utilize that sector in any manner they choose. If the security feature is not required, the Secured Silicon Sector can be treated as an additional Flash memory space.

Please note the following:

1. The Secured Silicon Sector can be read any number of times, but can be locked only once, and each bit can only be programmed from “1” to “0”.
2. The Secured Silicon Sector can be locked through the Secured Silicon Sector Protection Bit (DQ0 at Lock Register) is permanently set to “0”.
3. The Secured Silicon Sector lock must be used with caution as once locked, there is no procedure available for unlocking the Secured Silicon Sector area, the Secured Silicon Sector area will always be protected, none of the bits in the Secured Silicon Sector memory space can be modified in any way.
4. The accelerated programming (ACC) and unlock bypass modes are not available when the Secured Silicon Sector is enabled.
5. The system must write the Exit Secured Silicon Sector Region instruction sequence which returns the device to the memory array at sector 0.

5.7.3 Secured Silicon Sector Entry/Exit Instruction Sequences

The system can access the Secured Silicon Sector region by issuing the three-cycle Enter Secured Silicon Sector instruction sequence. The device continues to access the Secured Silicon Sector region until the system issues the four-cycle Exit Secured Silicon Sector instruction sequence.

The Secured Silicon Sector Entry Instruction allows the following instructions to be executed:

1. Read customer and factory Secured Silicon areas.

2. Program the customer Secured Silicon Sector.

After the system has written the Secured Silicon Sector Entry instruction sequence, it may read the Secured Silicon Sector by using the addresses normally occupied by sector SA0 within the memory array. This mode of operation continues until the system issues the Secured Silicon Sector Exit instruction sequence, or until power is removed from the device.

Secured Silicon Sector Entry

Cycle	Operation	Byte Address	Word Address	Data
Unlock Cycle 1	Write	AAAh	555h	00AAh
Unlock Cycle 2	Write	555h	2AAh	0055h
Entry Cycle	Write	AAAh	555h	0088h

Figure 32. Secured Silicon Sector Entry (word mode)

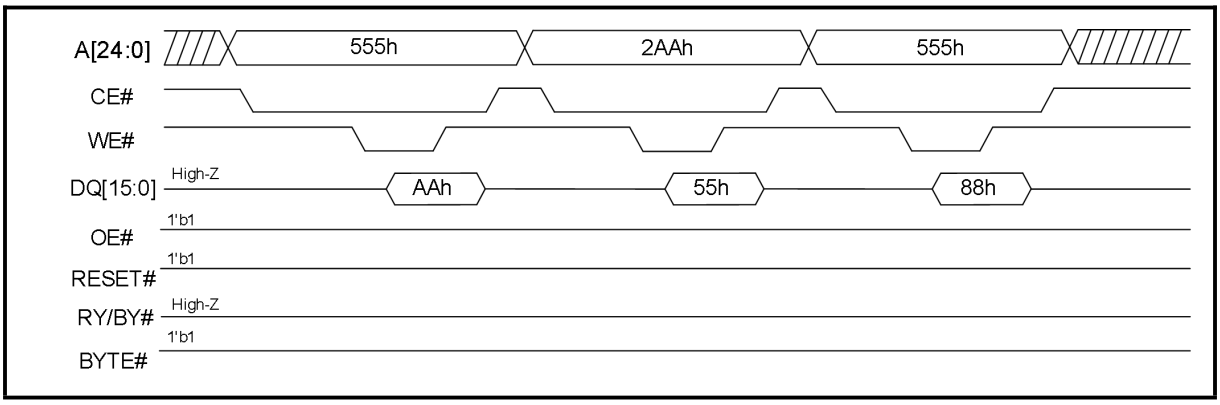
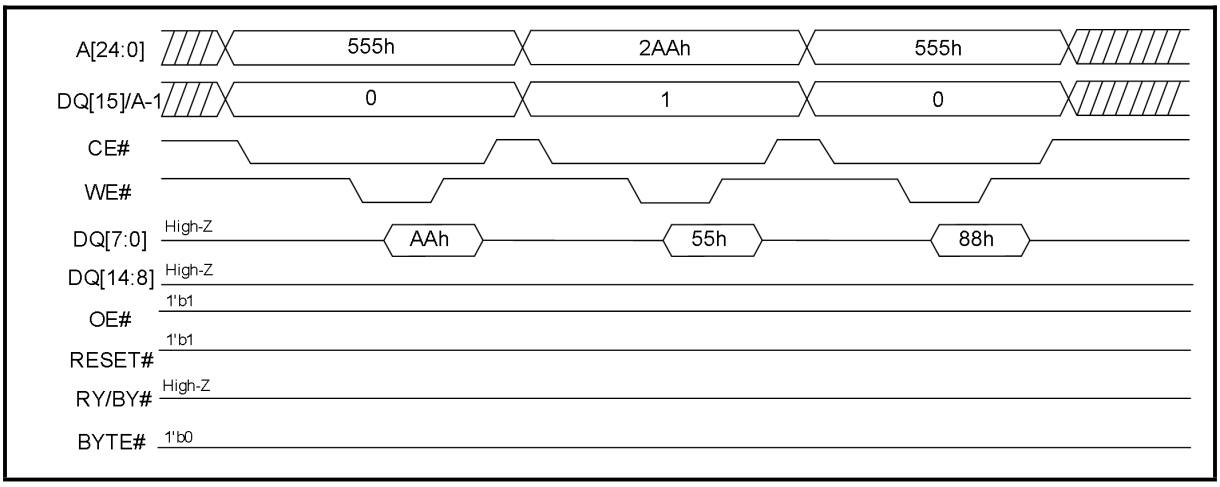


Figure 33. Secured Silicon Sector Entry (byte mode)



Secured Silicon Sector Exit

Cycle	Operation	Byte Address	Word Address	Data
Unlock Cycle 1	Write	AAAh	555h	00AAh
Unlock Cycle 2	Write	555h	2AAh	0055h
Exit Cycle 3	Write	AAAh	555h	0090h
Exit Cycle 4	Write	XXXh	XXXh	0000h

Figure 34. Secured Silicon Sector Exit (word mode)

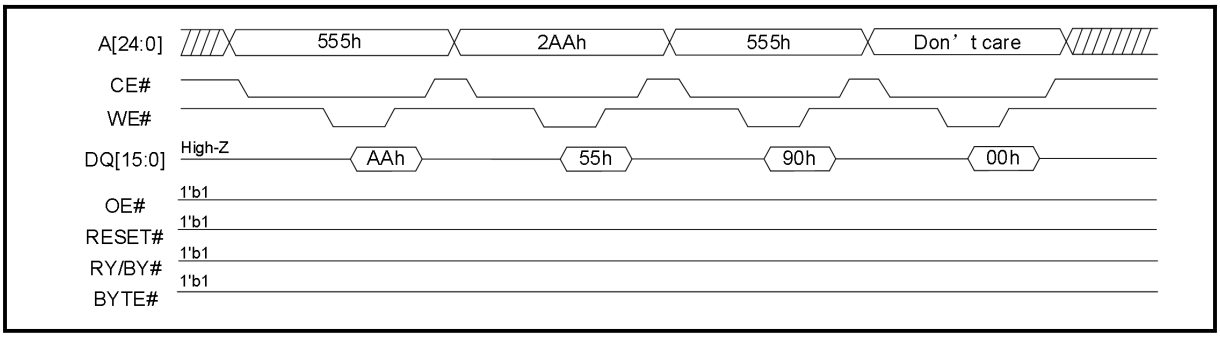
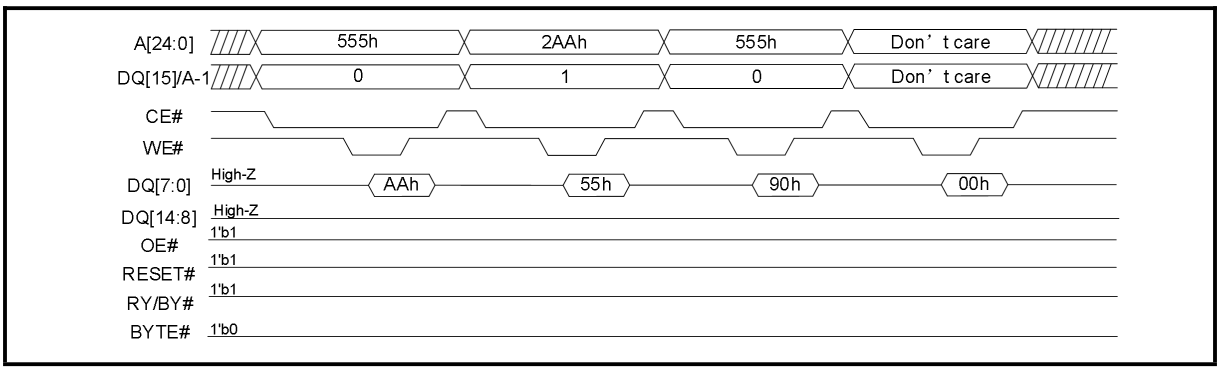


Figure 35. Secured Silicon Sector Exit (byte mode)



5.8 Autoselect

The Autoselect mode provides manufacturer ID, Device identification, and sector protection information, through identifier codes output from the internal register (separate from the memory array) on DQ7-DQ0. This mode is primarily intended for programming equipment to automatically match a device to be programmed with its corresponding programming algorithm. The Autoselect codes can also be accessed in-system. There are two methods to access autoselect codes.

When using programming equipment, the autoselect mode requires on address pin A9. Address pins must be as shown in table.

1. To access Autoselect mode without using high voltage on A9, the host system must issue the Autoselect instruction.
2. The Autoselect instruction sequence may be written to an address within a sector that is either in the read or erase-suspend-read mode.
3. The Autoselect instruction may not be written while the device is actively programming or erasing.
4. The system must write the reset instruction to return to the read mode (or erase-suspend-read mode if the sector was previously in Erase Suspend).
5. It is recommended that A9 apply V_{ID} after power-up sequence is completed. In addition, it is recommended that A9 apply from V_{ID} to V_{IH}/V_{IL} before power-down the V_{CC}/V_{IO}.
6. See ***Instruction Definitions*** for instruction sequence details.
7. When verifying sector protection, the sector address must appear on the appropriate highest order address bits. The remaining address bits are don't care. When all necessary bits have been set as required, the programming equipment may then read the corresponding identifier code on DQ15-DQ0. The Autoselect codes can also be accessed in-system through the instruction register.

5.8.1 Autoselect Codes, (High Voltage Method)

Description	CE#	OE#	WE#	Amax to A16	A14 to A1 0	A9	A8 to A7	A6	A5 to A4	A3 to A2	A1	A0	DQ8 to DQ15		DQ7 to DQ0
													BYTE #= V_{IH}	BYTE # = V_{IL}	
Manufacturer ID:	L	L	H	X	X	V_{ID}	X	L	X	L	L	L	00	X	01h
Device ID BY29G512FS Cycle 1	L	L	H	X	X	V_{ID}	X	L	X	L	L	H	22	X	7Eh
Device ID BY29G512FS Cycle 2										H	H	L	22	X	23h
Device ID BY29G512FS Cycle 3										H	H	H	22	X	01h
Secor Group Protection Verification	L	L	H	SA	X	V_{ID}	X	L	X	L	H	L	X	X	01h (protected), 00h (unprotected)
sector															
Secured Silicon Sector Indicator Bit (DQ7), WP# protects lowest ad dress sector	L	L	H	X	X	V_{ID}	X	L	X	L	H	H	X	X	89h (factory locked), 09h (not factory locked)

Legend
L = Logic Low = V_{IL}, H = Logic High = V_{IH}, SA = Sector Address, X = Don't care. V_{ID} = 11.5V to 12.5V

5.8.2 Autoselect Addresses in System

Description	Address	Read Data (word/byte mode)
Manufacturer ID	00h	xx01h/1h
Device ID, Word 1	01h	227Eh/7Eh
Device ID, Word 2	0Eh	2223h/23h (BY29G512FS)
Device ID, Word 3	0Fh	2201h/01h
Secure Device Verify	03h	XX09h/09h = Not Factory Locked. XX89h/89h = Factory Locked.
Sector Protect Verify	(SA) + 02h	xx01h/01h = Locked, xx00h/00h = Unlocked

5.8.3 Autoselect Entry in System

Cycle	Operation	Byte Address	Word Address	Data
Unlock Cycle 1	Write	AAAh	555h	0x00AAh
Unlock Cycle 2	Write	555h	2AAh	0x0055h
Autoselect Instruction	Write	AAAh	555h	0x0090h

5.8.4 Autoselect Exit

Cycle	Operation	Byte Address	Word Address	Data
Autoselect Exit Instruction	Write	XXXh	XXXh	0x00F0h

Note
1. Any offset within the device works.

Figure 36. Autoselect Entry (word mode)

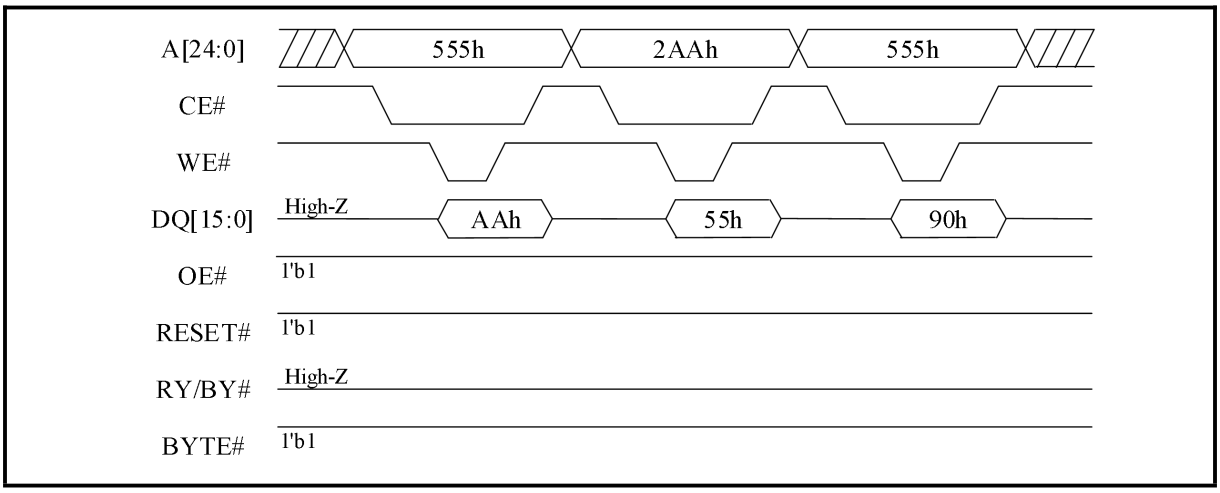


Figure 37. Autoselect Entry (byte mode)

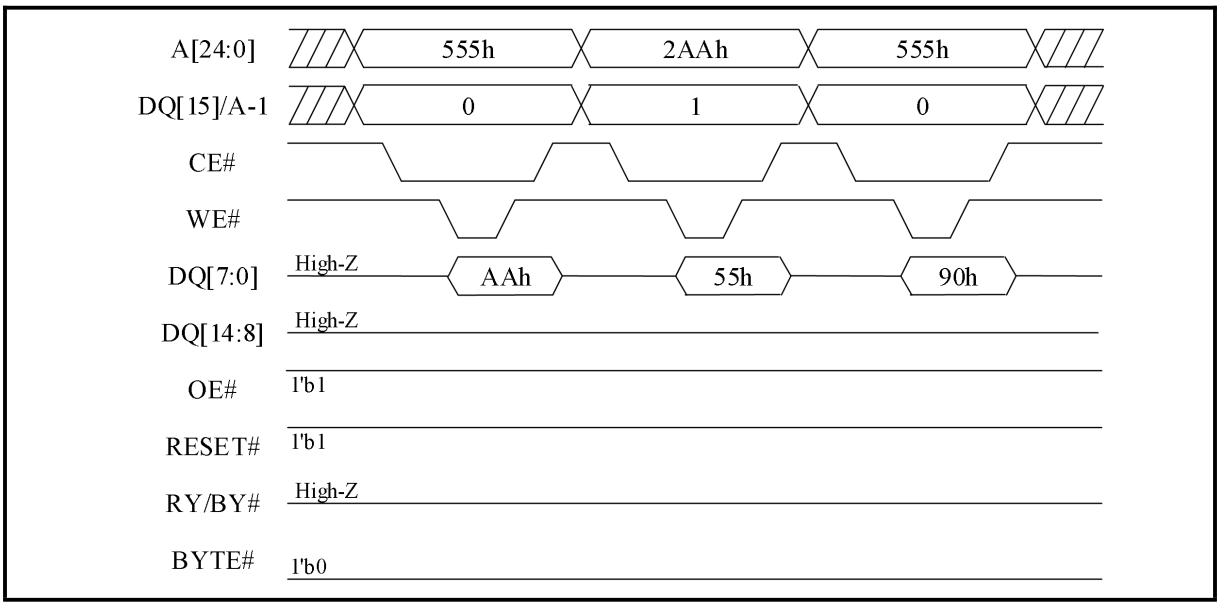


Figure 38. Autoselect Exit (word mode)

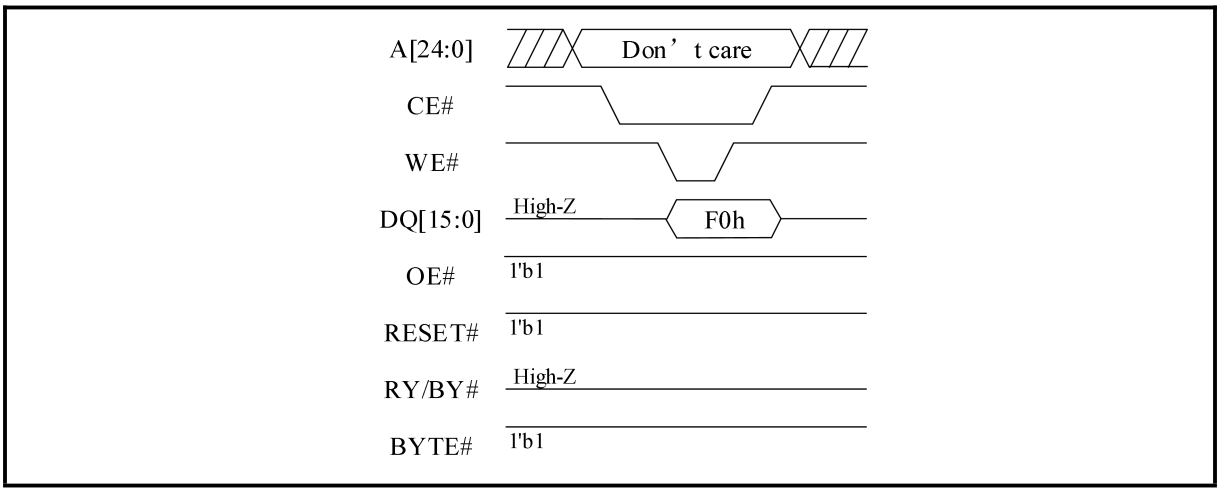
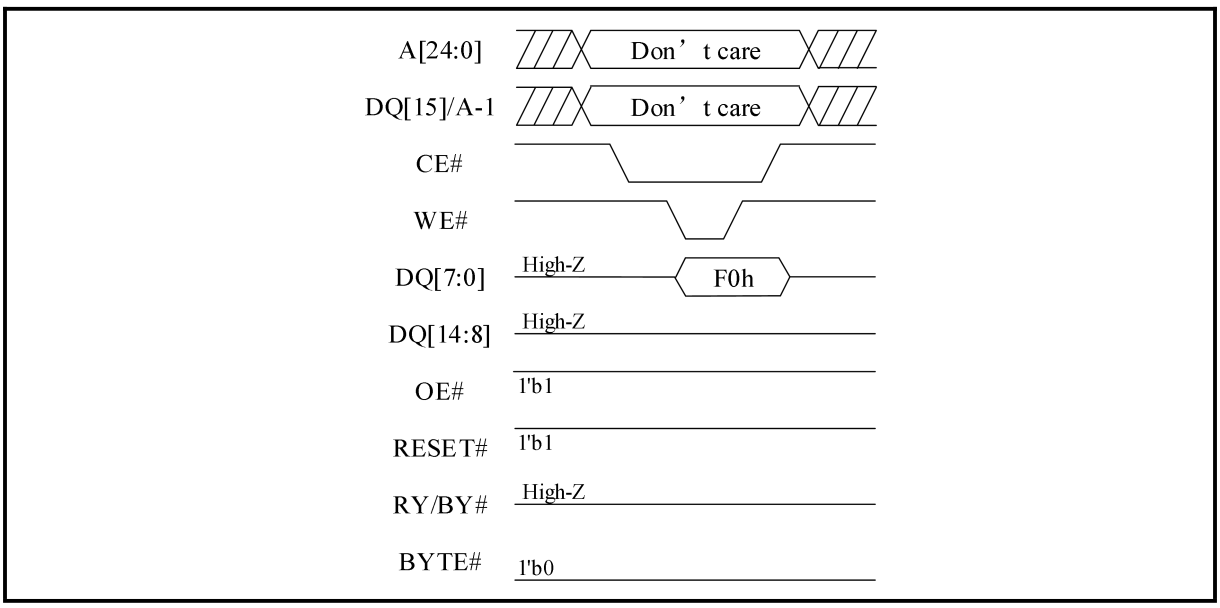


Figure 39. Autoselect Exit (byte mode)



5.9 Reset Operations

5.9.1 Hardware Reset

The RESET# input provides a hardware method of resetting the device to reading array data. When RESET# is driven low for at least a period of t_{RP} (RESET# Pulse Width), the device immediately terminates any operation in progress, tristates all outputs, resets the configuration register, and ignores all read/write instructions for the duration of the RESET# pulse. The device also resets the internal state machine to reading array data.

To ensure data integrity Program/Erase operations that were interrupted should be reinitiated once the device is ready to accept another instruction sequence.

When RESET# is held at V_{SS}, the device draws V_{CC} reset current (I_{CC5}). If RESET# is held at V_{IL}, but not at VSS, the standby current is greater. RESET# may be tied to the system reset circuitry which enables the system to read the boot-up firmware from the Flash memory upon a system reset. See ***Figure 100*** and ***Figure 101*** for timing diagrams.

5.9.2 Software Reset

Software reset is part of the instruction set that also returns the device to array read mode and must be used for the following conditions:

1. Exit CFI/Autoselect mode, return to read mode or suspend-read mode.
2. Exit the erase/program error condition (DQ5=1), but software reset is invalid when the erase/program is executed normally.

Software Functions and Sample Code

Reset

Cycle	Operation	Byte Address	Word Address	Data
Reset Instruction	Write	xxxh	xxxh	00F0h

Figure 40. Reset (word mode)

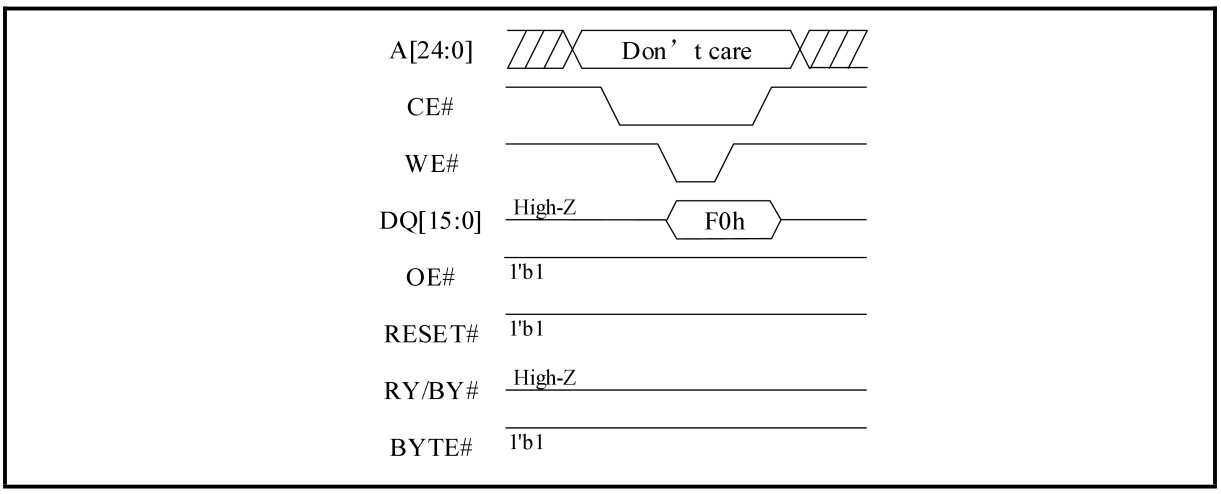
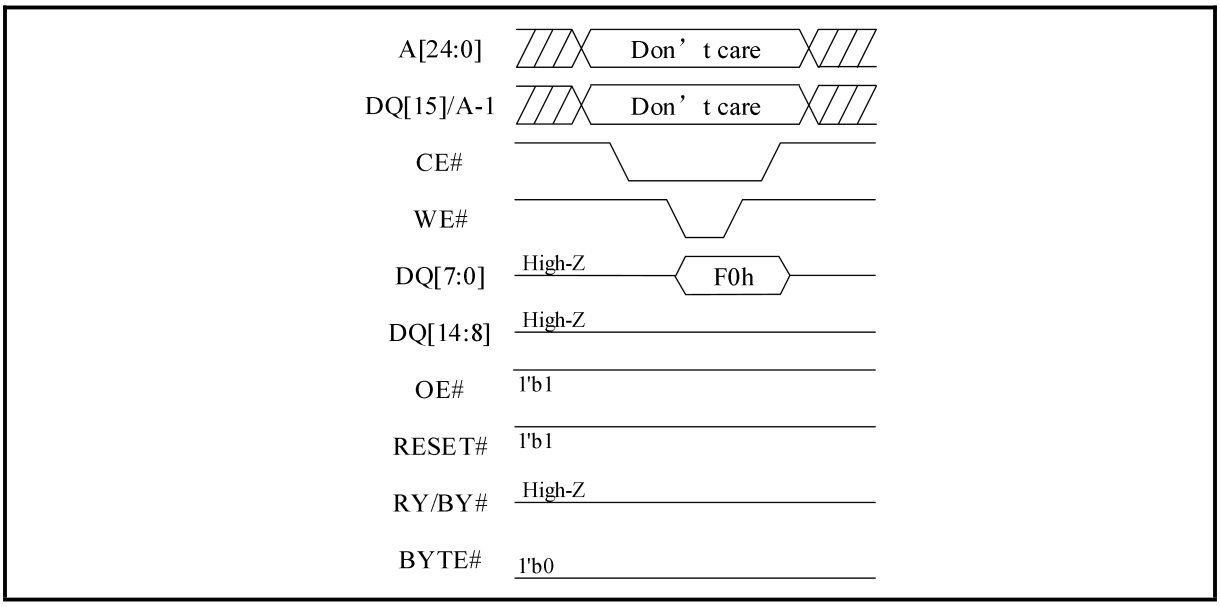


Figure 41. Reset (byte mode)



5.10 Common Flash Memory Interface

The Common Flash Interface (CFI) specification outlines device and host system software interrogation handshake, which allows specific vendor-specified software algorithms to be used for entire families of devices. Software support can then be device- independent, JEDEC ID-independent, and forward- and back-ward-compatible for the specified flash device families. Flash vendors can standardize their existing interfaces for long-term compatibility.

This device enters the CFI Query mode when the system writes the CFI Query instruction, 98h, to address 55h any time the device is ready to read array data. The system can read CFI information at the addresses given in ***Appendix***. All reads outside of the CFI address range, returns non-valid data. Reads from other sectors are allowed, writes are not. To terminate reading CFI data, the system must write the reset instruction.

The system can also write the CFI query instruction when the device is in the autoselect mode. The device enters the CFI query mode, and the system can read CFI data at the addresses given in ***Appendix***. The system must write the reset instruction to return the device to reading array data.

Figure 42. CFI query (word mode)

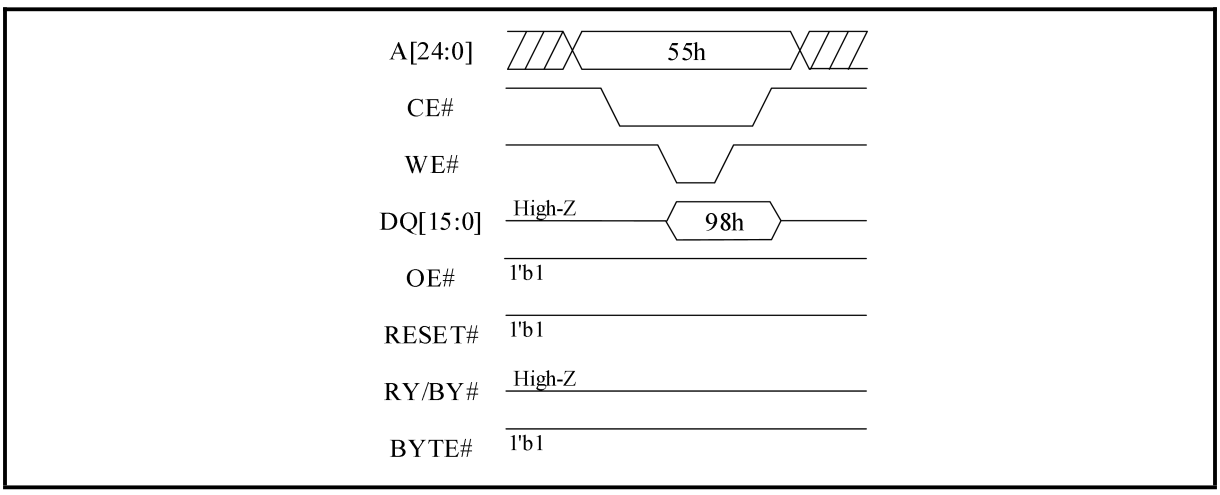
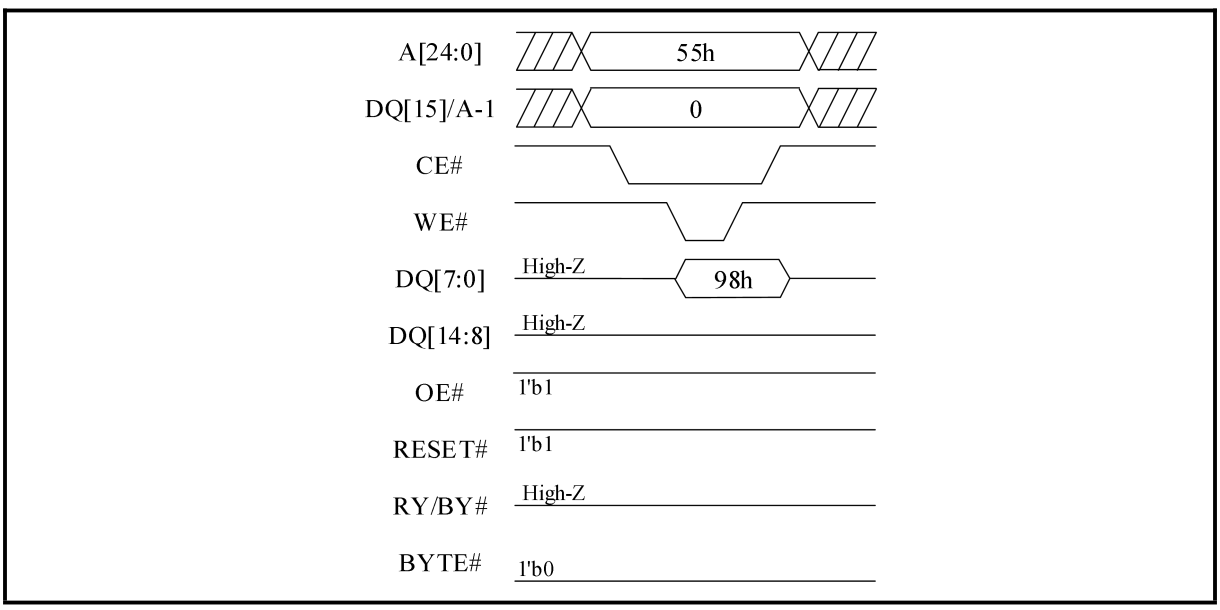


Figure 43. CFI query (byte mode)

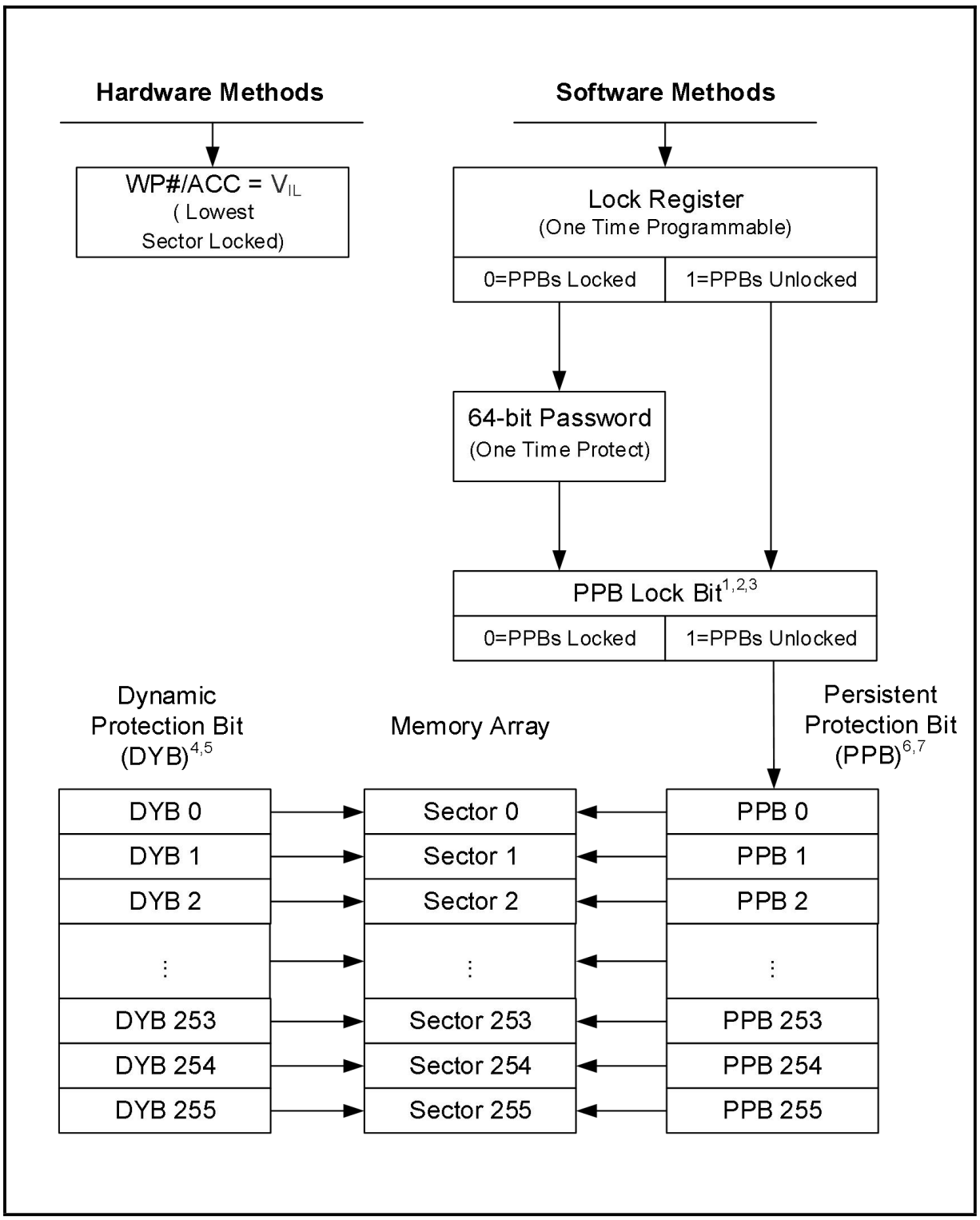


5.11 Advanced Sector Protection/Unprotection

The Advanced Sector Protection/Unprotection feature disables or enables programming or erase operations in any or all sectors and can be implemented through software and/or hardware methods, which are independent of each other. The device offers the main type of data protection at the sector level via hardware control: When WP#/ACC is at V_{IL}, the lowest sector is locked (device specific). This section describes the various methods of protecting data stored in the memory array.

An overview of these methods in shown in ***Figure 44***.

Figure 44. Advanced Sector Protection/Unptection



Note

1. *PPB Lock Bit is volatile, in Persistent Protection Mode, defaults to "1" and in Password Protection Mode, defaults to "0".*
2. *PPB Lock Bit Programming to "0" locks all PPBs to their current state.*
3. *PPB Lock Bit once programmed to "0" requires hardware reset, power-up or a password to "1".*
4. *DYB: 0 = Sector Protected, 1 = Sector Unprotected.*
5. *DYB is Volatile Bit: the user can select the default value after power-up before shipping from the factory.*
6. *PPB: 0 = Sector Protected, 1 = Sector Unprotected.*
7. *PPBs programmed individually, but cleared collectively.*

Advanced Sector Protection Software Examples

Table 8. Sector Protection: DYB, PPB and PPB Lock Bit Combinations

Sector PPB 0 = protected 1 = un protected	Sector DYB 0 = protected 1 = un protected	Sector Protection Status
0	0	Protected through PPB
0	1	Protected through PPB
1	0	Protected through DYB
1	1	Unprotected

5.11.1 Lock Register

As shipped from the factory, all devices default to the persistent mode when power is applied, and all sectors are unprotected, unless otherwise chosen through the DYB ordering option. The device programmer or host system must then choose which sector protection method to use.
Programming (setting to "0") any one of the following two one-time programmable, non-volatile bits locks the part permanently in that mode:

1. Lock Register Secured Silicon Sector Protection Bit (DQ0)
2. Lock Register Persistent Protection Mode Lock Bit (DQ1)
3. Lock Register Password Protection Mode Lock Bit (DQ2)

Table 9. Lock Register

DQ15-3	DQ2	DQ1	DQ0
Don't Care	Password Protection Mode Lock Bit	Persistent Protection Mode Lock Bit	Secured Silicon Sector Protection Bit
×	Default =1	Default =1	Factory Locked Secured Silicon Sector: Default = 0; Customer Lockable Secured Silicon Sector: Default = 1
OTP	OTP	OTP	OTP

Note

1. *If the password mode is chosen, the password must be programmed before setting the corresponding lock register bit.*
2. *If both lock bits are selected to be programmed (to zeros) at the same time, the operation aborts, the device then returns to the read mode.*
3. *Once the Password Mode Lock Bit is programmed, the Persistent Mode Lock Bit is permanently disabled, and no changes to the protection scheme are allowed. Similarly, if the Persistent Mode Lock Bit is programmed, the Password Mode is permanently disabled.*

After selecting a sector protection method, each sector can operate in any of the following three states:

1. Constantly locked. The selected sectors are protected and can not be reprogrammed unless PPB lock bit is cleared via a password, hardware reset, or power cycle.

2. Dynamically locked. The selected sectors are protected and can be altered via software instructions.
3. Unlocked. The sectors are unprotected and can be erased and/or programmed.

Figure 45. Lock Register Enter (word mode)

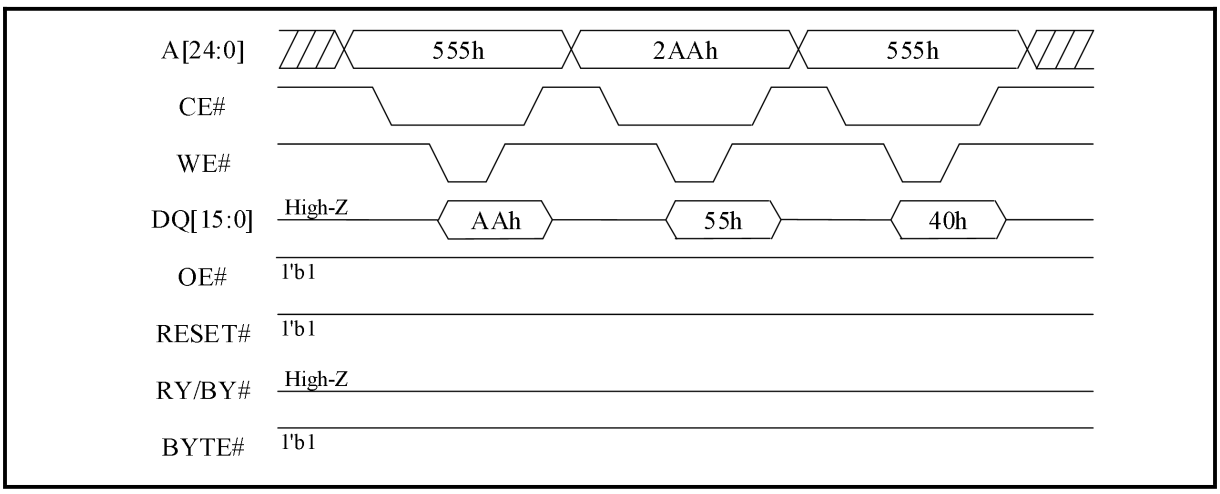


Figure 46. Lock Register Enter (byte mode)

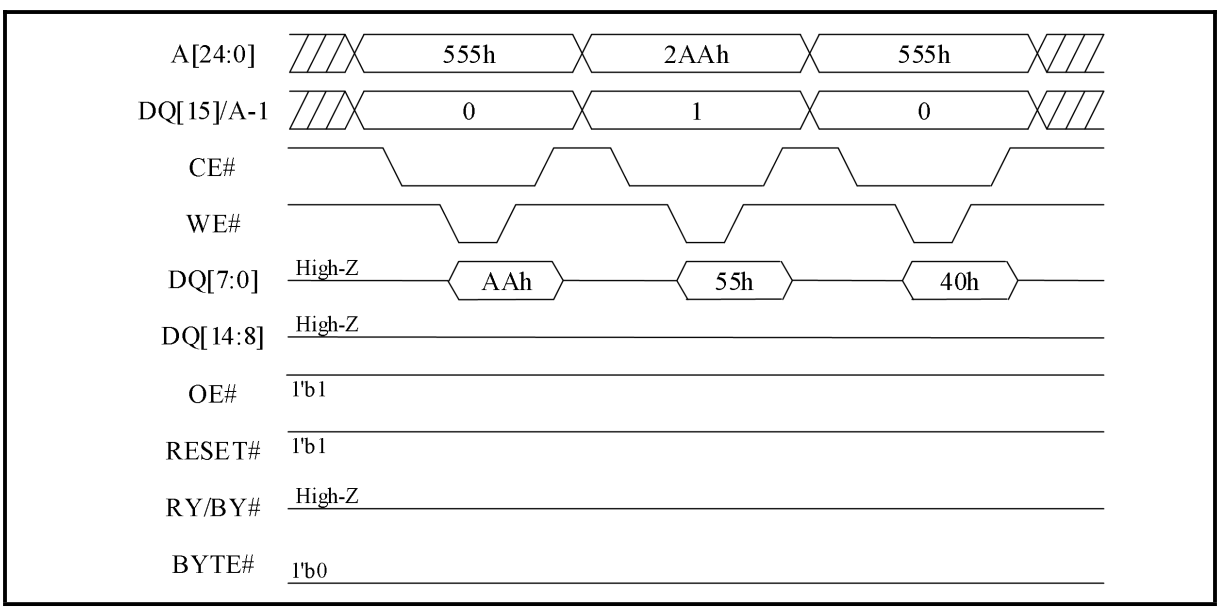


Figure 47. Lock Register Read(word mode)

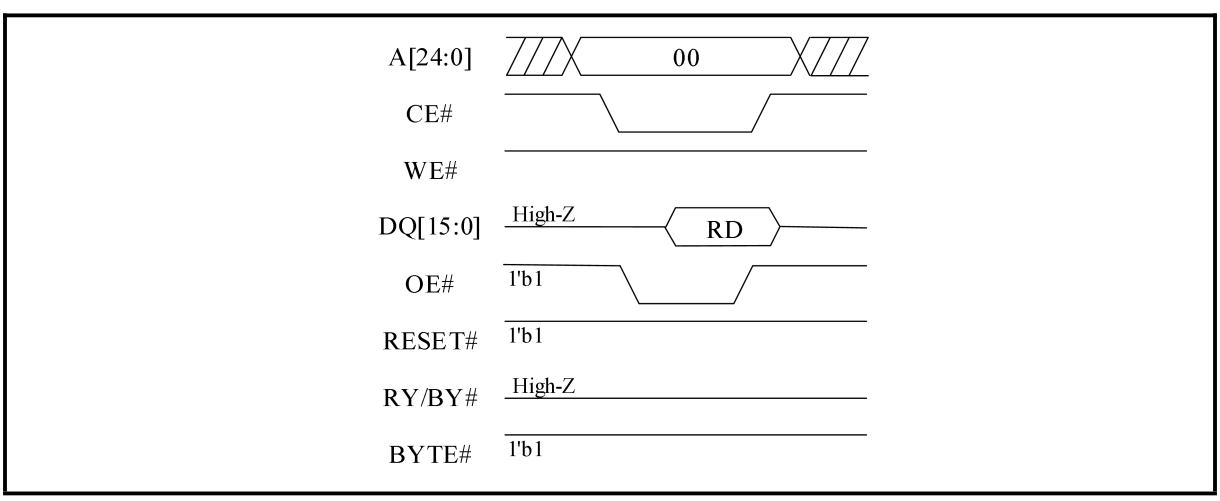


Figure 48. Lock Register Read (byte mode)

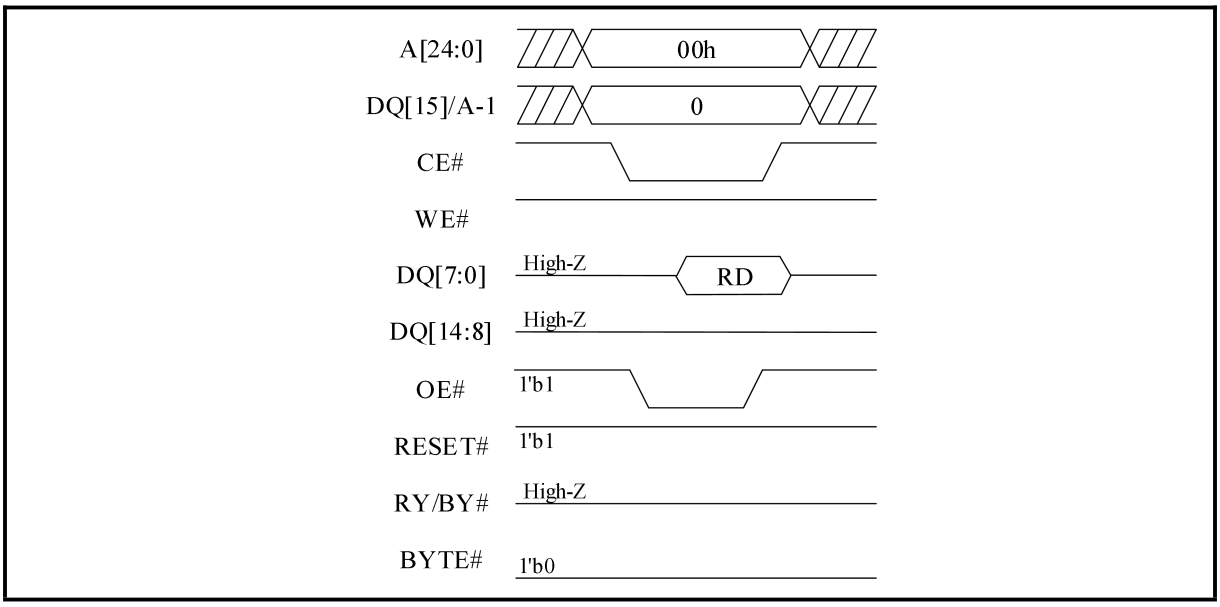


Figure 49. Lock Register Program (word mode)

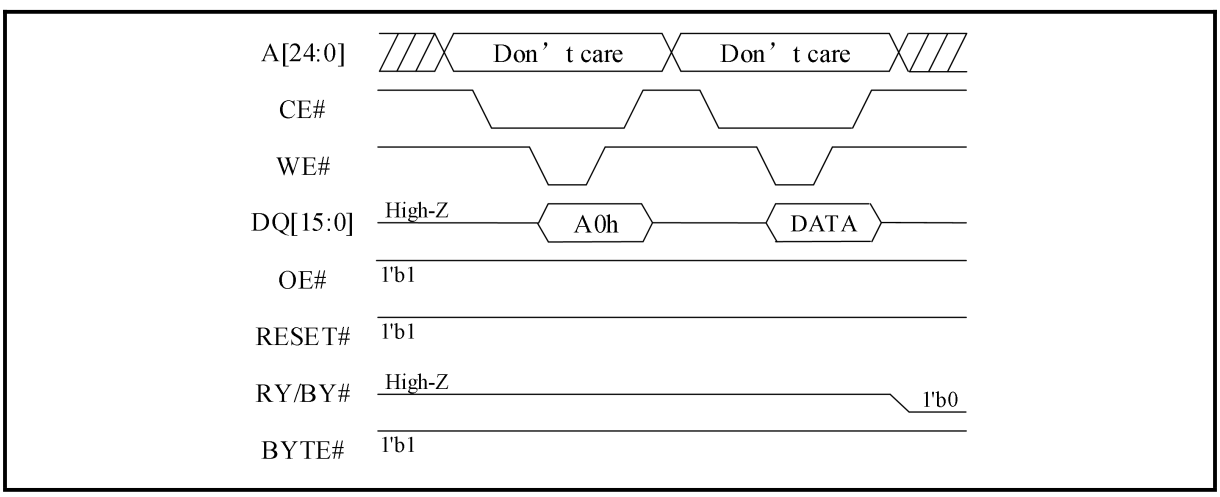


Figure 50. Lock Register Program (byte mode)

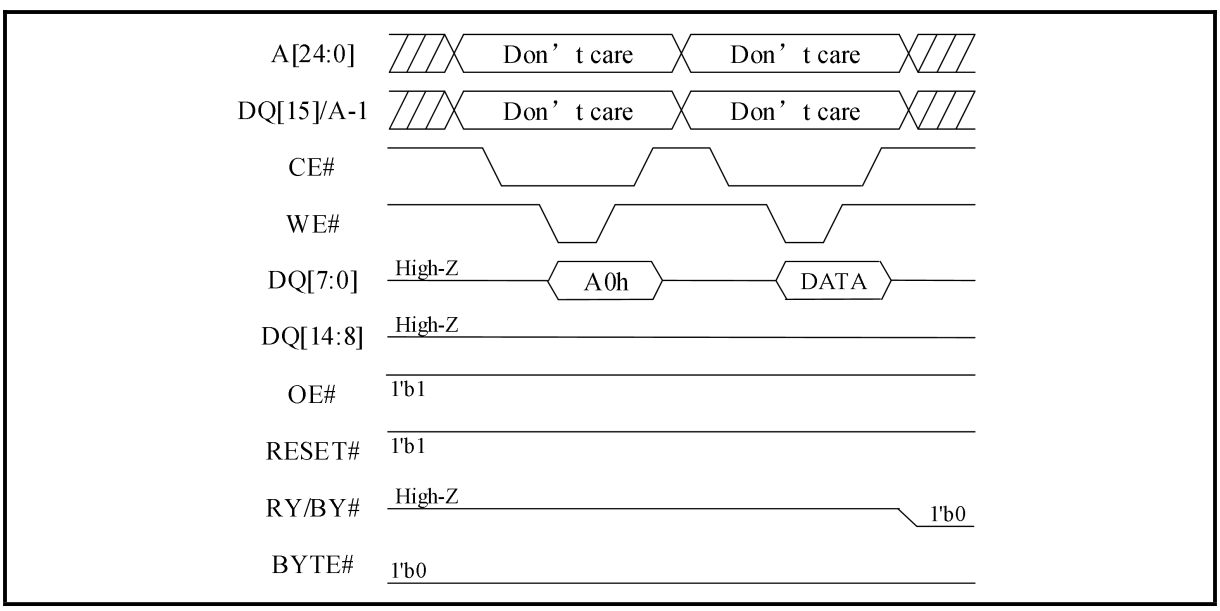


Figure 51. Lock Register Exit (word mode)

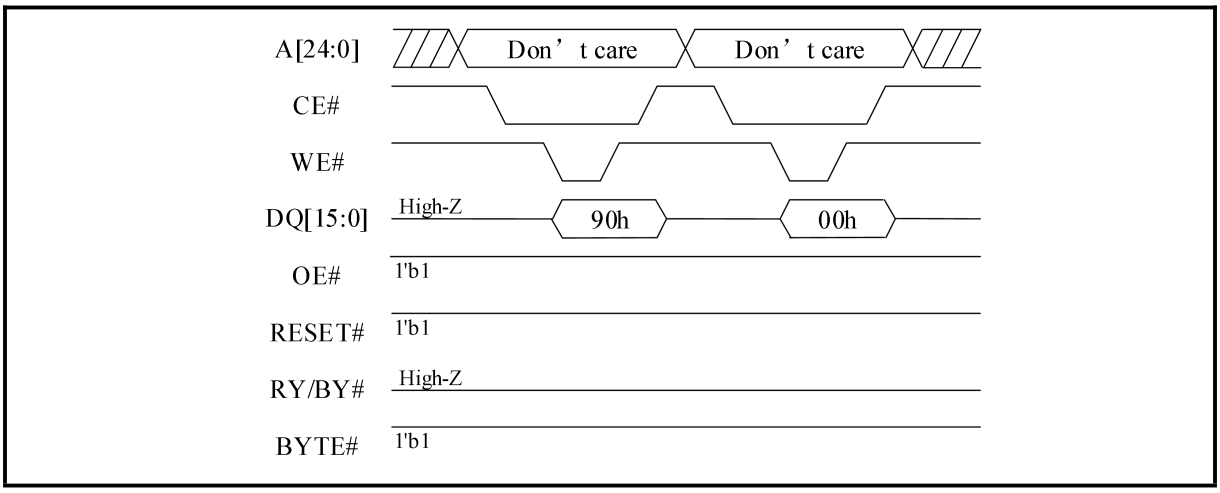
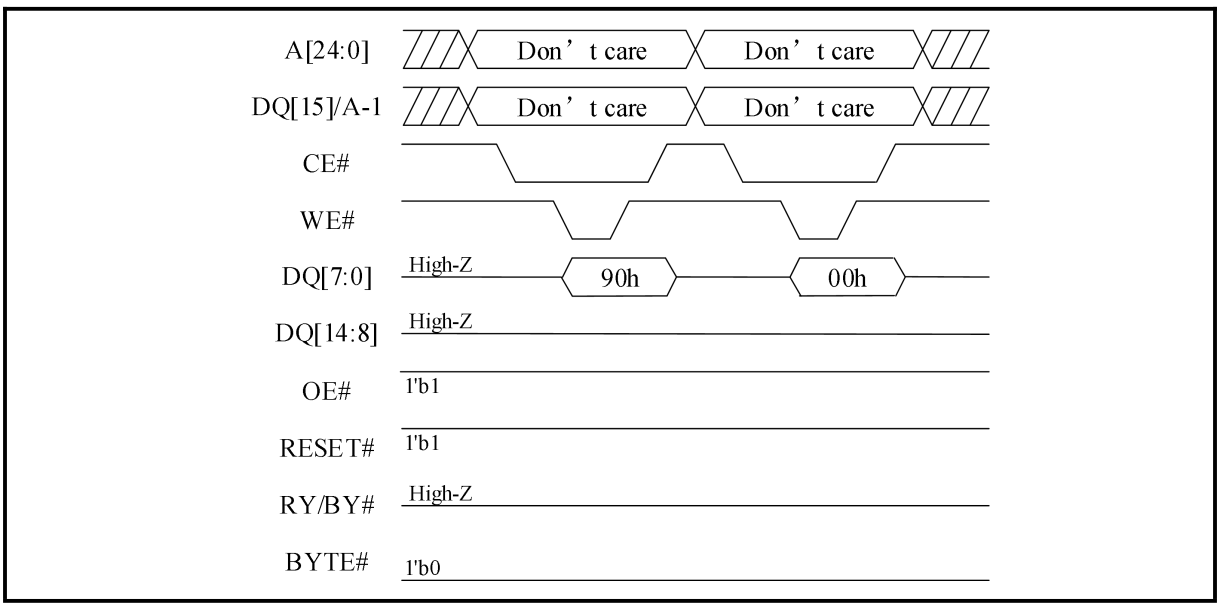


Figure 52. Lock Register Exit (byte mode)



5.11.2 Persistent Protection Bit Lock Bit

The Persistent Protection Bit Lock Bit is a global volatile bit for all sectors. When set (programmed to “0”), it locks all PPBs and when cleared (programmed to “1”), allows the PPBs to be changed. There is only one PPB Lock Bit per device.

Note

1. No software instruction sequence unlocks this bit unless the device is in the password protection mode; only a hardware reset or a power-up clears this bit.
2. The PPB Lock Bit must be set (programmed to “0”) only after all PPBs are configured to the desired settings.
3. Refer to ***Figure 51-Figure 52*** for exit instruction.

Figure 53. PPB Lock Bit Set Enter (word mode)

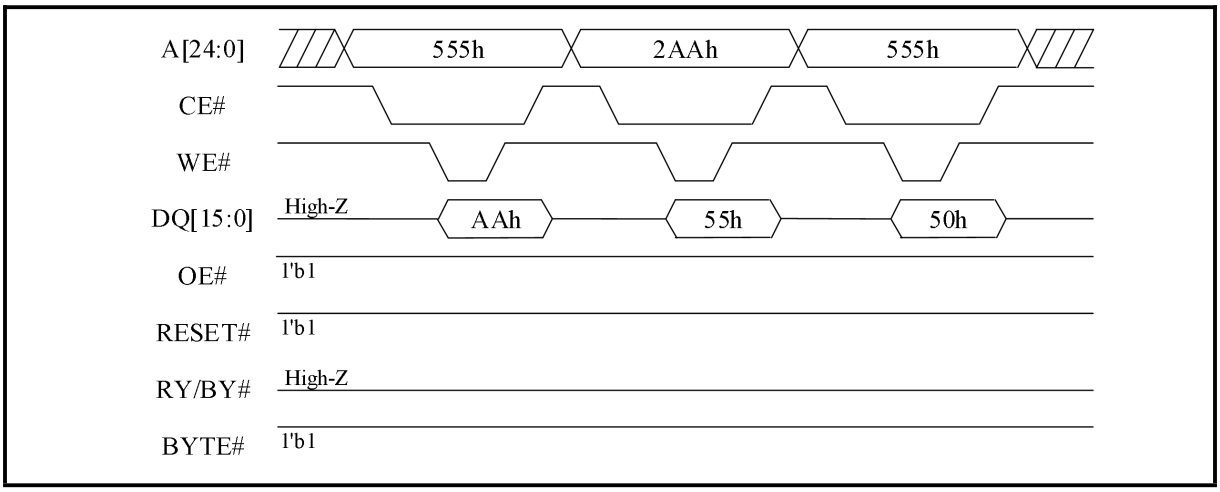


Figure 54. PPB Lock Bit Set Enter (byte mode)

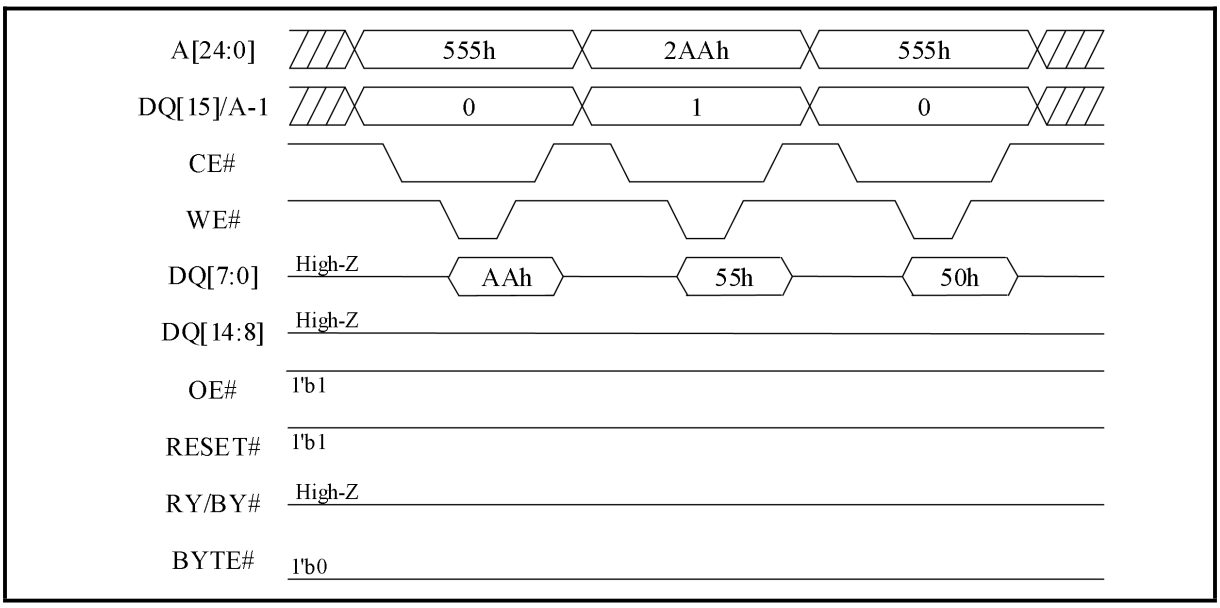


Figure 55. PPB Lock Bit Set Read (word mode)

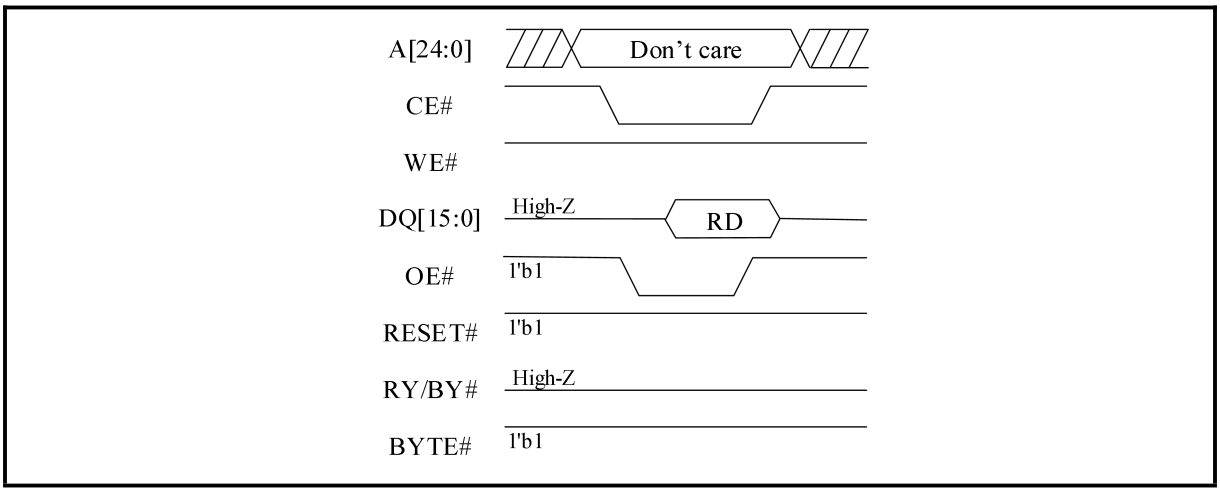


Figure 56. PPB Lock Bit Set Read (byte mode)

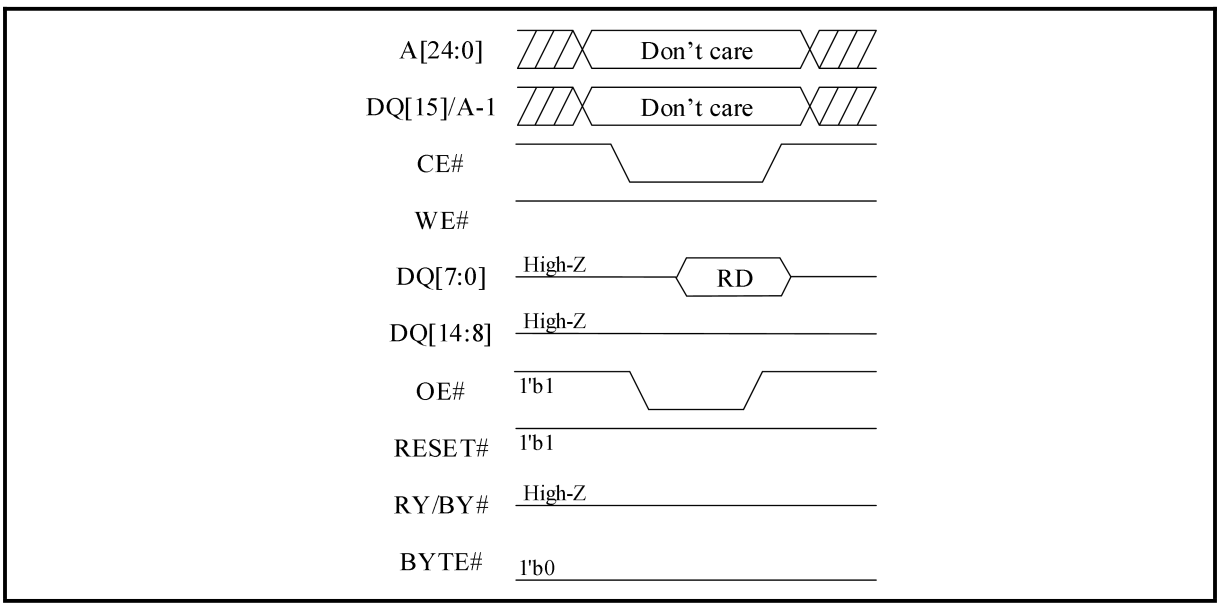


Figure 57. PPB Lock Bit Set (word mode)

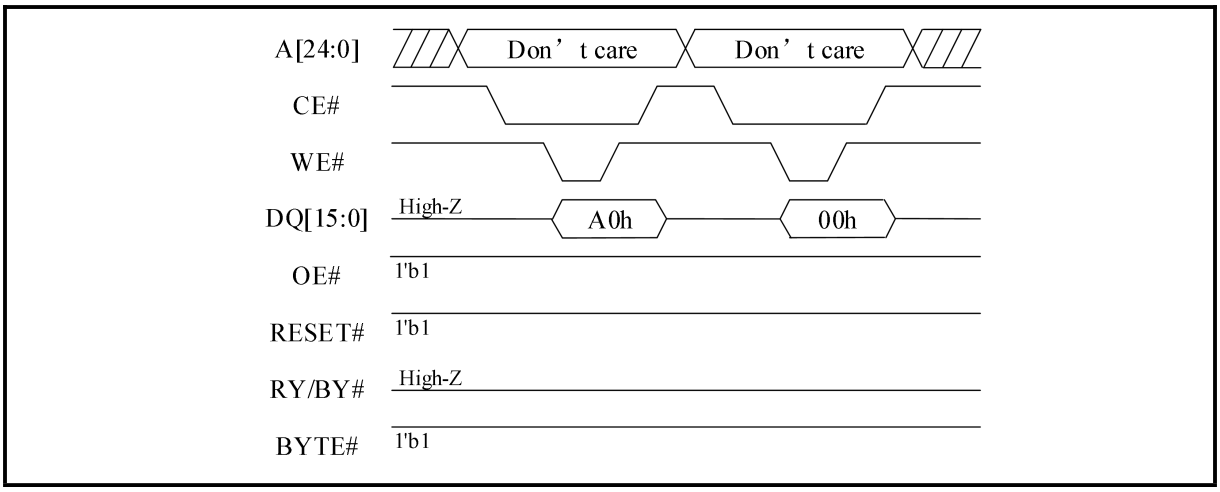
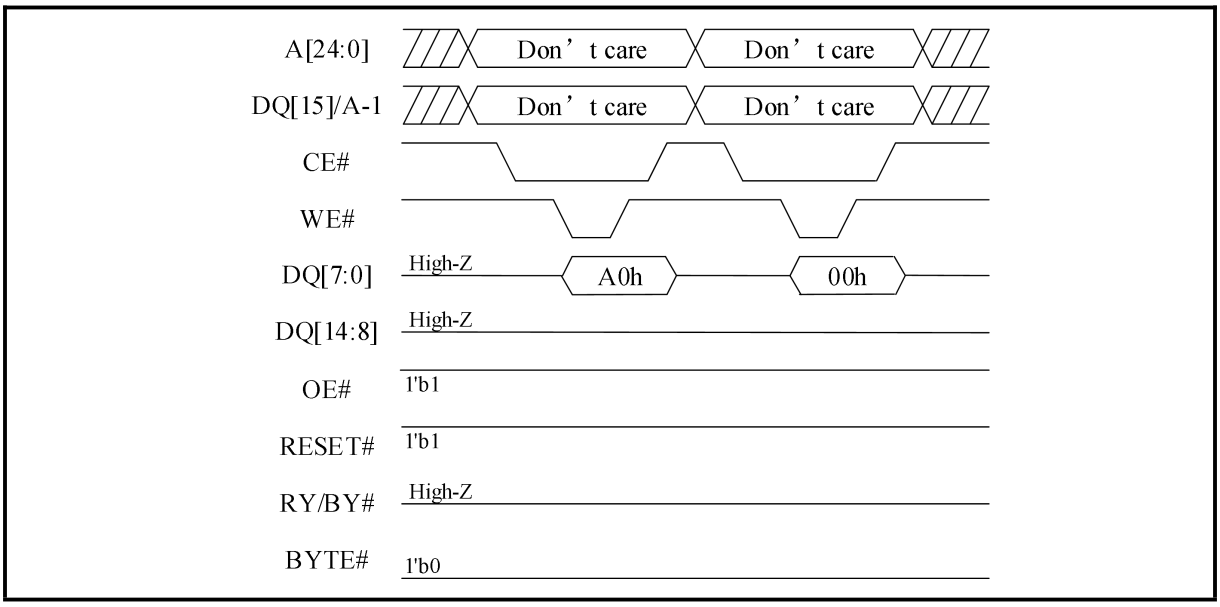


Figure 58. PPB Lock Bit Set (byte mode)



5.11.3 Persistent Protection Bits

The Persistent Protection Bits are unique and nonvolatile for each sector and have the same endurances as the Flash memory.

Note

1. Each PPB is individually programmed and all are erased in parallel.
2. Reads within that sector return the PPB status for that sector.
3. The specific sector address are written at the same time as the program instruction.
4. If the PPB Lock Bit is set, the PPB Program or erase instruction does not execute.
5. There are no means for individually erasing a specific PPB and no specific sector address is required for this operation.
6. Exit instruction must be issued after the execution which resets the device to read mode. Refer to ***Figure 51***-***Figure 52*** for exit instruction.
7. The programming state of the PPB for a given sector can be verified by writing a PPB Status Read Instruction to the device as described by the flow chart shown in ***Figure 59***.
8. PPB bits have the same function when WP#/ACC = V_{HH} as they do when ACC =V_{IH}.

Figure 59. PPB ALL ERASE Algorithm

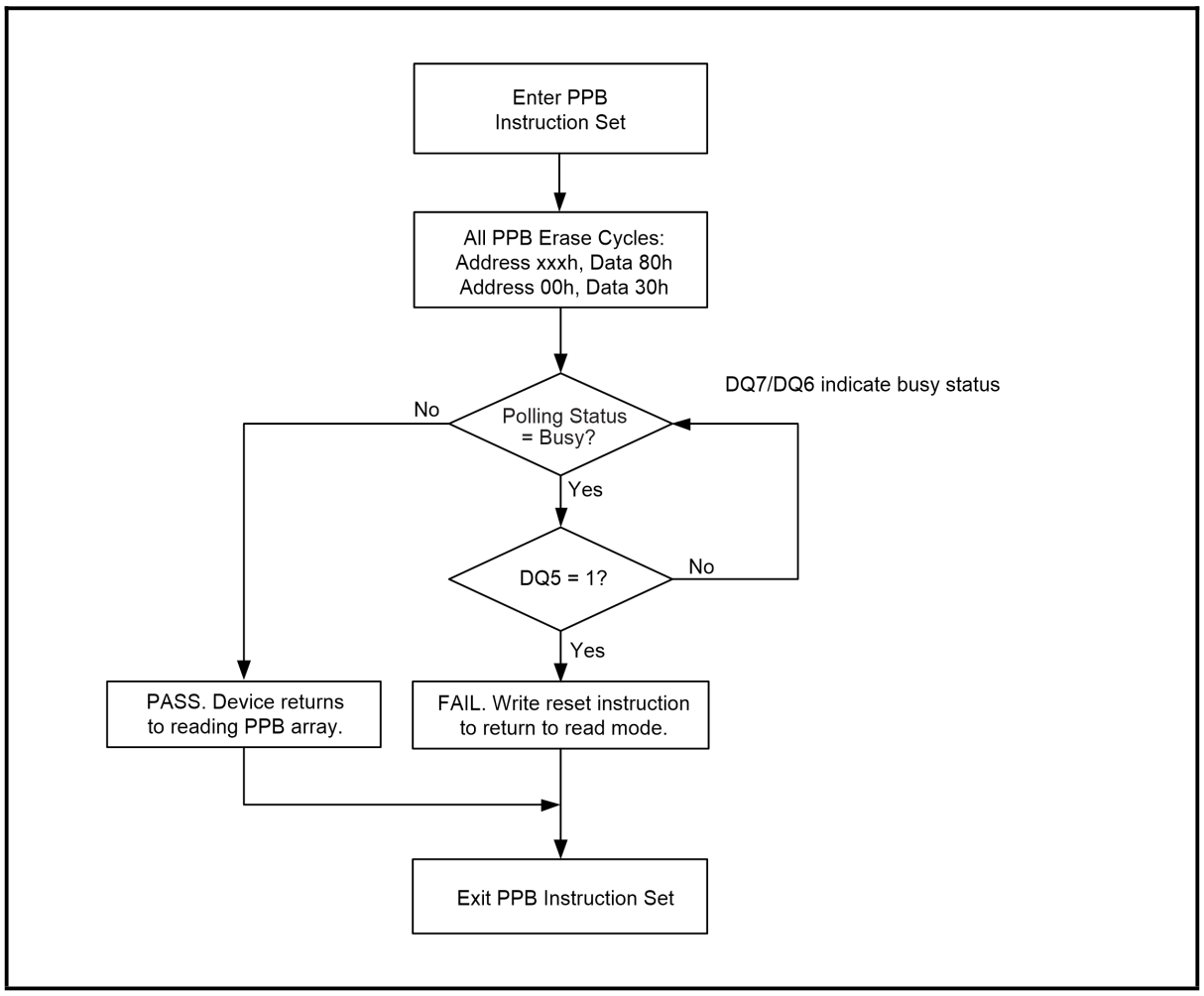


Figure 60. PPB Enter (word mode)

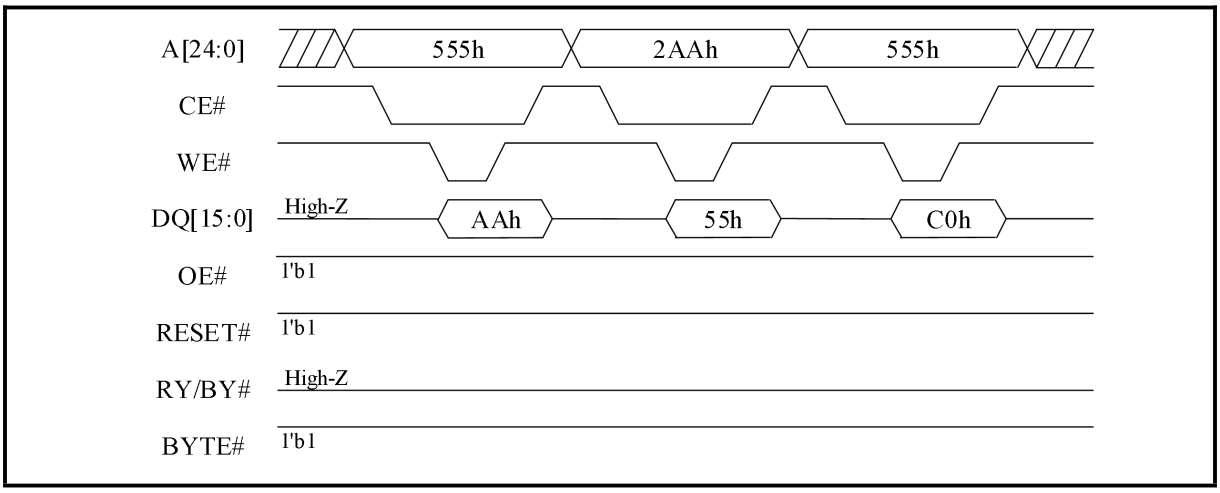


Figure 61. PPB Enter (byte mode)

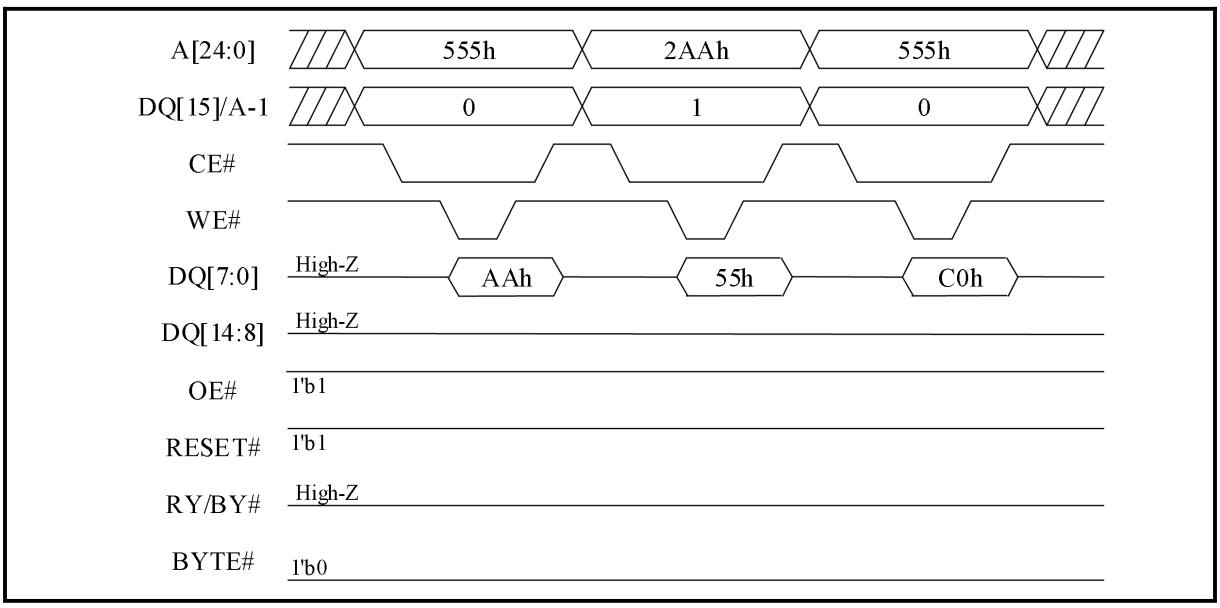


Figure 62. PPB Read(word mode)

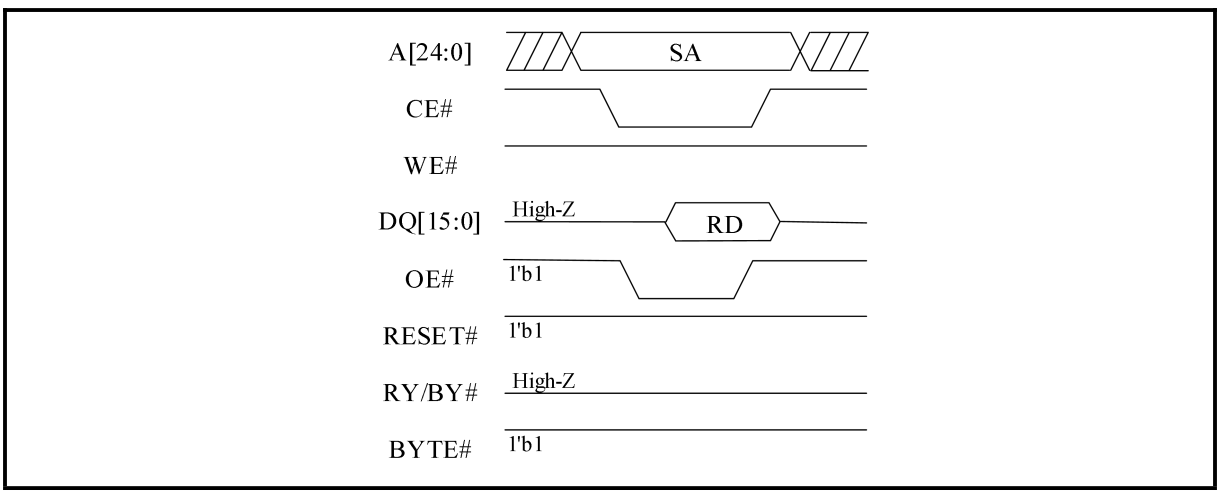


Figure 63. PPB Read (byte mode)

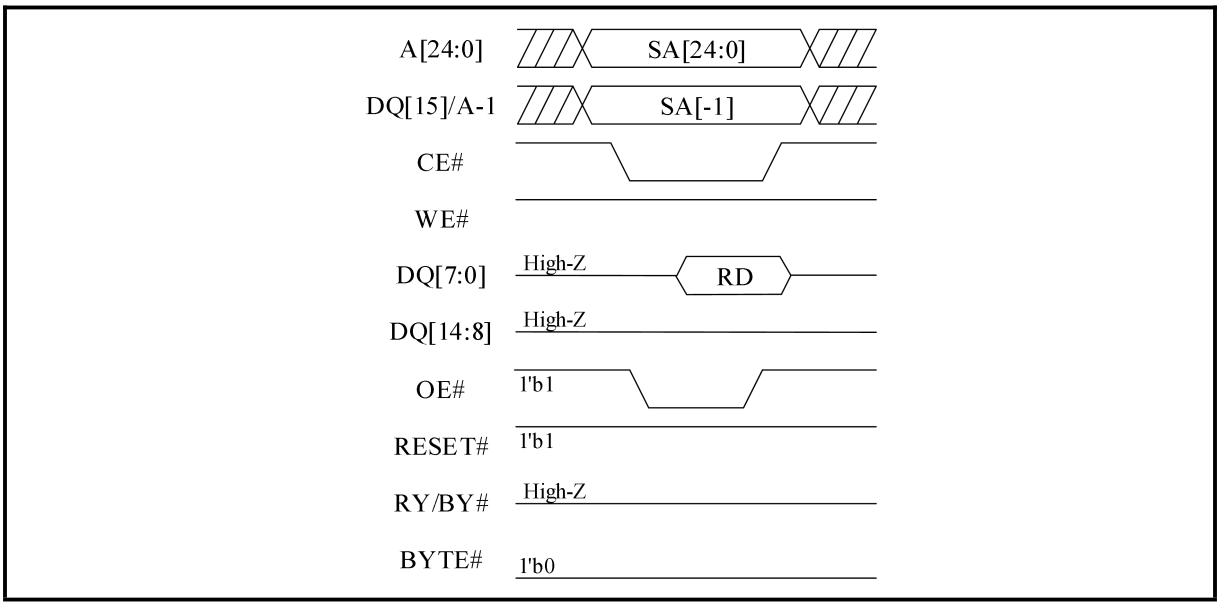


Figure 64. PPB Program (word mode)

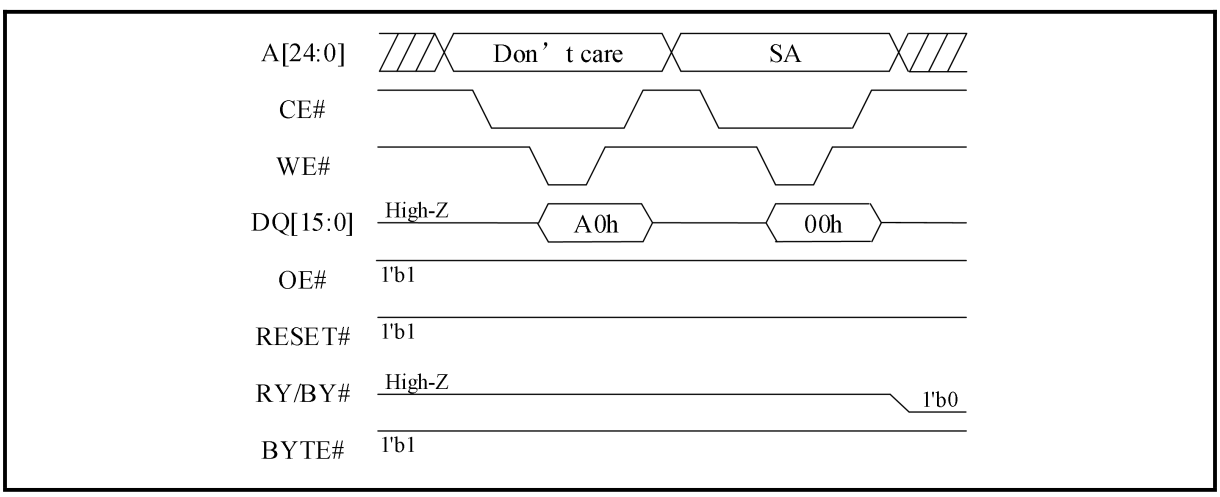


Figure 65. PPB Program (byte mode)

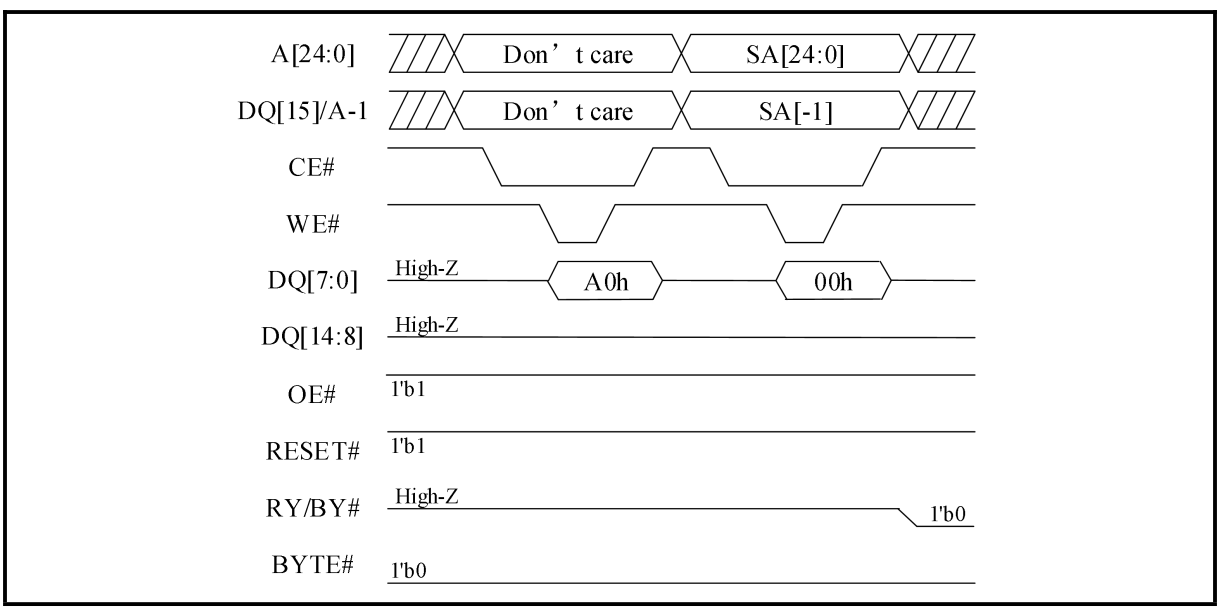


Figure 66. PPB All Erase (word mode)

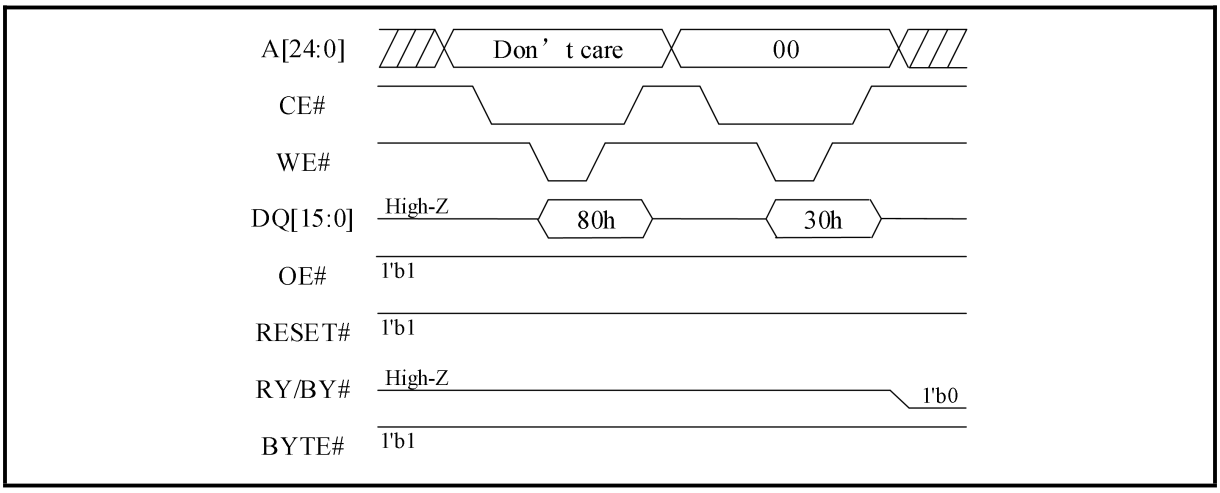
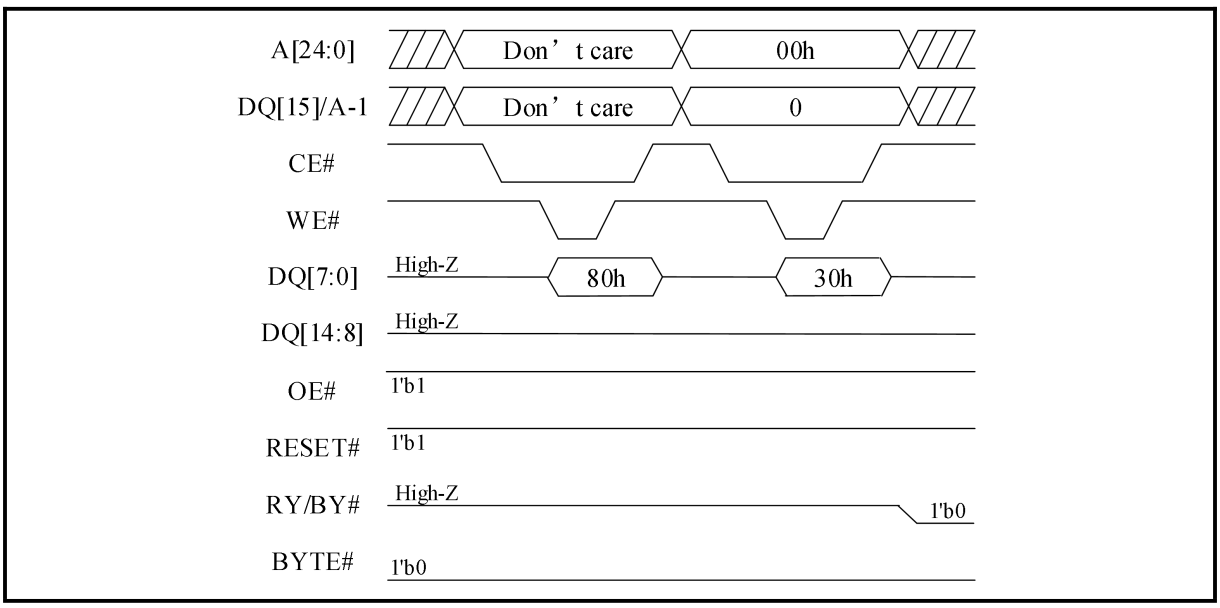


Figure 67. PPB All Erase (byte mode)



5.11.4 Dynamic Protection Bits

Dynamic Protection Bits are volatile and unique for each sector and can be individually modified. DYBs only control the protection scheme for unprotected sectors that have their PPBs cleared (erased to “1”). By issuing the DYB Set or Clear instruction sequences, the DYBs are set (programmed to “0”) or cleared (erased to “1”), thus placing each sector in the protected or unprotected state respectively. This feature allows software to easily protect sectors against inadvertent changes yet does not prevent the easy removal of protection when changes are needed.

Note

1. The DYBs can be set (programmed to “0”) or cleared (erased to “1”) as often as needed. When the parts are first shipped, the PPBs are cleared (erased to “1”) and upon power up or reset, the DYBs can be set or cleared depending upon the ordering option chosen.
2. If the option to clear the DYBs after power up is chosen, (erased to “1”), then the sectors may be modified depending upon the PPB state of that sector
3. The sectors would be in the protected state if the option to set the DYBs after power up is chosen (programmed to “0”).
4. The DYB Set or Clear instructions for the dynamic sectors signify protected or unprotected state of the sectors respectively.
5. DYB bits have the same function when WP#/ACC = V_{HH} as they do when ACC =V_{IH}.
6. Refer to ***Figure 51***-***Figure 52*** for exit instruction.

Figure 68. DYB Enter (word mode)

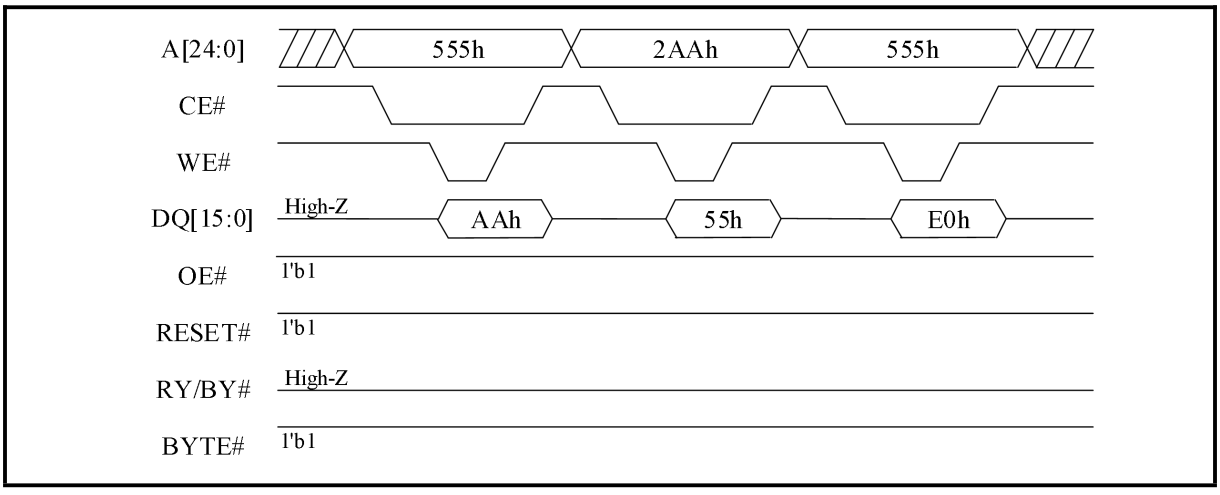


Figure 69. DYB Enter (byte mode)

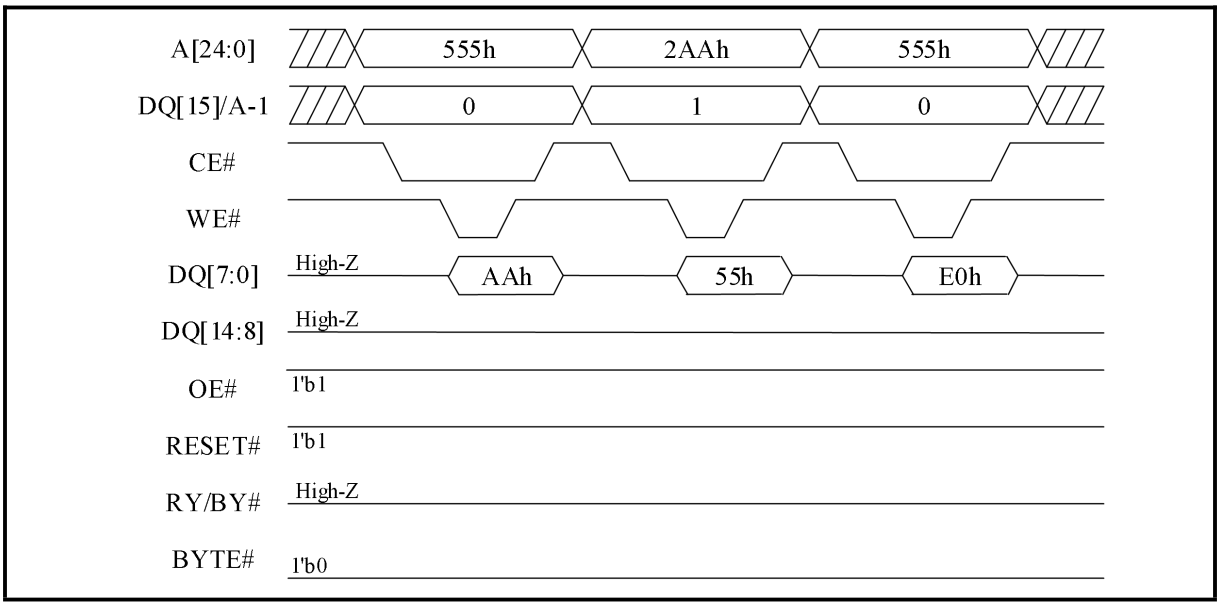


Figure 70. DYB Read(word mode)

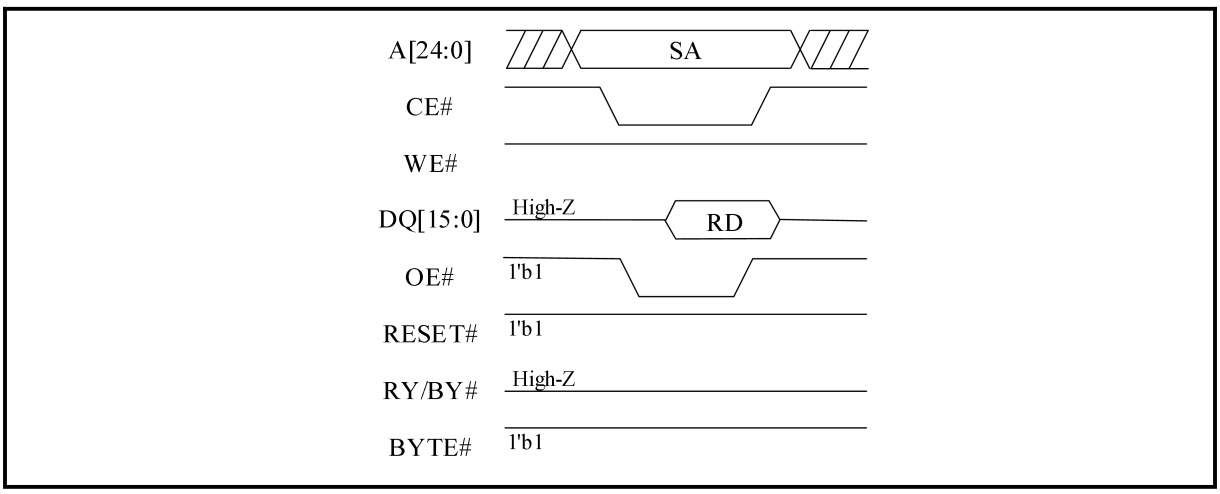


Figure 71. DYB Read (byte mode)

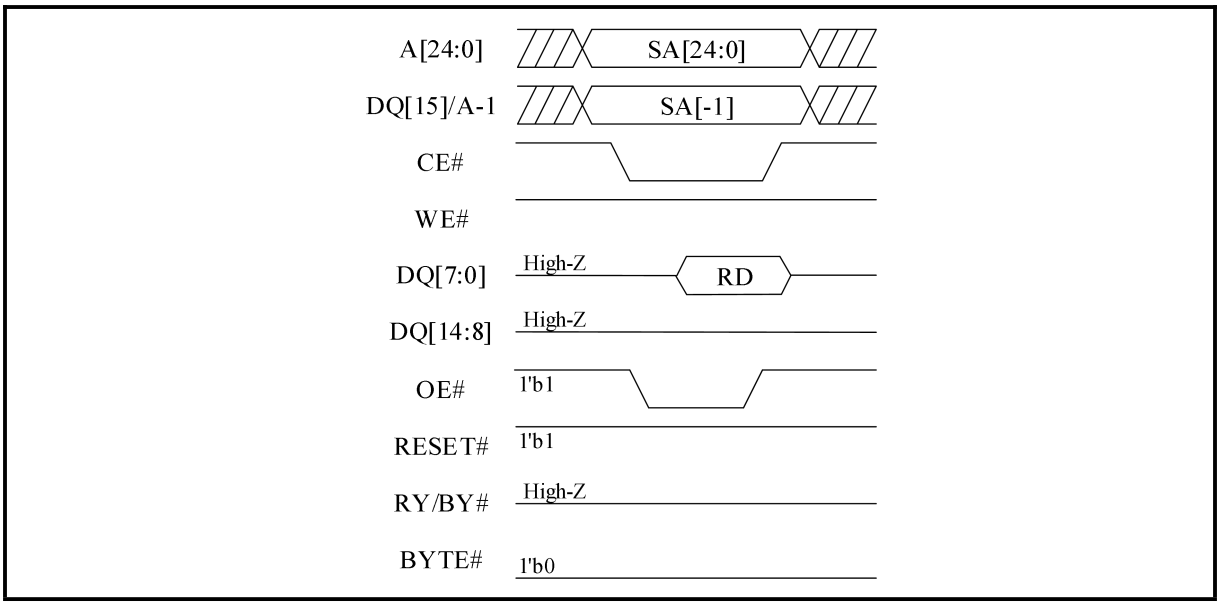


Figure 72. DYB Set (word mode)

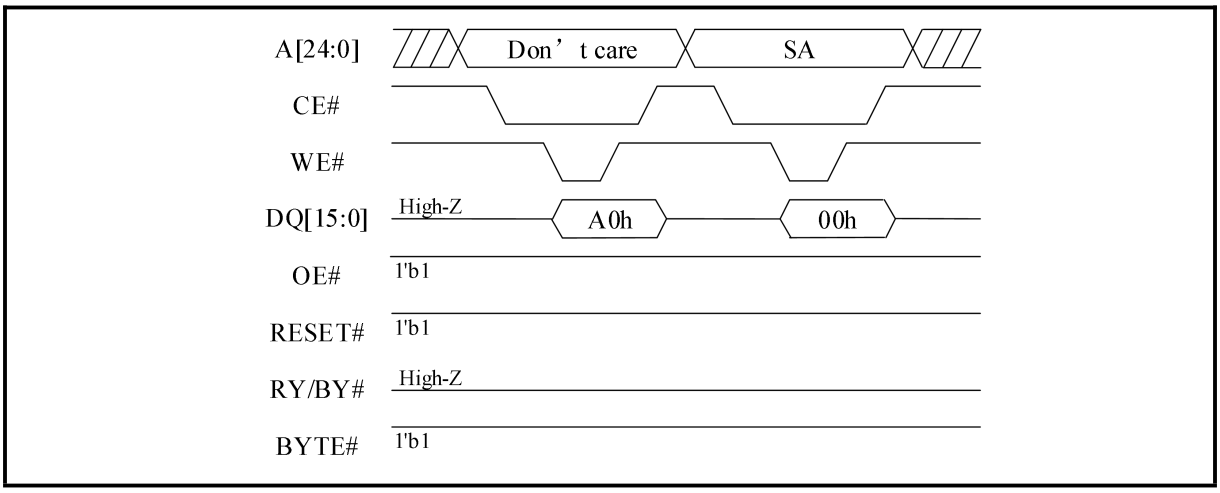


Figure 73. DYB Set (byte mode)

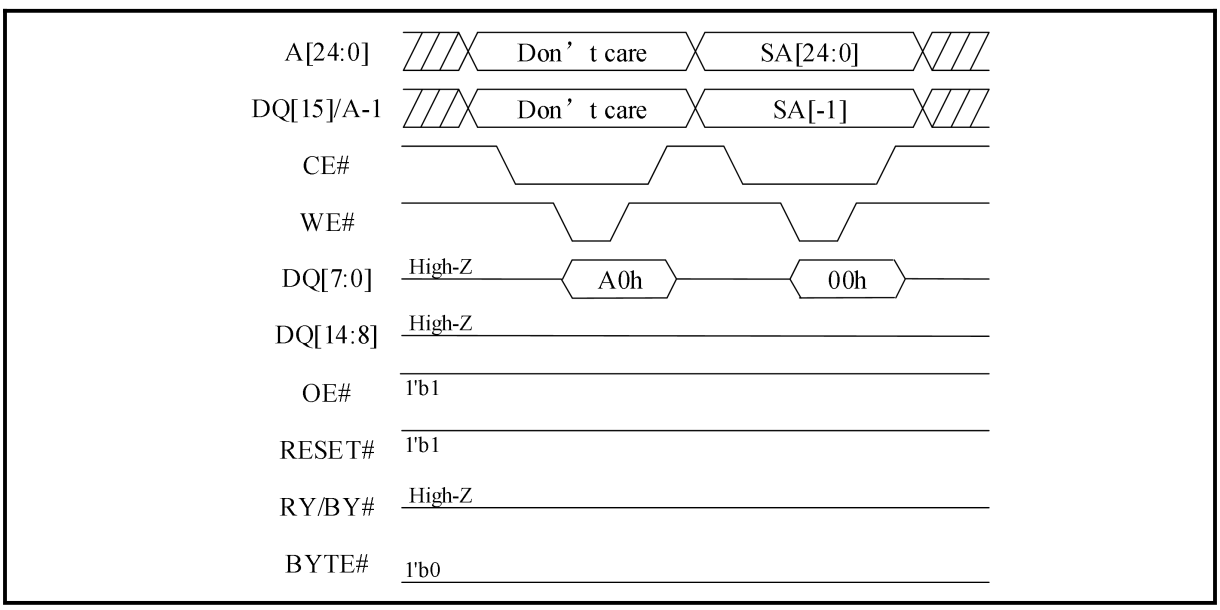


Figure 74. DYB Clear (word mode)

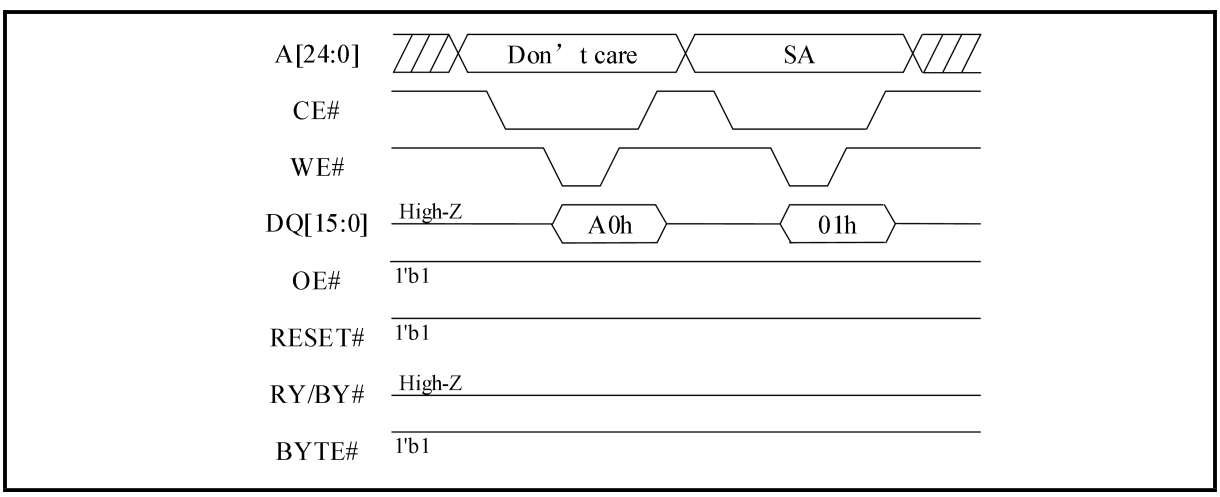
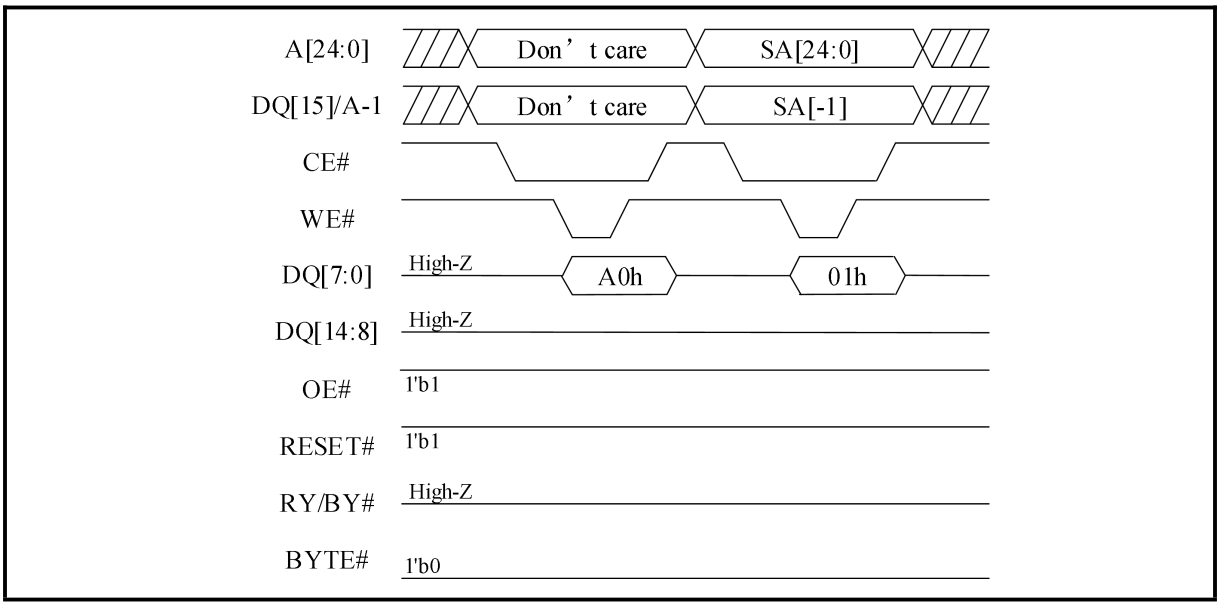


Figure 75. DYB Clear (byte mode)



5.11.5 Password Protection Method

The Password Protection Method allows an even higher level of security than the Persistent Sector Protection Mode by requiring a 64-bit password for unlocking the device PPB Lock Bit. In addition to this password requirement, after power up and reset, the PPB Lock Bit is set “0” to maintain the password mode of operation. Successful execution of the Password Unlock instruction by entering the entire password clears the PPB Lock Bit, allowing for sector PPBs modifications.

Note

1. There is no special addressing order required for programming the password. Once the Password is written and verified, the Password Mode Locking Bit must be set in order to prevent access.
2. The password is all “1”s when shipped from the factory.
3. A “0” cannot be programmed back to a “1”. A succeeding read shows that the data is still “0”.
4. All 64-bit password combinations are valid as a password.
5. There is no means to verify what the password is after it is set.
6. The Password Mode Lock Bit, once set, prevents reading the 64-bit password on the data bus and further password programming.
7. The Password Mode Lock Bit is not erasable.
8. The lower eight address bits (A7–A0) are valid during the Password Read, Password Program, and Password Unlock.
9. The exact password must be entered in order for the unlocking function to occur.
10. The unlock operation will fail if the password provided by the Password Unlock instruction does not match the stored password. This will insert a 1 μs delay (DQ6 bit can be used to determine whether the status is complete) before the next password can be provided to prevent a hacker from running through all the 64-bit combinations in an attempt to correctly match a password.
11. Approximately 1 μs (DQ6 bit can be used to determine whether the status is complete) is required for unlocking the device after the valid 64-bit password is given to the device.
12. Password verification is only allowed before modifying DQ2 (in Lock Register) = 1 to DQ2 = 0.
13. If the password is lost after setting the Password Mode Lock Bit, there is no way to clear the PPB Lock Bit.
14. Refer to ***Figure 51***-***Figure 52*** for exit instruction.

Figure 76. Lock Regsister Program Algorithm

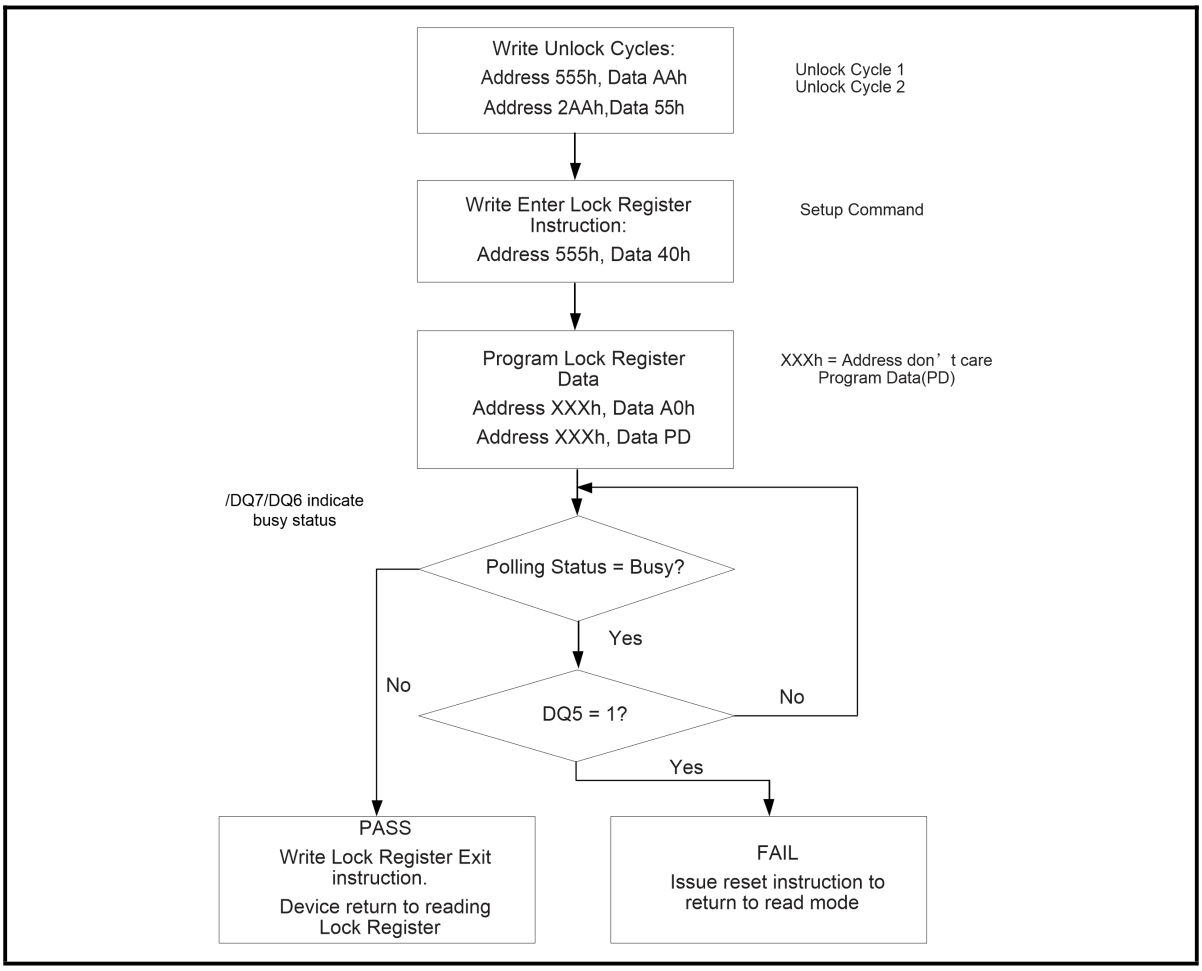


Figure 77. Password Enter (word mode)

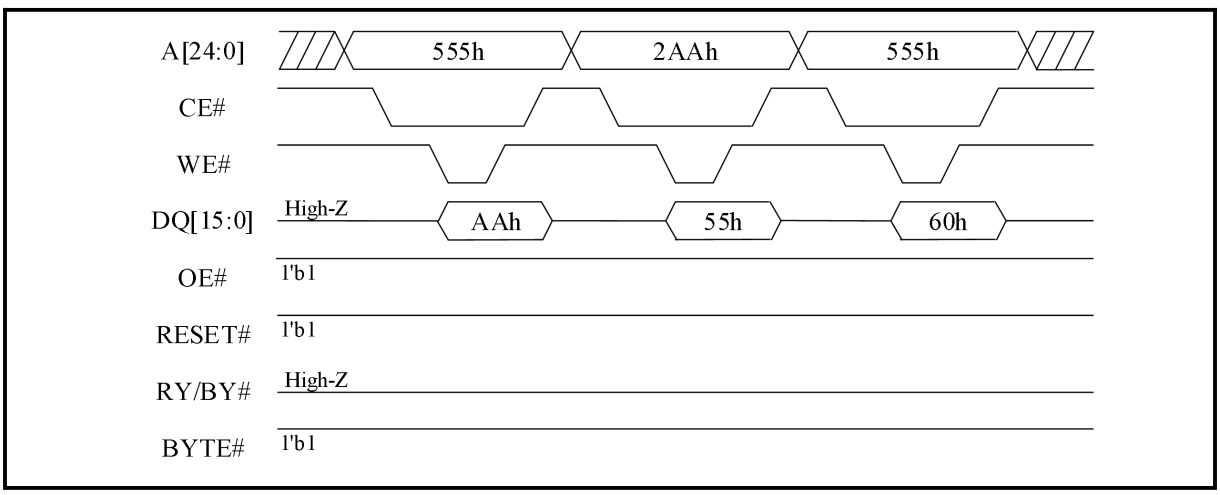


Figure 78. Password Enter (byte mode)

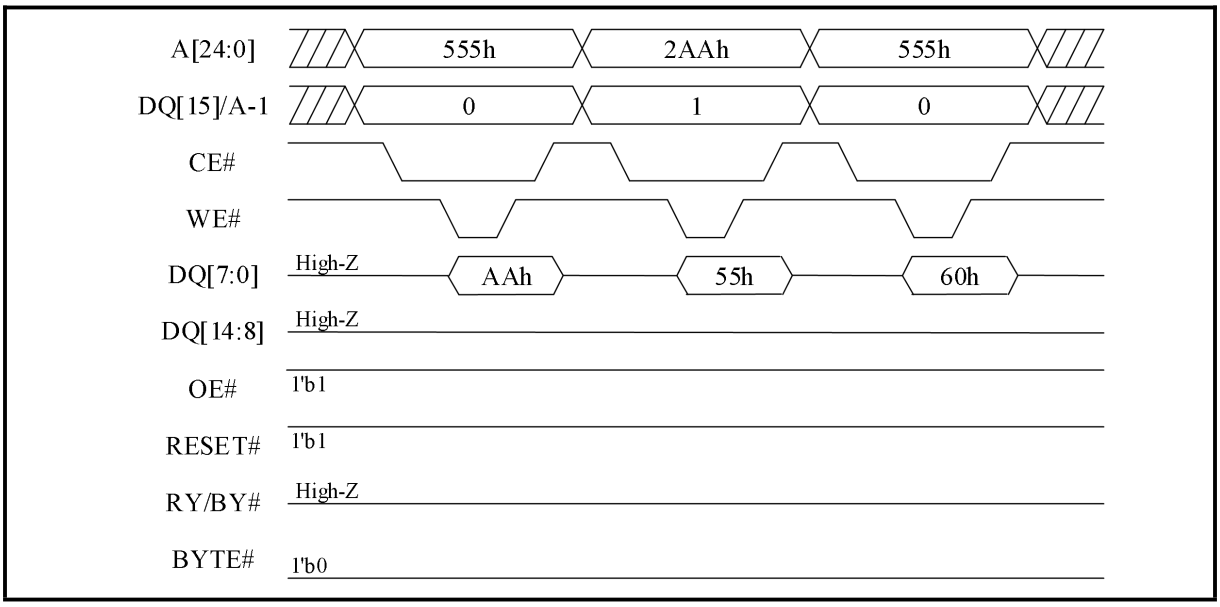


Figure 79. Password Read(word mode)

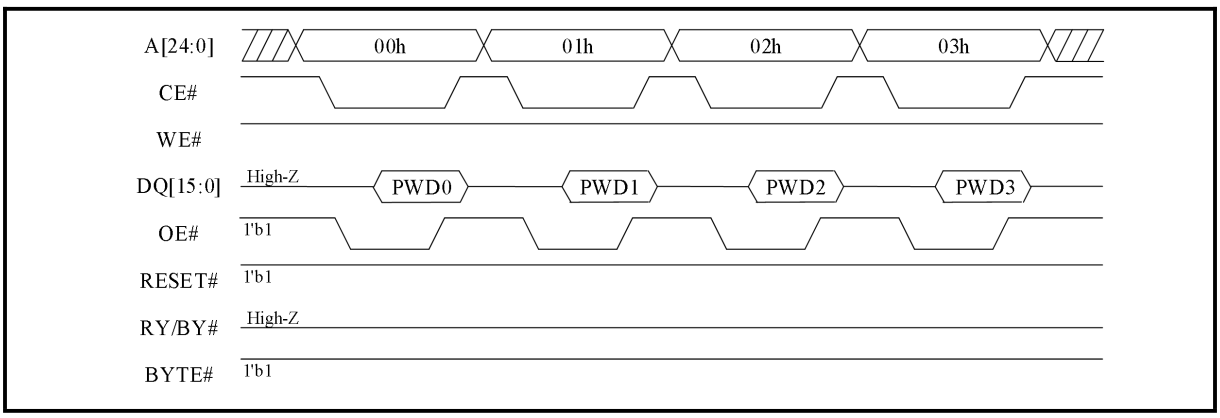


Figure 80. Password Read (byte mode)

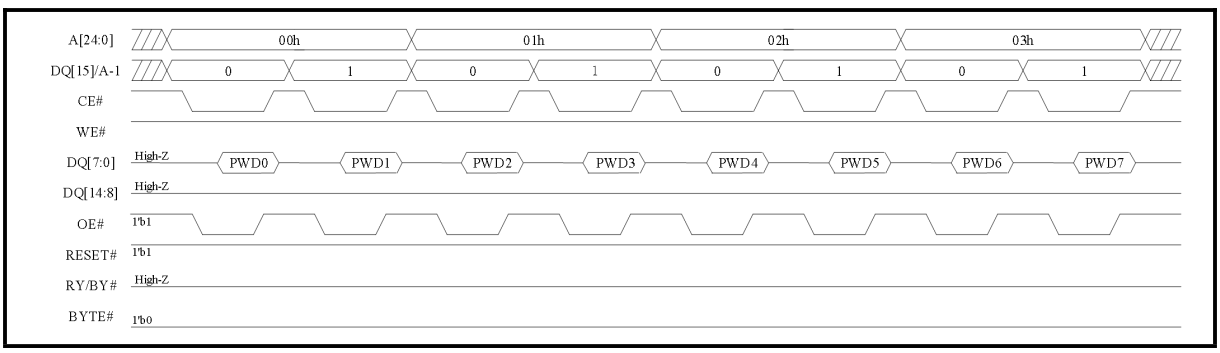


Figure 81. Password Program (word mode)

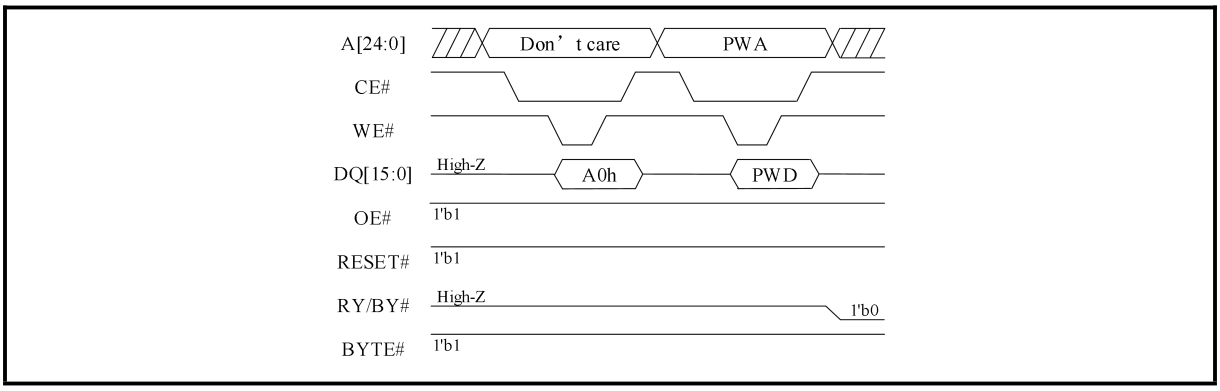


Figure 82. Password Program (byte mode)

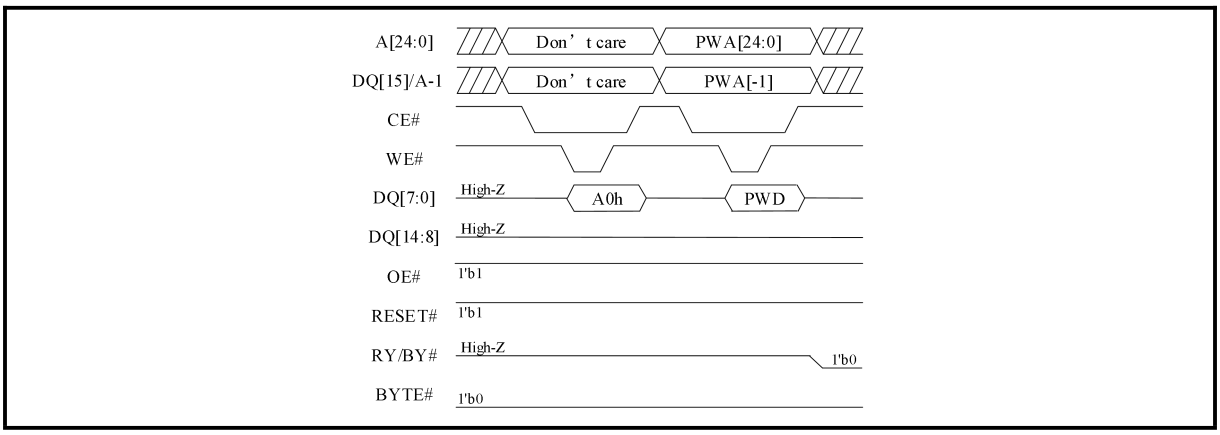


Figure 83. Password Unlock (word mode)

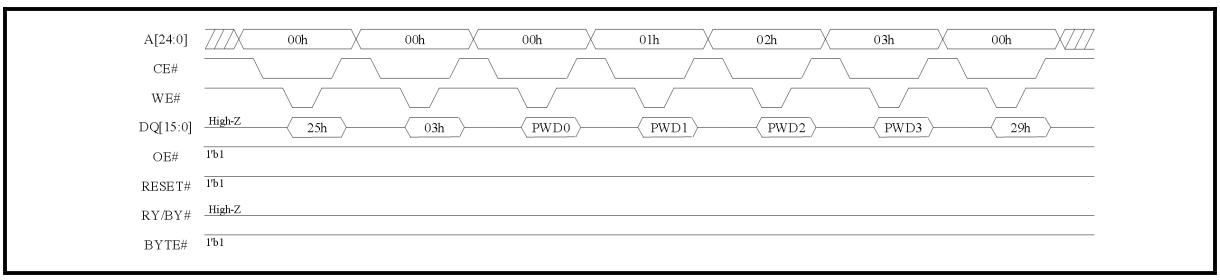
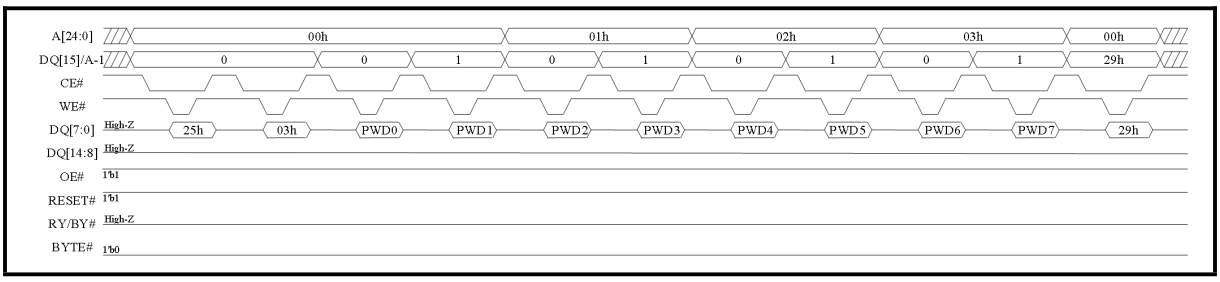


Figure 84. Password Unlock (byte mode)



6. ELECTRICAL CHARACTERISTICS

6.1 Absolute Maximum Ratings

Description		Rating
Storage Temperature, Plastic Packages		–65°C to +150°C
Ambient Temperature with Power Applied		–65°C to +125°C
Voltage with Respect to Ground	All Inputs and I/Os except as noted below (Note 1)	–0.5 V to V_{CC} + 0.5 V
	V_{CC} (Note 1)	–0.5 V to +4.0 V
	V_{IO}	–0.5V to +4.0V
	A9 and ACC (Note 2)	–0.5 V to +12.5 V
Output Short Circuit Current (Note 3)		200 mA

Note

1. *Minimum DC voltage on input or I/Os is –0.5 V. During voltage transitions, inputs or I/Os may undershoot V_{SS} to –2.0 V for periods of up to 20 ns. See **Figure 85**. Maximum DC voltage on input or I/Os is VCC + 0.5 V. During voltage transitions inputs or I/Os may overshoot to V_{CC} + 2.0 V for periods up to 20 ns. See **Figure 86**.*
2. *Minimum DC input voltage on pins A9 and ACC is -0.5V. During voltage transitions, A9 and ACC may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. See **Figure 85**. Maximum DC voltage on pins A9 and ACC is +12.5 V, which may overshoot to 14.0 V for periods up to 20 ns.*
3. *No more than one output may be shorted to ground at a time. Duration of the short circuit should not be greater than one second.*
4. *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.*

Figure 85. Maximum Negative Overshoot Waveform

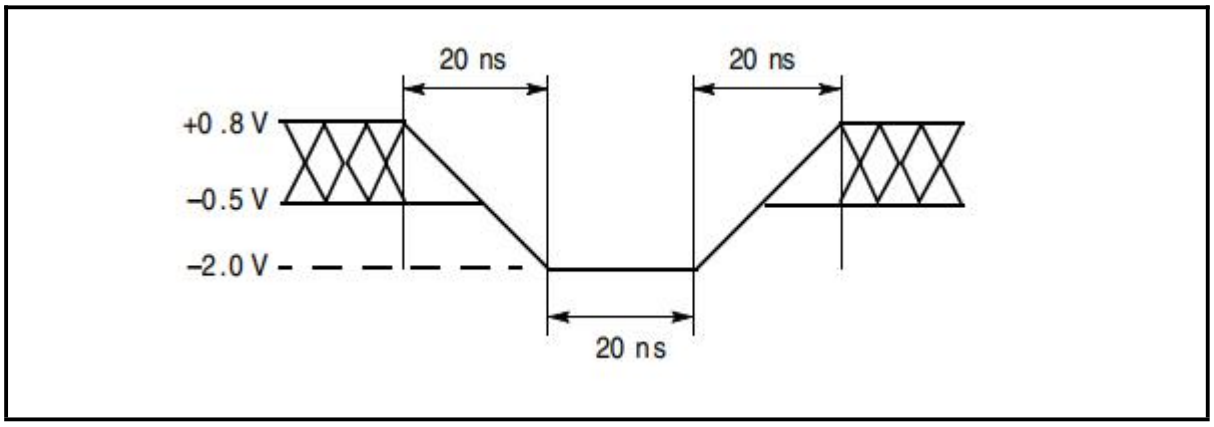
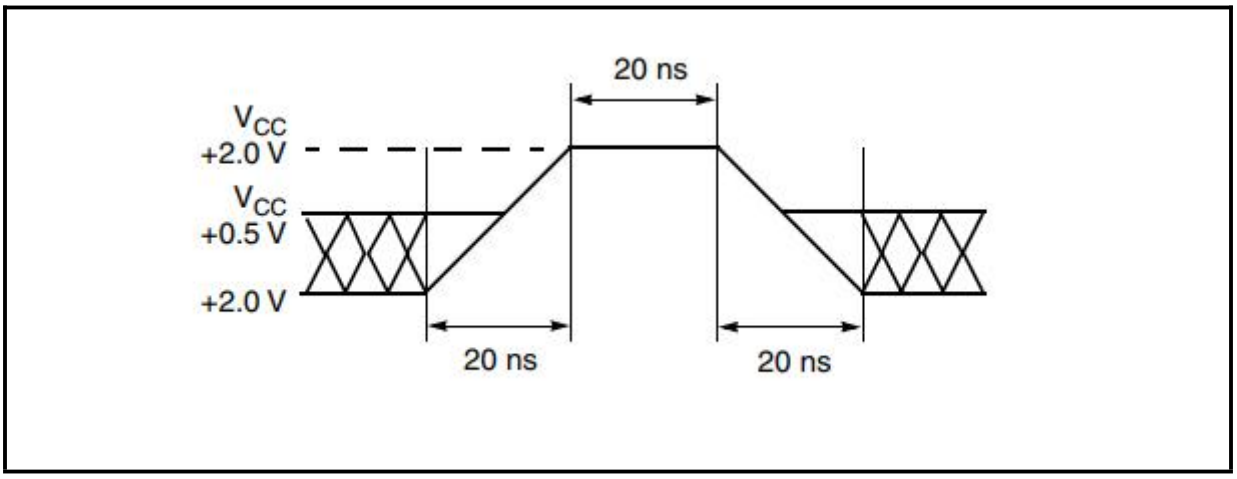


Figure 86. Maximum Positive Overshoot Waveform



6.2 Operating Ranges

Specifications		Range
Ambient Temperature (TA), Industrial (I) Device		–40°C to +85°C
Ambient Temperature (TA), Commercial (C) Device		–40°C to +85°C
Supply Voltages	V_{CC}	+2.7 V to 3.6 V or +3.0 V to 3.6 V
V_{IO} Supply Voltages	V_{IO}	+1.65 V to V_{CC}

Note
1. *Operating ranges define those limits between which the functionality of the device is guaranteed.*
2. *See also **Order Information**.*
3. *For valid V_{CC}/V_{IO} range combinations, see **Order Information**. The I/Os do not operate at 3 V when V_{IO} = 1.8 V.*

6.3 Test Conditions

Figure 87. Test Setup

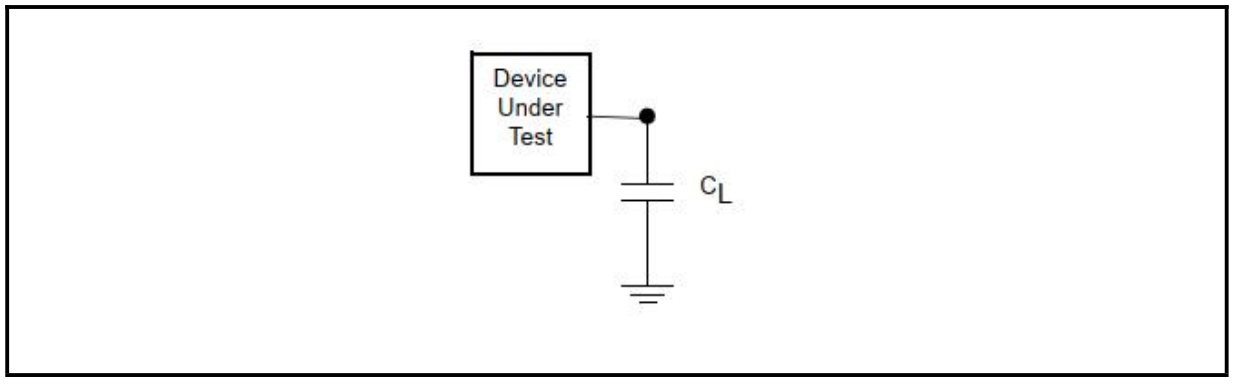


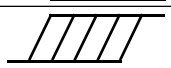
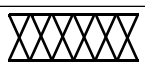
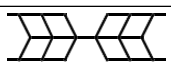
Table 10. Test Specifications

Test Condition	All Speeds	Unit
Output Load Capacitance, C_L (including jig capacitance)	30	pF
Input Rise and Fall Times	5	ns
Input Pulse Levels	0.0–V_{IO}	V
Input timing measurement reference levels (See Note)	0.5V_{IO}	V
Output timing measurement reference levels	0.5V_{IO}	V

Note

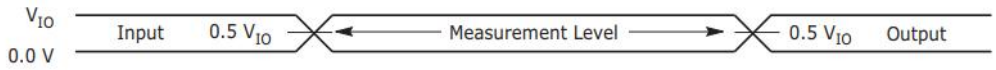
1. If VI_O < V_{CC}, the reference level is 0.5 V_{IO}.

6.4 Key to Switching Waveforms

Waveform	Inputs	Outputs
	Steady	
	Changing from H to L	
	Changing from L to H	
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High Impedance State (High Z)

6.5 Switching Waveforms

Figure 88. Input Waveforms and Measurement Levels



Note

1. If V_{IO} < V_{CC}, the input measurement reference level is 0.5 V_{IO}.

6.6 DC Characteristics

DC Characteristics (CMOS Compatible)

Parameter Symbol	Parameter Description (Notes)	Test Conditions		Min	Typ	Max	Unit
I_{LI}	Input Load Current	V_{IN} = V_{SS} to V_{CC}, V_{CC} = $V_{CC\ max}$	WP/ACC			±5.0	µA
			Others			±2.0	
I_{LIT}	A9 Input Load Current	V_{CC} = $V_{CC\ max}$; A9 = 12.5 V				35	µA
I_{LO}	Output Leakage Current	V_{OUT} = V_{SS} to V_{CC}, V_{CC} = $V_{CC\ max}$				±1.0	µA
I_{CC1}	V_{CC} Active Read Current (1)	CE# = V_{IL}, OE# = V_{IH}, V_{CC} = V_{CCmax}, *f* = 1 MHz			2	20	mA
		CE# = V_{IL}, OE# = V_{IH}, V_{CC} = V_{CCmax}, *f* = 5 MHz			8	55	
		CE# = V_{IL}, OE# = V_{IH}, V_{CC} = V_{CCmax}, *f* = 10 MHz			20	110	
I_{IO2}	V_{IO} Non-Active Output	CE# = V_{IL}, OE# = V_{IH}			0.2	10	mA
I_{CC2}	V_{CC} Intra-Page Read Current (1)	CE# = V_{IL}, OE# = V_{IH}, V_{CC} = V_{CCmax}, *f* = 10 MHz			1	10	mA
		CE# = V_{IL}, OE# = V_{IH}, V_{CC} = V_{CCmax}, *f* = 33 MHz			5	20	
I_{CC3}	V_{CC} Active Erase/ Program Current (2, 3)	CE# = V_{IL}, OE# = V_{IH}, V_{CC} = V_{CCmax}			50	90	mA
I_{CC4}	V_{CC} Standby Current	CE#, RESET# = V_{CC} ± 0.3 V, OE# = V_{IH}, V_{CC} = V_{CCmax} V_{IL} = V_{SS} + 0.3 V/-0.1V,			100	500	µA
I_{CC5}	V_{CC} Reset Current	V_{CC} = V_{CCmax}; V_{IL} = V_{SS} + 0.3 V/-0.1V, RESET# = V_{SS} ± 0.3 V			250	500	µA
I_{CC6}	Automatic Sleep Mode (4)	V_{CC} = V_{CCmax}, V_{IH} = V_{CC} ± 0.3 V, V_{IL} = V_{SS} + 0.3 V/-0.1V, WP#/ACC = V_{IH}			100	500	µA
I_{ACC}	ACC Accelerated Program Current	CE# = V_{IL}, OE# = V_{IH}, V_{CC} = V_{CCmax}, WP#/ACC = V_{HH}	WP#/ACC pin		10	20	mA
			V_{CC} pin		50	80	
V_{IL}	Input Low Voltage (5)			–0.1		0.3 x V_{IO}	V
V_{IH}	Input High Voltage (5)			0.7 x V_{IO}		V_{IO} + 0.3	V
V_{HH}	Voltage for Program Acceleration	V_{CC} = 2.7 –3.6 V		11.5		12.5	V
V_{ID}	Voltage for Autoselect and Temporary Sector Unprotect	V_{CC} = 2.7 –3.6 V		11.5		12.5	V
V_{OL}	Output Low Voltage (5)	I_{OL} = 100 µA				0.15 x V_{IO}	V
V_{OH}	Output High Voltage (5)	I_{OH} = -100 µA		0.85 x V_{IO}			V
V_{LKO}	Low V_{CC} Lock-Out Voltage (3)			2.3		2.5	V

Note

1. *The ICC current listed is typically less than 2 mA/MHz, with OE# at VIH.*
2. *ICC active while Embedded Erase or Embedded Program or Write Buffer Programming is in progress.*
3. *Not 100% tested.*
4. *Automatic sleep mode enables the lower power mode when addresses remain stable tor t_{ACC} + 30 ns.*
5. *V_{CC} = 3 V and V_{IO} = 3V or 1.8V. When V_{IO} is at 1.8V, I/O pins cannot operate at 3V.*

6.7 AC Characteristics

6.7.1 Read Operations

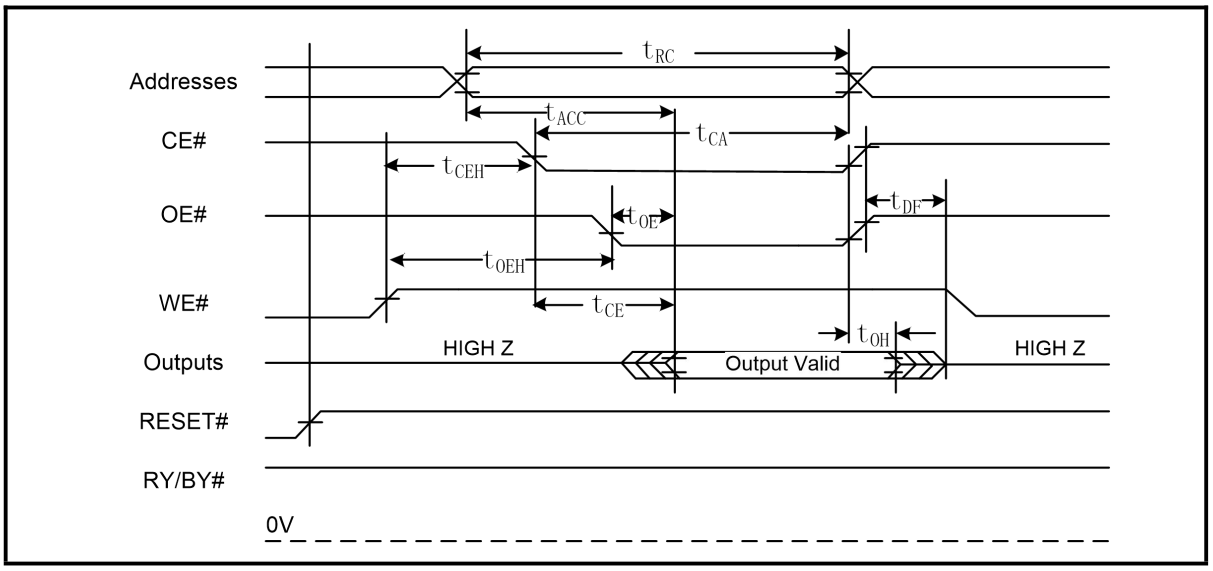
Read Operations

Parameter		Description (Notes)		Test Setup		Speed Options			Unit
JEDEC	Std.					110	120	130	
t_{AVAV}	t_{RC}	Read Cycle Time		$V_{IO} = V_{CC} = 2.7$ V	Min	110	120	–	ns
				$V_{IO} = 1.65$ V to V_{CC}, $V_{CC} = 3$ V		110	120	130	
				$V_{IO} = V_{CC} = 3.0$ V		110	–	–	
t_{AVQV}	t_{ACC}	Address to Output Delay (1)		$V_{IO} = V_{CC} = 2.7$ V	Max	110	120	–	ns
				$V_{IO} = 1.65$ V to V_{CC}, $V_{CC} = 3$ V		110	120	130	
				$V_{IO} = V_{CC} = 3.0$ V		110	–	–	
t_{ELQV}	t_{CE}	Chip Enable to Output Delay (2)		$V_{IO} = V_{CC} = 2.7$ V	Max	110	120	–	ns
				$V_{IO} = 1.65$ V to V_{CC}, $V_{CC} = 3$ V		110	120	130	
				$V_{IO} = V_{CC} = 3.0$ V		110	–	–	
	t_{PACC}	Page Access Time			Max	25			ns
t_{GLQV}	t_{OE}	Output Enable to Output Delay			Max	25			ns
t_{EHQZ}	t_{DF}	Chip Enable to Output High Z (3)			Max	20			ns
t_{GHQZ}	t_{DF}	Output Enable to Output High Z (3)			Max	20			ns
t_{AXQX}	t_{OH}	Output Hold Time From Addresses, CE# or OE#, Whichever Occurs First			Min	0			ns
	t_{OEH}	Output Enable Hold Time (3)	Read		Min	0			ns
			Toggle and Data# Polling		Min	10			ns
	t_{CEH}	Chip Enable Hold Time	Read		Min	35			ns
	t_{CA}	Chip Enable to address change		$V_{IO} = V_{CC} = 2.7$ V	Min	110	120	–	ns
				$V_{IO} = 1.65$ V to V_{CC}, $V_{CC} = 3$ V		110	120	130	
				$V_{IO} = V_{CC} = 3.0$ V		110	–	–	

Note

1. *CE#, OE# = V_{IL}*
2. *OE# = V_{IL}*
3. *Not 100% tested.*
4. *See Figure87 and Table10 for test specifications.*
5. *Unless otherwise indicated, AC specifications for 110 ns speed options are tested with $V_{IO} = V_{CC} = 2.7$ V. AC specifications for 110 ns speed options are tested with $V_{IO} = 1.8$ V and $V_{CC} = 3.0$ V.*

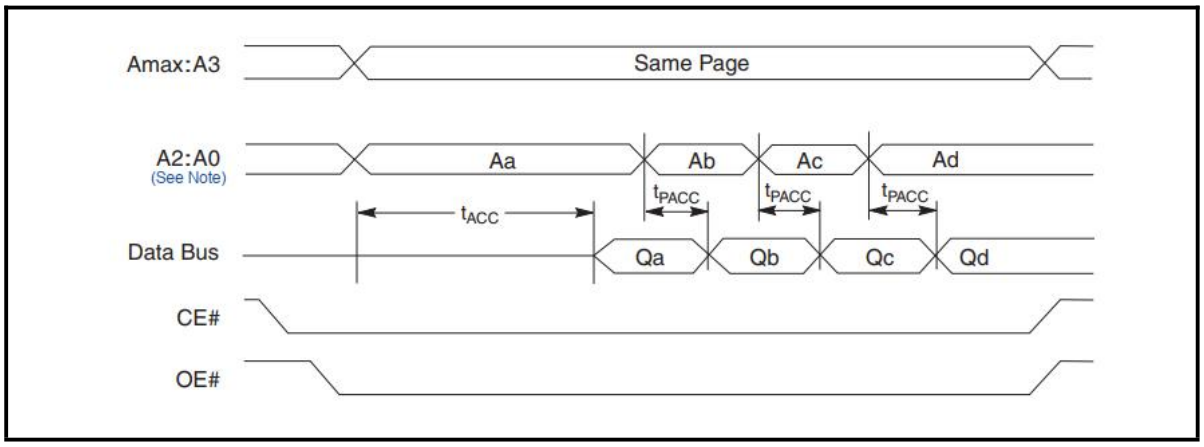
Figure 89. Read Operation Timings



Note

1. *For **Figure 89** parameters t_{CEH} and t_{OEH} are specific to a read cycle following a flash write operation.*

Figure 90. Page Read Timings



Note

1. ***Figure 90** shows word mode. Addresses are A2:A-1 for byte mode.*

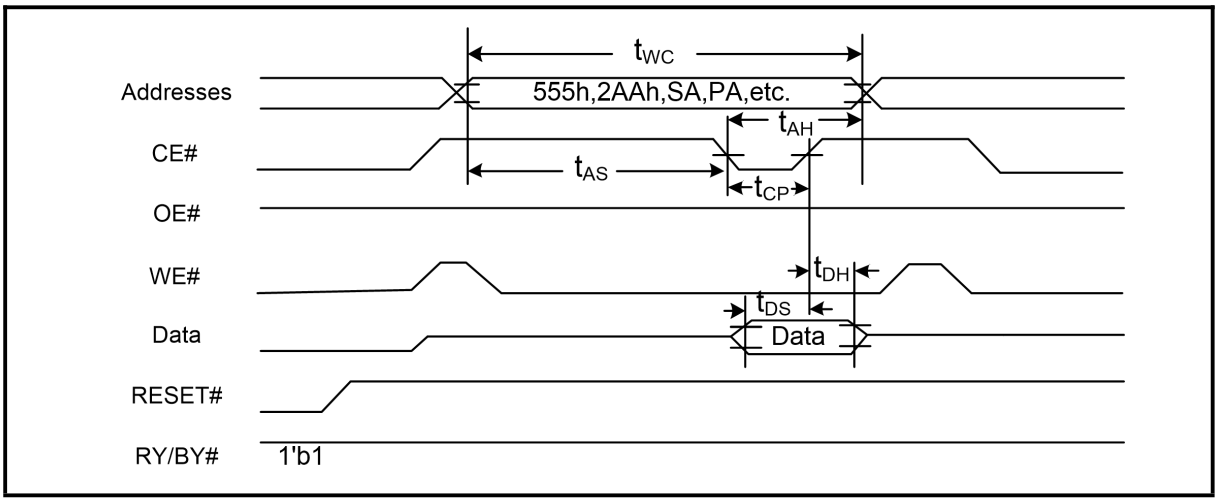
6.7.2 CE#/WE# Controlled Write Operations

CE#/WE# Controlled Write Operations

Parameter		Description (Notes)		Speed Options			
JEDEC	Std.			110	120	130	Unit
t_{AVAV}	t_{WC}	Write Cycle Time (Note 1)	Min	110	120	130	ns
	t_{AS}	Address Setup Time	Min	0			ns
	t_{AH}	Address Hold Time	Min	45			ns
	t_{CP}	CE# Pulse Width	Min	35			ns
	t_{WP}	WE# Pulse Width	Min	35			ns
	t_{DS}	Data Setup Time	Min	30			ns
	t_{DH}	Data Hold Time	Min	0			ns

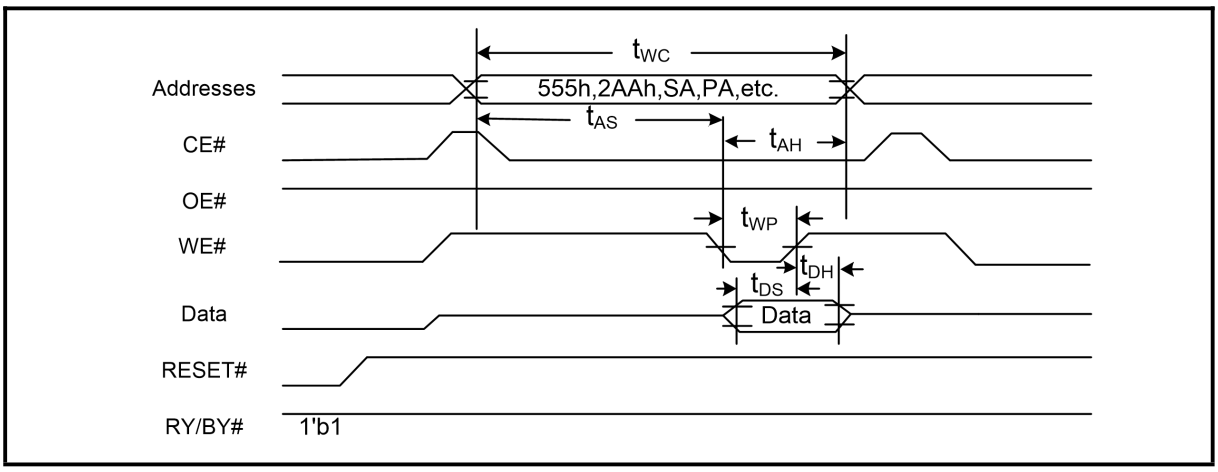
Note
1. *Not 100% tested.*
2. *See **DC Characteristics** for more information.*
3. *Unless otherwise indicated, AC specifications are tested with V_{IO} = 1.8 V and V_{CC} = 3.0 V.*

Figure 91. CE# Controlled Write Operation Timings



Note
1. *PA = program address, SA = sector address.*

Figure 92. WE# Controlled Write Operation Timings



Note
1. *PA = program address, SA = sector address.*
2. *CE # can be kept low or pulled high again for each cycle.*

6.7.3 Erase and Program Operations

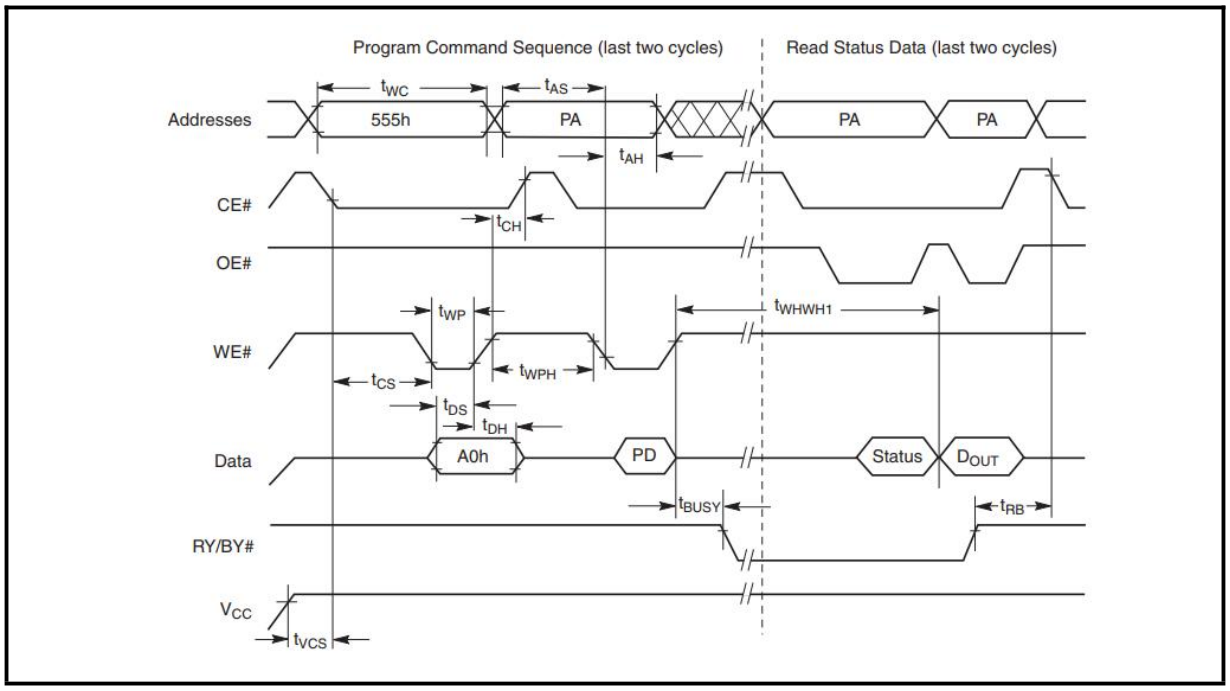
Erase and Program Operations

Parameter		Description			Speed Options			Unit
JEDEC	Std.				110	120	130	
t_{AVAV}	t_{WC}	Write Cycle Time (Note 1)		Min	110	120	130	ns
t_{AVWL}	t_{AS}	Address Setup Time		Min	0			ns
	t_{ASO}	Address Setup Time to OE# low during toggle bit polling		Min	15			ns
t_{WLAX}	t_{AH}	Address Hold Time		Min	45			ns
	t_{AHT}	Address Hold Time From CE# or OE# high during toggle bit polling		Min	0			ns
t_{DVWH}	t_{DS}	Data Setup Time		Min	30			ns
t_{WHDX}	t_{DH}	Data Hold Time		Min	0			ns
	t_{CEPH}	CE# High during toggle bit polling		Min	20			ns
	t_{OEPH}	Output Enable High during toggle bit polling		Min	20			ns
t_{ELWL}	t_{CS}	CE# Setup Time		Min	0			ns
t_{WHEH}	t_{CH}	CE# Hold Time		Min	0			ns
t_{WLWH}	t_{WP}	Write Pulse Width		Min	35			ns
t_{WHDL}	t_{WPH}	Write Pulse Width High		Min	30			ns
t_{WHWH1}	t_{WHWH1}	Write Buffer Program Operation (Notes 2, 3)		Typ	480			µs
		Effective Write Buffer Program Operation (Notes 2, 4)	Per Word	Typ	15			µs
		Accelerated Effective Write Buffer Program Operation (Notes 2, 4)	Per Word	Typ	13.5			µs
		Program Operation (Note 2)	Word	Typ	60			µs
		Accelerated Programming Operation (Note 2)	Word	Typ	54			µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 2)		Typ	0.5			sec
	t_{VHH}	V_{HH} Rise and Fall Time (Note 1)		Min	250			ns
	t_{VCS}	V_{CC} Setup Time (Note 1)		Min	35			µs
	t_{BUSY}	Erase/Program Valid to RY/BY# Delay		Max	90			ns
	t_{SEA}	Sector Erase Timeout		Max	50			µs

Note

1. *Not 100% tested.*
2. *See **DC Characteristics** for more information.*
3. *For 1–32 words/1–64 bytes programmed.*
4. *Effective write buffer specification is based upon a 32-word/64-byte write buffer operation.*
5. *Unless otherwise indicated, AC specifications for 110 ns speed option are tested with*
6. *V_{IO} = V_{CC} = 2.7 V. AC specifications for 110 ns speed options are tested with V_{IO} = 1.8 V and V_{CC} = 3.0 V.*

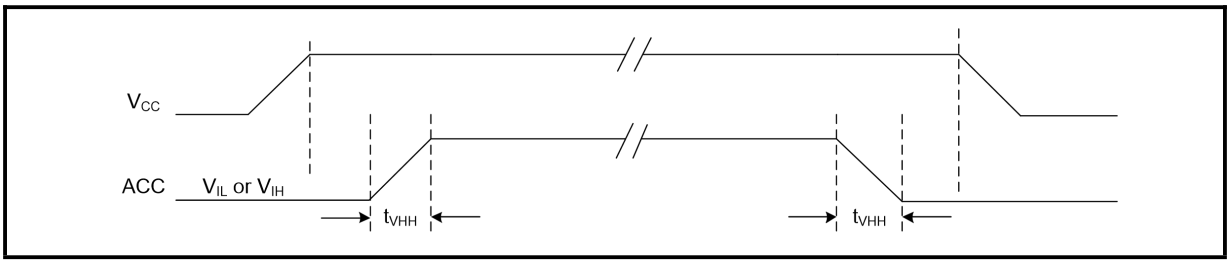
Figure 93. Program Operation Timings



Note

1. *PA = program address, PD = program data, D_{OUT} is the true data at the program address.*
2. *Illustration shows device in word mode.*

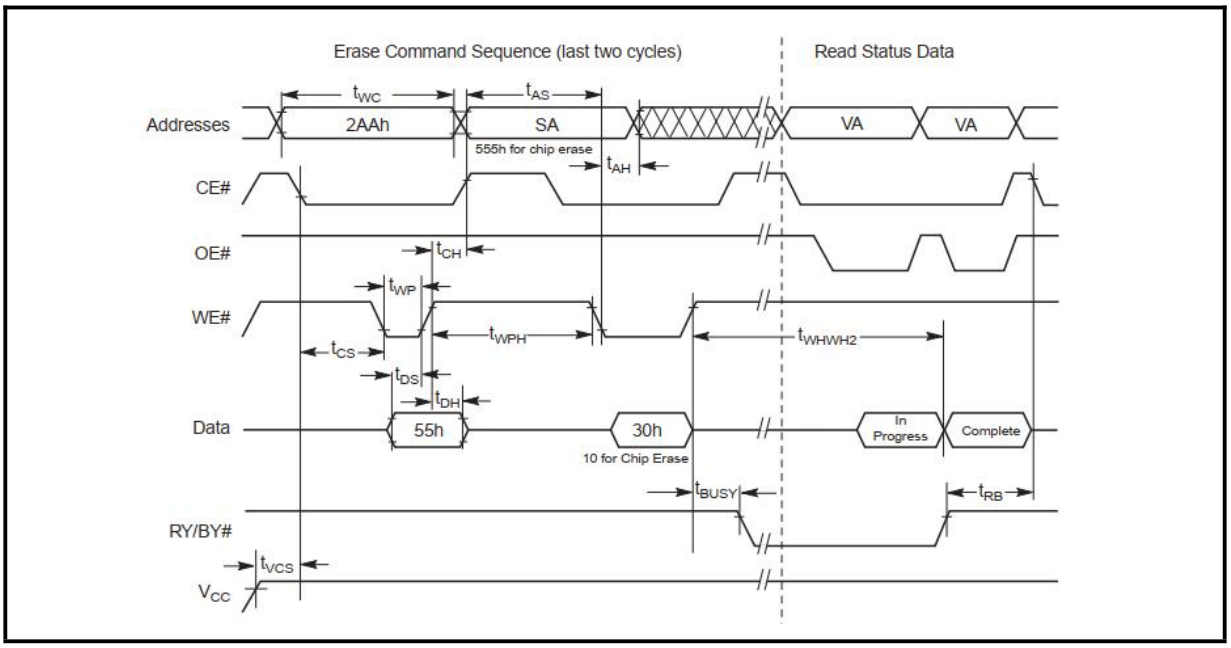
Figure 94. Accelerated Program Timing Diagram



Note

1. *Not 100% tested.*
2. *CE#, OE# = V_{IL}.*
3. *OE# = V_{IL}.*
4. *See Figure87 and Table10 for test specifications.*

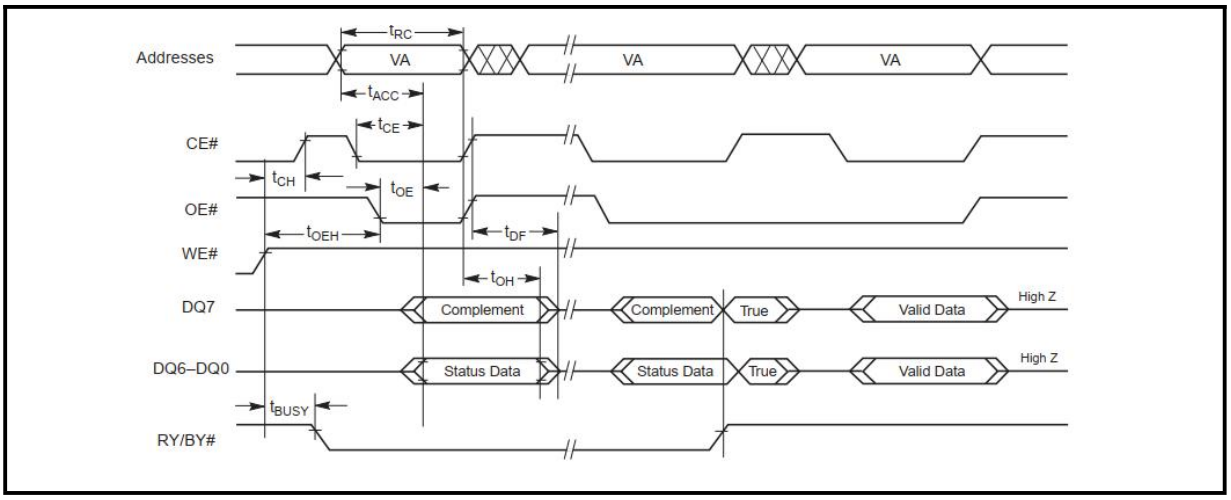
Figure 95. Chip/Sector Erase Operation Timings



Note

1. *SA = sector address (for Sector Erase), VA = Valid Address for reading status data (**Write Operation Status**).*
2. *These waveforms are for the word mode. Input Waveforms and Measurement Levels.*

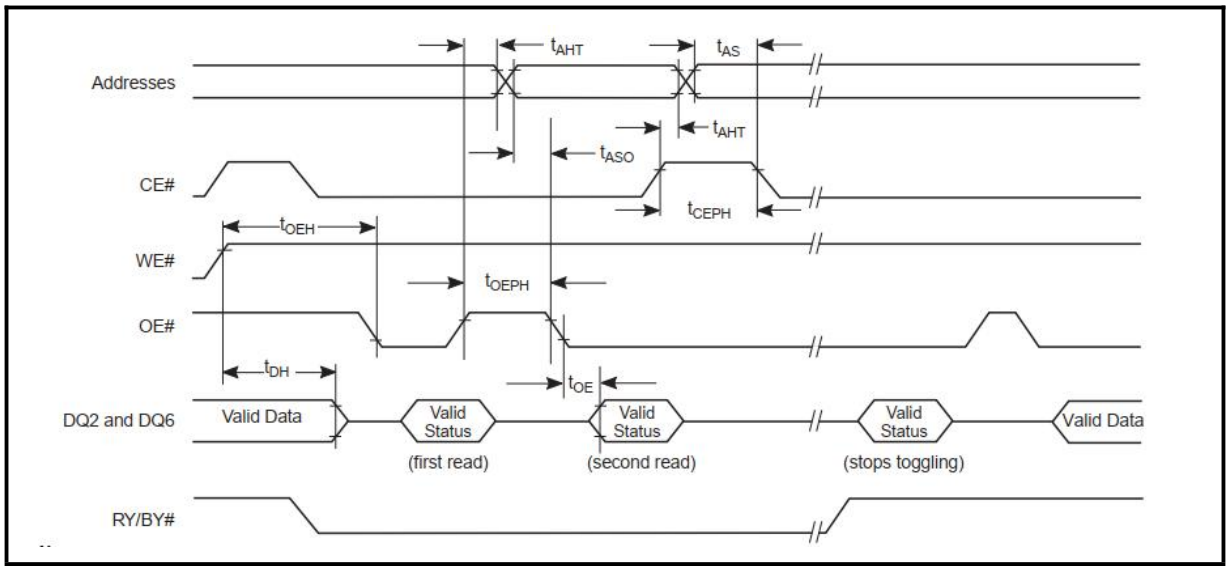
Figure 96. Data# Polling Timings (During Embedded Algorithms)



Note

1. *VA = Valid address. Illustration shows first status cycle after instruction sequence, last status read cycle, and array data read cycle.*
2. *t_{OE} for data polling is 45 ns when V_{IO} = 1.65 to 2.7 V and is 35 ns when V_{IO} = 2.7 to 3.6 V*
3. *CE# does not need to go high between status bit reads*

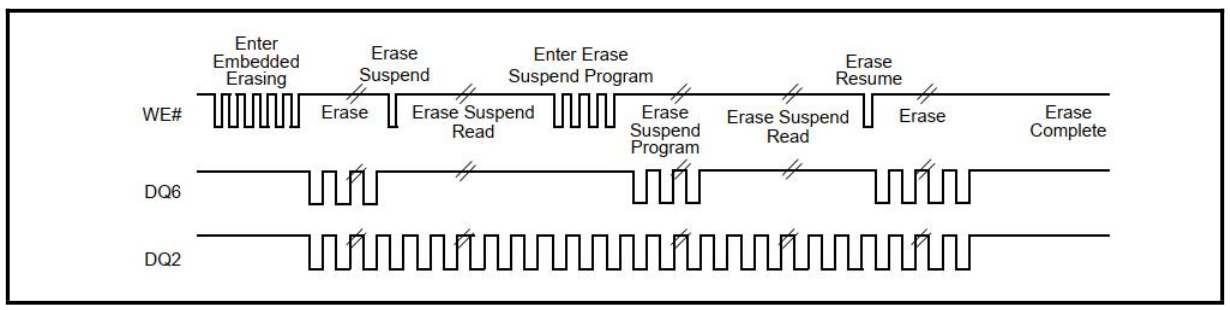
Figure 97. Toggle Bit Timings (During Embedded Algorithms)



Note

1. *A = Valid address; not required for DQ6. Illustration shows first two status cycle after instruction sequence, last status read cycle, and array data read cycle CE# does not need to go high between status bit reads.*

Figure 98.DQ2 vs. DQ6



Note

1. *DQ2 toggles only when read at an address within an erase-suspended sector. The system can use OE# or CE# to toggle DQ2 and DQ6.*

6.7.4 Alternate CE# Controlled Erase and Program Operations

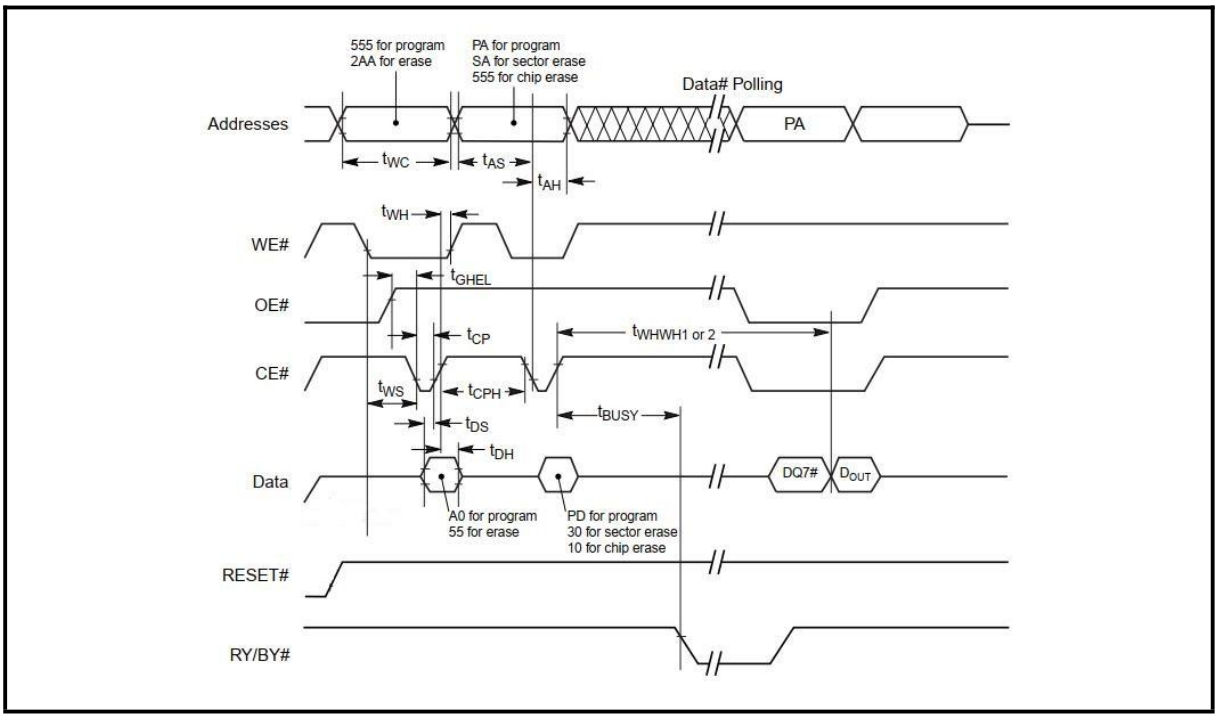
Alternate CE# Controlled Erase and Program Operations

Parameter		Description (Notes)			Speed Options			
JEDEC	Std.				110	120	130	Unit
t_{AVAV}	t_{WC}	Write Cycle Time (Note 1)		Min	110	120	130	ns
t_{AVWL}	t_{AS}	Address Setup Time		Min	0			ns
	t_{ASO}	Address Setup Time to OE# low during toggle bit polling		Min	15			ns
t_{ELAX}	t_{AH}	Address Hold Time		Min	45			ns
	t_{AHT}	Address Hold Time From CE# or OE# high during toggle bit polling		Min	0			ns
t_{DVEH}	t_{DS}	Data Setup Time		Min	30			ns
t_{EHDX}	t_{DH}	Data Hold Time		Min	0			ns
	t_{CEPH}	CE# High during toggle bit polling		Min	20			ns
	t_{OEPH}	OE# High during toggle bit polling		Min	20			ns
t_{GHEL}	t_{GHEL}	Read Recovery Time Before Write (OE# High to CE# Low)		Min	0			ns
t_{WLEL}	t_{WS}	WE# Setup Time		Min	0			ns
t_{EHWH}	t_{WH}	WE# Hold Time		Min	0			ns
t_{ELEH}	t_{CP}	CE# Pulse Width		Min	35			ns
t_{EHEL}	t_{CPH}	CE# Pulse Width High		Min	30			ns
t_{WHWH1}	t_{WHWH1}	Write Buffer Program Operation (Notes 2, 3)		Typ	480			µs
		Effective Write Buffer Program Operation (Notes 2, 4)	Per Word	Typ	15			µs
		Effective Accelerated Write Buffer Program Operation (Notes 2, 4)	Per Word	Typ	13.5			µs
		Program Operation (Note 2)	Word	Typ	60			µs
		Accelerated Programming Operation (Note 2)	Word	Typ	54			µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 2)		Typ	0.5			sec

Note

1. *Not 100% tested.*
2. *See **DC Characteristics** for more information.*
3. *For 1–32 words/1–64 bytes programmed.*
4. *Effective write buffer specification is based upon a 32-word/64-byte write buffer operation.*
5. *Unless otherwise indicated, AC specifications are tested with V_{IO} = 1.8 V and V_{CC} = 3.0 V.*

Figure 99. Alternate CE# Controlled Write (Erase/Program) Operation Timings



Note

1. ***Figure 99*** *indicates last two bus cycles of a program or erase operation.*
2. *PA = program address, SA = sector address, PD = program data.*
3. *DQ7# is the complement of the data written to the device. DOUT is the data written to the device.*
4. *Waveforms are for the word mode.*

6.7.5 Erase And Programming Performance

Erase And Programming Performance

Parameter		Typ (Note 1)	Max (Note 2)	Unit	Comments
Sector Erase Time		0.5	3.5	sec	Excludes 00h programming prior to erasure (Note 4)
Chip Erase Time	BY29G512FS	512	2048	sec	
Total Write Buffer Time (Note 3)		480		µs	Excludes system level overhead (Note 5)
Total Accelerated Write Buffer Programming Time (Note 3)		432		µs	
Chip Program Time	BY29G512FS	984		sec	

Note

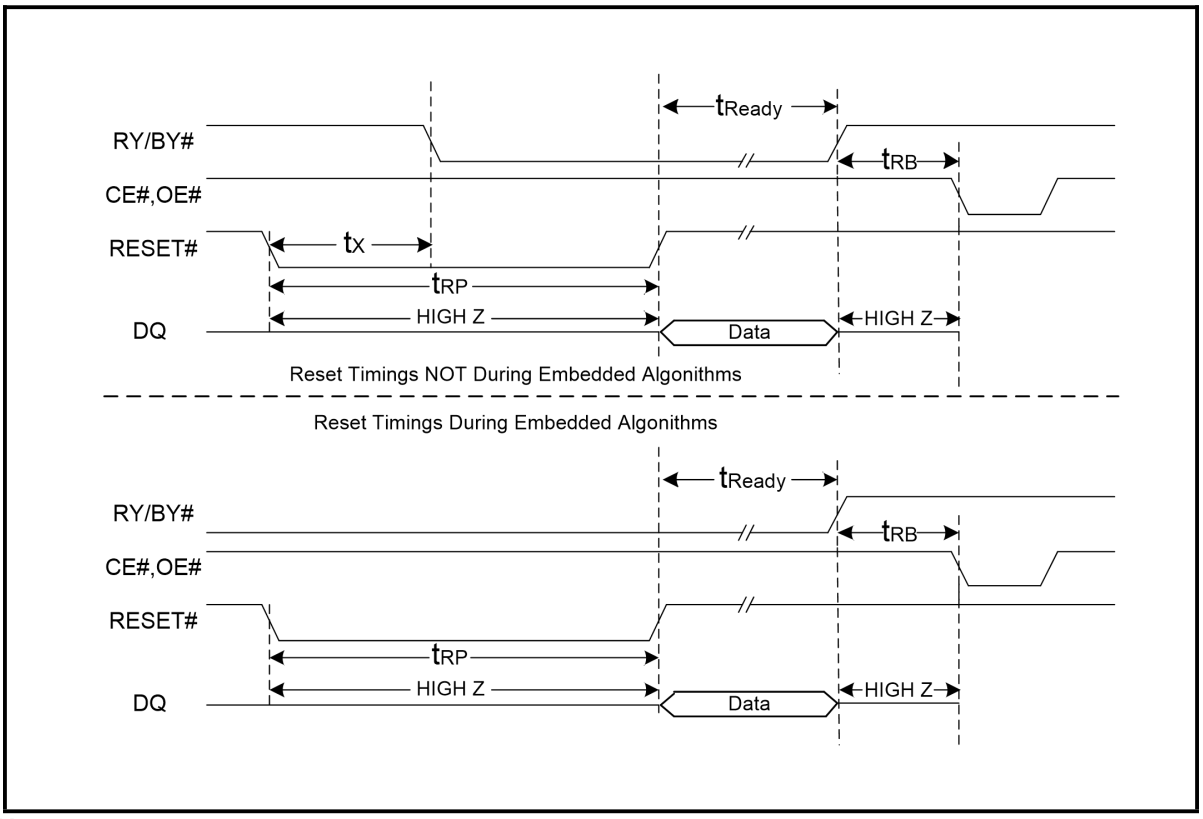
1. *Typical program and erase times assume the following conditions: 25°C, 3.6 V V_{CC}, 10,000 cycles, checkerboard pattern.*
2. *Under worst case conditions of -40°C, V_{CC} = 3.0 V, 100,000 cycles.*
3. *Effective write buffer specification is based upon a 32-word write buffer operation.*
4. *In the pre-programming step of the Embedded Erase algorithm, all bits are programmed to 00h before erasure.*
5. *System-level overhead is the time required to execute the two- or four-bus-cycle sequence for the program instruction.*

6.7.6 Hardware Reset (RESET#) Operation

Hardware Reset (RESET#)

Parameter		Description		Speed	Unit
JEDEC	Std.				
	t_{Ready}	RESET# Pin High (During Embedded Algorithms) to the end of Reset	Max	100	μs
	t_{Ready}	RESET# Pin High (NOT During Embedded Algorithms) to the end of Reset	Max	100	μs
	t_{RP}	RESET# Pulse Width	Min	3	μs
	t_{RB}	RY/BY# Recovery Time	Min	0	ns
	t_X	RESET# Pin Low (NOT During Embedded Algorithms) to RY/BY# Low	Max	3	μs

Figure 100. Reset Timings



Note

1. *DQ: If the OE # pin is pulled down for Read operation after RESET # pin is pulled up and before the reset is completed, the Data after each reset is random, and this random value is output in cycles.*

Power-up Sequence Timings

Parameter	Description	Speed		Unit
		Min	Max	
t_{VCS}	Reset Low Time from rising edge of V_{CC} (or last Reset pulse) to falling edge of CE#	100		μs
t_{VIOS}	Reset Low Time from rising edge of V_{IO} (or last Reset pulse) to falling edge of CE#	100		μs
V_{LKO}	Write Inhibit Threshold Voltage V_{LKO}	2.3	2.5	V

Note

1. *V_{IO} < V_{CC} + 200 mV.*
2. *V_{IO} and V_{CC} ramp must be synchronized during power up.*
3. *If RESET# is not stable for t_{VCS} or t_{VIOS}:*
   The device does not permit any read and write operations.
   A valid read operation returns FFh.
   A hardware reset is required.
4. *V_{CC} maximum power-up current (RST=V_{IL}) is 20 mA.*

Figure 101. Power-up Sequence Timings

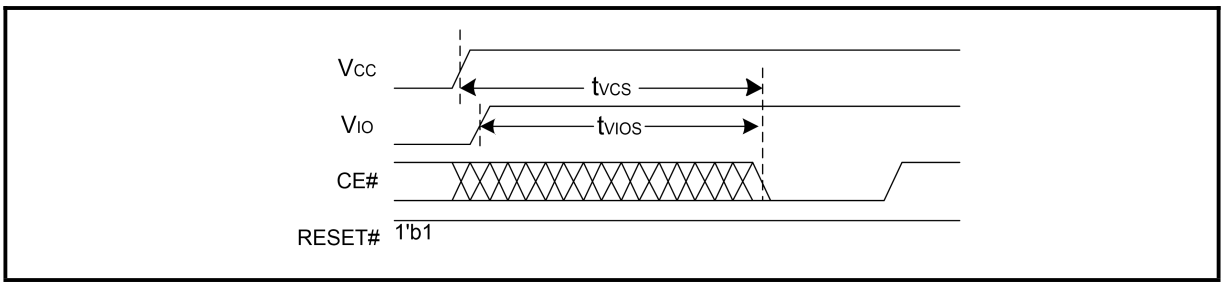
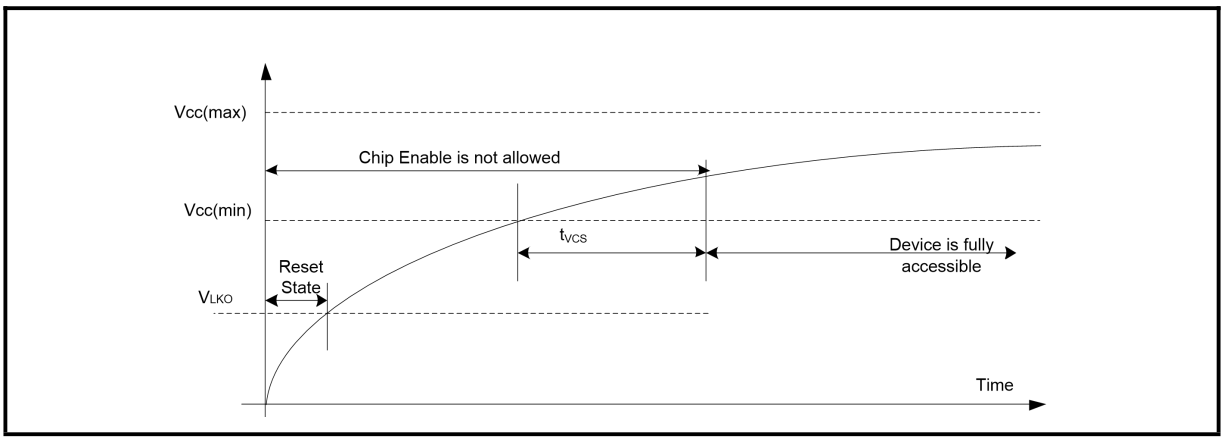


Figure 102. Power-up Timing and Voltage Levels



6.7.7 TSOP Pin and BGA Package Capacitance

Package Capacitance

Parameter Symbol	Parameter Description	Test Setup	Typ	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	10	12	pF
C_{IN2}	Control Pin Capacitance	V_{IN} = 0	8	10	pF
WP#/ACC	Separated Control Pin	V_{IN} = 0	42	45	pF
RESET#	Separated Control Pin	V_{IN} = 0	25	28	pF
CE#	Separated Control Pin	V_{IN} = 0	22	25	pF

Note

1. *Sampled, not 100% tested.*
2. *Test conditions TA = 25°C, f = 100 MHz.*

7. APPENDIX

7.1 CFI Query Identification String

Addresses (x16)	Addresses (x8)	Data	Description
10h 11h 12h	20h 22h 24h	0051h 0052h 0059h	Query Unique ASCII string “QRY”
13h 14h	26h 28h	0002h 0000h	Primary OEM Instruction Set
15h 16h	2Ah 2Ch	0040h 0000h	Address for Primary Extended Table
17h 18h	2Eh 30h	0000h 0000h	Alternate OEM Instruction Set (00h = none exists)
19h 1Ah	32h 34h	0000h 0000h	Address for Alternate OEM Extended Table (00h = none exists)

7.2 System Interface String

Addresses (x16)	Addresses (x8)	Data	Description
1Bh	36h	0027h	V_{CC} Min. (write/erase) D7–D4: volt, D3–D0: 100 mV
1Ch	38h	0036h	V_{CC} Max. (write/erase) D7–D4: volt, D3–D0: 100 mV
1Dh	3Ah	0000h	V_{PP} Min. voltage (00h = no V_{PP} pin present)
1Eh	3Ch	0000h	V_{PP} Max. voltage (00h = no V_{PP} pin present)
1Fh	3Eh	0006h	Typical timeout per single byte/word write 2^N µs
20h	40h	0006h	Typical timeout for buffer write 2^N µs (00h = not supported)
21h	42h	0009h	Typical timeout per individual block erase 2^N ms
22h	44h	0012h = 512 Mb	Typical timeout for full chip erase 2^N ms (00h = not supported)
23h	46h	0003h	Max. timeout for byte/word write 2^N times typical
24h	48h	0005h	Max. timeout for buffer write 2^N times typical
25h	4Ah	0003h	Max. timeout per individual block erase 2^N times typical
26h	4Ch	0002h	Max. timeout for full chip erase 2^N times typical (00h = not supported)

7.3 Device Geometry Definition

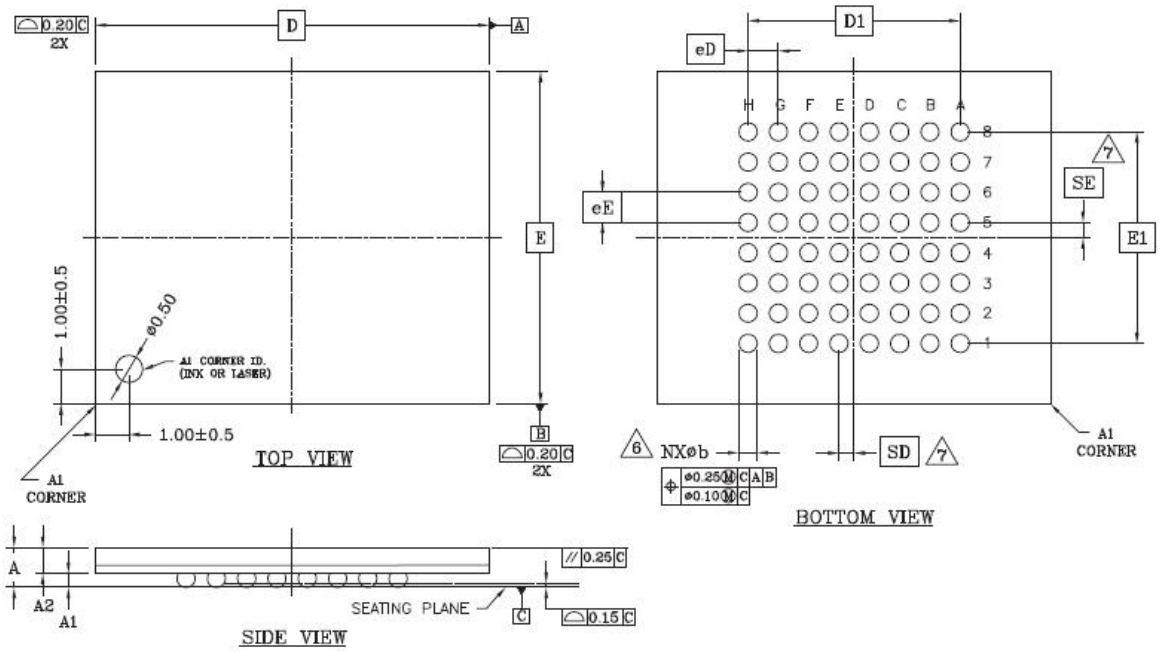
Addresses (x16)	Addresses (x8)	Data	Description
27h	4Eh	001Ah	Device Size = 2^N byte 1A = 512Mb
28h 29h	50h 52h	0002h 0000h	Flash Device Interface description (refer to CFI publication 100)
2Ah 2Bh	54h 56h	0006h 0000h	Max. number of byte in multi-byte write = 2^N (00h = not supported)
2Ch	58h	0001h	Number of Erase Block Regions within device (01h = uniform device, 02h = boot device)
2Dh 2Eh 2Fh 30h	5Ah 5Ch 5Eh 60h	00xxh 000xh 0000h 000xh	Erase Block Region 1 Information (refer to the CFI specification or CFI publication 100) 00FFh, 0001h, 0000h, 0002h =512 Mb
31h 32h 33h 34h	62h 64h 66h 68h	0000h 0000h 0000h 0000h	Erase Block Region 2 Information (refer to CFI publication 100)
35h 36h 37h 38h	6Ah 6Ch 6Eh 70h	0000h 0000h 0000h 0000h	Erase Block Region 3 Information (refer to CFI publication 100)
39h 3Ah 3Bh 3Ch	72h 74h 76h 78h	0000h 0000h 0000h 0000h	Erase Block Region 4 Information (refer to CFI publication 100)

7.4 Primary Vendor-Specific Extended Query

Addresses (x16)	Addresses (x8)	Data	Description
40h 41h 42h	80h 82h 84h	0050h 0052h 0049h	Query-unique ASCII string “PRI”
43h	86h	0031h	Major version number, ASCII
44h	88h	0033h	Minor version number, ASCII
45h	8Ah	0014h	Address Sensitive Unlock (Bits 1-0) 0 = Required, 1 = Not Required Process Technology (Bits 7-2) 0101b = ETOX 50 nm
46h	8Ch	0002h	Erase Suspend 0 = Not Supported, 1 = To Read Only, 2 = To Read & Write
47h	8Eh	0001h	Sector Protect 0 = Not Supported, X = Number of sectors in per group
48h	90h	0000h	Sector Temporary Unprotect 00 = Not Supported, 01 = Supported
49h	92h	0008h	Sector Protect/Unprotect scheme 0008h = Advanced Sector Protection
4Ah	94h	0000h	Simultaneous Operation 00 = Not Supported, X = Number of Sectors
4Bh	96h	0000h	Burst Mode Type 00 = Not Supported, 01 = Supported
4Ch	98h	0002h	Page Mode Type 00 = Not Supported, 01 = 4 Word Page, 02 = 8 Word Page
4Dh	9Ah	00B5h	ACC (Acceleration) Supply Minimum 00h = Not Supported, D7-D4: Volt, D3-D0: 100 mV
4Eh	9Ch	00C5h	ACC (Acceleration) Supply Maximum 00h = Not Supported, D7-D4: Volt, D3-D0: 100 mV
4Fh	9Eh	00xxh	WP# Protection 04h = Uniform sectors bottom WP# protect, 05h = Uniform sectors top WP# protect
50h	A0h	0001h	Program Suspend 00h = Not Supported, 01h = Supported

8. PACKAGE INFORMATION

8.1 TFBGA11*13-64BALL



PACKAGE	LAA 064			
JEDEC	N/A			
	13.00 mm x 11.00 mm PACKAGE			
SYMBOL	MIN	NOM	MAX	NOTE
A	---	---	1.40	PROFILE HEIGHT
A1	0.40	---	---	STANDOFF
A2	0.60	---	---	BODY THICKNESS
D		13.00 BSC.		BODY SIZE
E		11.00 BSC.		BODY SIZE
D1		7.00 BSC.		MATRIX FOOTPRINT
E1		7.00 BSC.		MATRIX FOOTPRINT
MD		8		MATRIX SIZE D DIRECTION
ME		8		MATRIX SIZE E DIRECTION
N		64		BALL COUNT
ϕb	0.50	0.60	0.70	BALL DIAMETER
eD		1.00 BSC.		BALL PITCH - D DIRECTION
eE		1.00 BSC.		BALL PITCH - E DIRECTION
SD / SE		0.50 BSC.		SOLDER BALL PLACEMENT
		NONE		DEPOPULATED SOLDER BALLS

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JESD 95-1, SPP-010 (EXCEPT AS NOTED).
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL ROW MATRIX SIZE IN THE "D" DIRECTION.

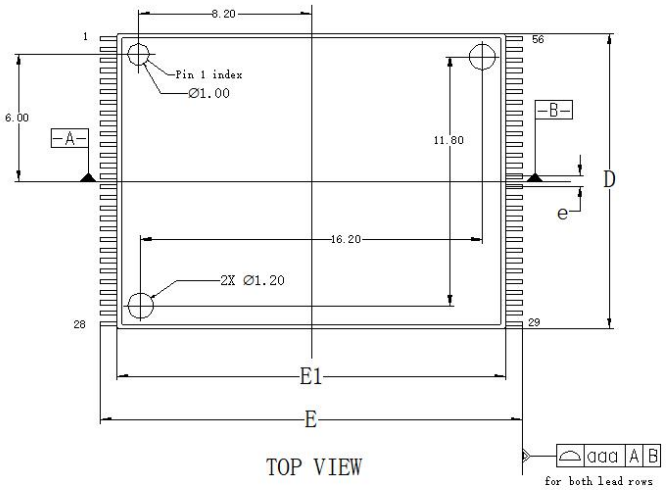
   SYMBOL "ME" IS THE BALL COLUMN MATRIX SIZE IN THE "E" DIRECTION.

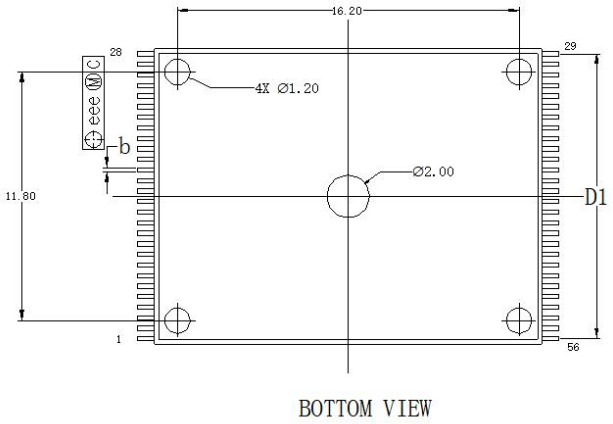
   N IS THE TOTAL NUMBER OF SOLDER BALLS.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.

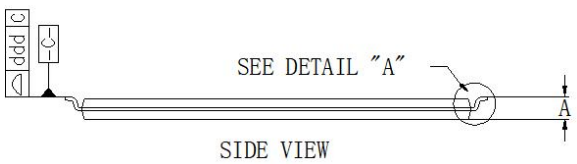
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW PARALLEL TO THE D OR E DIMENSION, RESPECTIVELY, SD OR SE = 0.000.

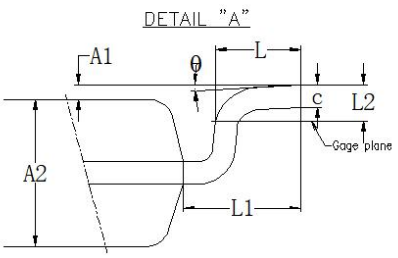
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = e/2
8. NOT USED.
9. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.

8.2 TSOP56 14*20mm







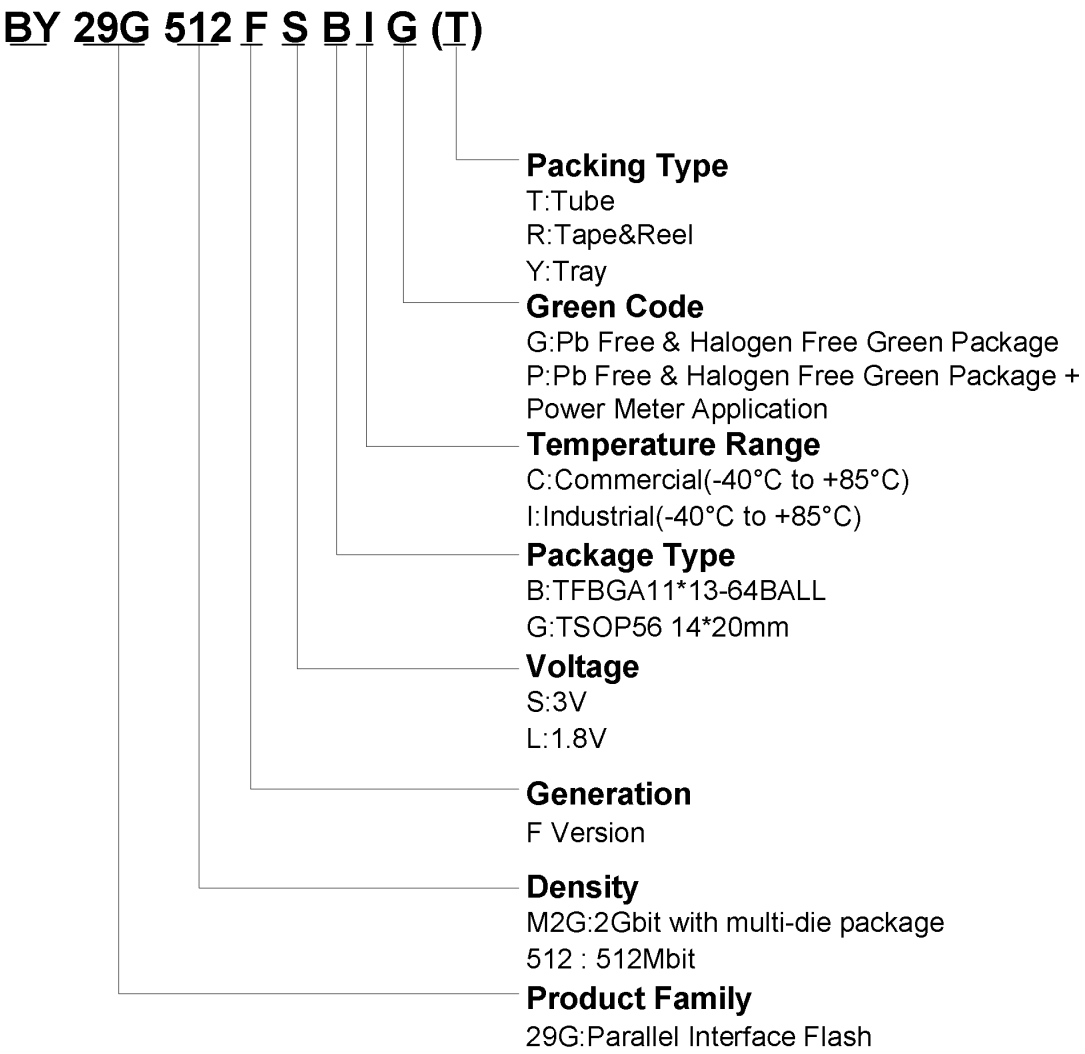


SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	---	---	1.20
A1	0.05	0.10	0.15
A2	0.95	1.00	1.05
b	0.17	0.22	0.27
c	0.10	---	0.21
D	13.90	14.00	14.10
E1	18.30	18.40	18.50
D1	---	13.50	---
E	19.80	20.00	20.20
e	0.50 BSC		
L 03	0.50	0.60	0.70
L1	---	0.80	---
L2	---	0.25	---
q	0°	---	8°
aaa	---	---	0.25
ddd	---	---	0.10
eee	---	---	0.08
n	56		

NOTES:

1. DIMENSION D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
2. MAXIMUM MOLD PROTRUSION 0.15(.006) PER SIDE.
3. DIMENSION b DOES NOT INCLUDE DAM BAR PROTRUSION. ALLOWABLE DAM BAR PROTRUSION SHALL BE 0.08(.003) 03 TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.

9. ORDER INFORMATION



10. VALID PART NUMBERS AND TOP SIDE MARKING

The following table provides the valid part numbers for BY29G512FS Parallel Flash Memory. Pls contact BY Technology for specific availability by density and package type.

For consumer and industry application:

Package Type	Density	Product Number	Top Side Marking
B TFBGA 11*13mm-64BALL	512M-bit	BY29G512FSBIG	BYT 29G512FSBIG YYWW
G TSOP56 14*20mm	512M-bit	BY29G512FSGIG	BYT 29G512FSGIG YYWW

10.1 Minimum Packing Quantity (MPQ)

Package Type	Packing Type	Qty for 1 Tube or Reel	Vacuum bag/ Inner Box	MPQ
TFBGA 11*13mm-64BALL	Tray	152ea/Tray	10+1 Trays/Bag 1Bag/InnerBox	1520
TSOP56 14*20mm	Tray	84ea/Tray	10+1 Trays/Bag 1Bag/InnerBox	840

11. DOCUMENT CHANGE HISTORY

REVISION	CHANGE DESCRIPTION	CLAUSE	ORIGINATOR DATE
1.0	Initiate;	/	Xingyue Huang Dongfu Yan 2025-04-27