DATASHEET

FOR

1G BIT SPI NOR FLASH

BY25QM1GFS

Features

- **Serial Peripheral Interface**
  - 4×256M-bit Serial MCP Flash memory
  - Standard SPI: SCLK, /CS, SI, SO, /WP, /HOLD
  - Dual SPI: SCLK, /CS, IO0, IO1, /WP, /HOLD
  - Quad SPI: SCLK, /CS, IO0, IO1, IO2, IO3
  - QPI: SCLK, /CS, IO0, IO1, IO2, IO3
  - DTR (Double Transfer Rate) Read
  - 3 or 4-Byte Addressing Mode
- **Read**
  - Normal Read (Serial): 55MHz clock rate
  - Fast Read (Serial): 100MHz clock rate with 30PF load
  - Dual I/O data transfer up to 200Mbits/S
  - Quad I/O & QPI data transfer up to 400Mbits/S
  - DTR Quad I/O Data transfer up to 400Mbits/s
  - Allows XIP (execute in place) Operation: Continuous Read with 8/16/32/64-byte Wrap
- **Program**
  - Serial-input Page Program up to 256bytes
  - Program Suspend and Resume
- **Erase**
  - Block Erase (64/32 KB)
  - Sector Erase (4 KB)
  - Chip Erase
  - Erase Suspend and Resume
- **Program/Erase Speed**
  - Page Program time: 0.6ms typical
  - Sector Erase time: 50ms typical
  - Block Erase time: 0.15/0.25s typical
  - Chip Erase time: 80s typical
- **Flexible Architecture**
  - Sector of 4K-byte
  - Block of 32/64K-byte
- **Low Power Consumption**
  - 20mA maximum active current
  - 60uA maximum power down current
- **Software/Hardware Write Protection**
  - Single Die BY25Q256FS 3x512-Byte Security Registers with OTP Locks
  - Discoverable Parameters (SFDP) register
  - Enable/Disable protection with /WP Pin
  - Top/Bottom, Complement array protection
  - Advanced Block/Sector Protection (Solid and Password Protect)
- **Single Supply Voltage**
  - Full voltage range: 2.7~3.6V
- **Temperature Range**
  - Commercial (-40℃ to +85℃)
  - Industrial (-40℃ to +85℃)
- **Cycling Endurance/Data Retention**
  - Typical 100k Program-Erase cycles on any sector
  - Typical 20-year data retention

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1. Description

The BY25QM1GFS is (4×256M-bit) Serial MCP (Multi Chip Package) Flash memory is based on the popular BY25Q series by stacking four indsividual BY25Q256FS die into a standard 16-pin or 24-ball package. It offers the highest memory density for the low pin-count package, as well as Concurrent Operations in Serial Flash memory for the first time. The BY25QM1GFS is ideal for small form factor system designs, and applications that demand high Program/Erase data throughput.

The BY25QM1GFS introduces a new “Software Die Select (C2h)” instruction, and a factory assigned “Die ID#” for each stacked die. Each BY25Q256FS die can be accessed independently even though the interface is shared. The BY25QM1GFS only allows a single die to be Active and have control of the SPI interface at any given time to avoid bus contention.

The BY25QM1GFS supports the Dual/Quad SPI: Serial Clock, Chip Select, Serial Data I/O0 (SI), I/O1 (SO), I/O2 (/WP), and I/O3 (/HOLD), Reset; and supports the QPI: Serial Clock, Chip Select, I/O0, I/O1, I/O2, and I/O3, Reset; The Dual I/O data is transferred with speed of 200Mbits/s and the Quad I/O & Quad output & QPI data is transferred with speed of 400Mbits/s. The Double Transfer Rate (DTR) Read is transferred with speed of 400Mbits/s. The device uses a single low voltage power supply, ranging from 2.7 Volt to 3.6 Volt.

Additionally, the device supports JEDEC standard manufacturer and device ID and three 512-bytes Security Registers 64-bit Unique ID for individual die.

In order to meet environmental requirements, BY Technology offers 24-ball TFBGA8*6mm (5*5 ball array), and other special-order packages, please contacts BY Technology for ordering information.

Figure 1. Logic diagram

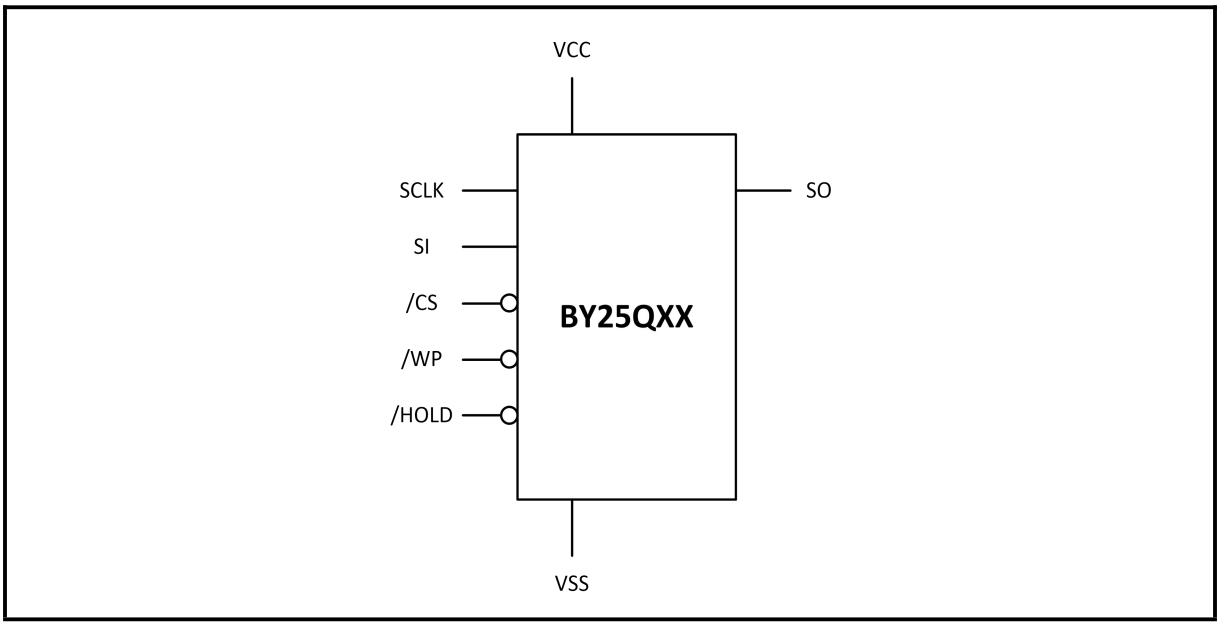
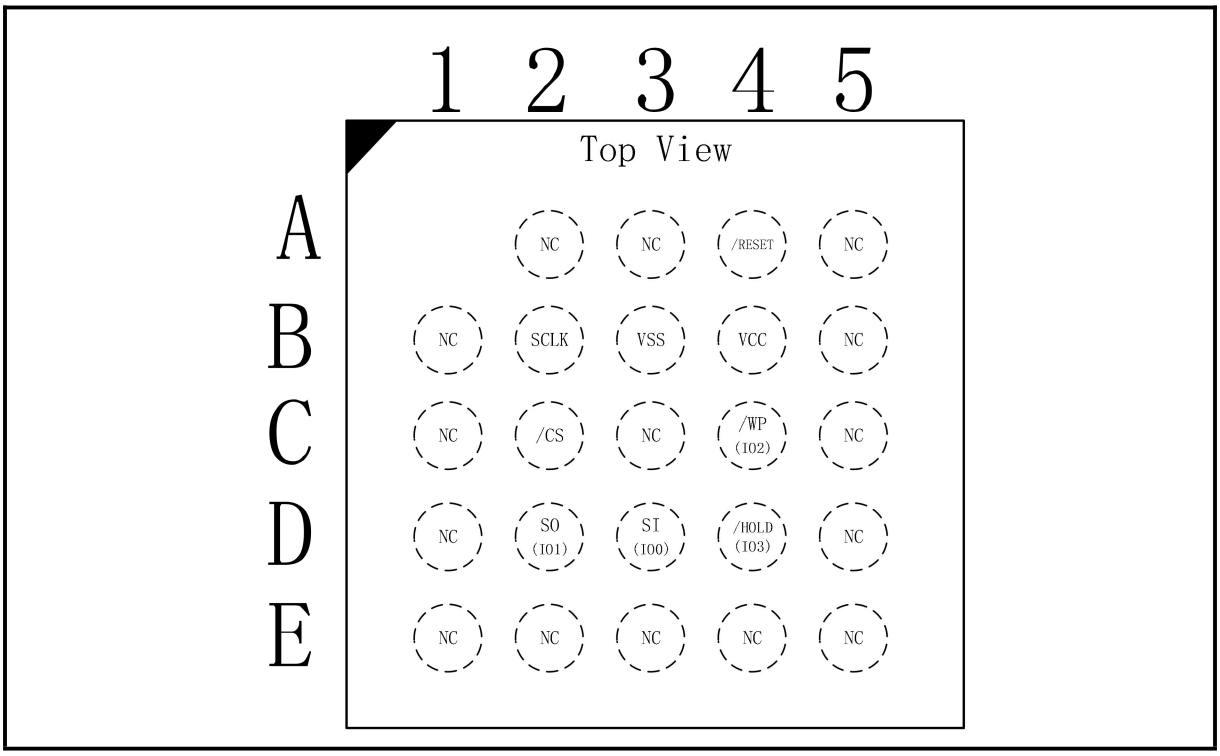


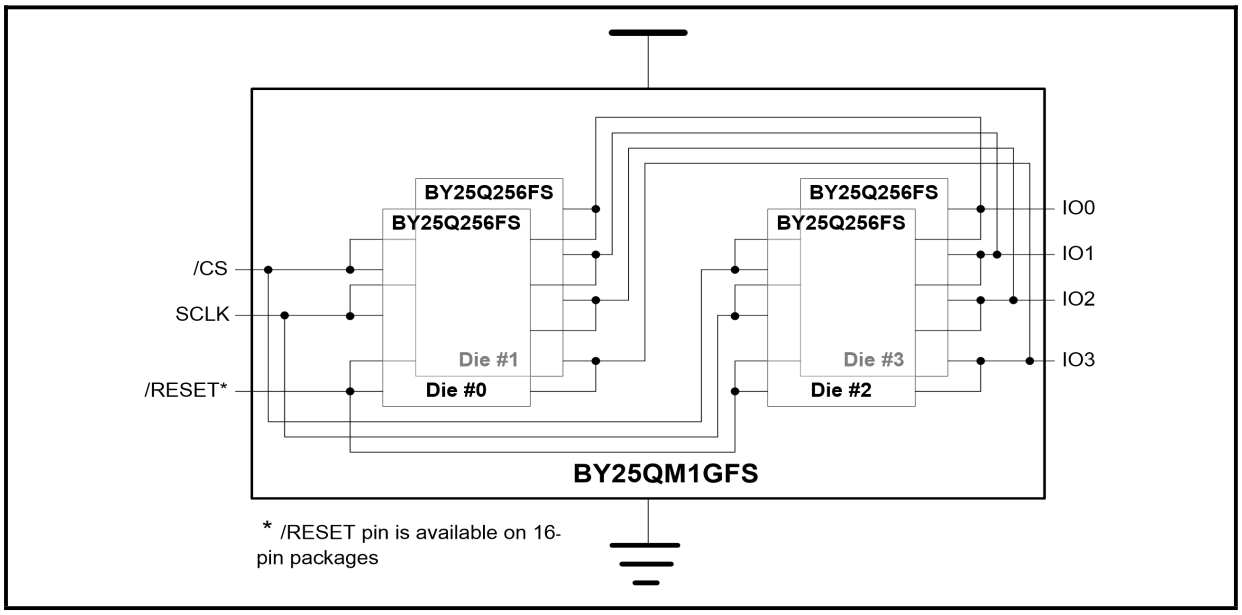
Figure 2. Pin Configuration 24-BALL TFBGA 8*6mm (5x5 ball array)



2. Signal Description

2.1 Serial MCP Device Configuration

Figure 4. BY25QM1GFS Device Configuration



All signal pins are shared by the stacked dies within the package. Each die is assigned a “Die ID#” in the factory. Only a single die is active at any given time, and have the control of the SPI bus to communicate with the external SPI controller. However, all the dies will accept two instructions regardless their Active or Idle status: 1) “Software Die Select (C2h)” instruction; it is used to set any single die to be active according to the 8-bit Die ID following the instruction. 2) “Software Reset (66h + 99h)” instruction & Hardware Reset; it is used to reset all the stacked dies to their power-up state.

During all operations, VCC must be held stable and within the specified valid range: VCC (min) to VCC (max).

All of the input and output signals must be held High or Low (according to voltages of VIH, VOH, VIL or VOL, see ***DC Electrical Characteristics***). These signals are described next.

2.2 Input/Output Summary

Table 1. Signal Names

Pin Name	I/O	Description
/CS	I	Chip Select
SO (IO1)	I/O	Serial Output for single bit data Instructions. IO1 for Dual or Quad Instructions
/WP (IO2)	I/O	Write Protect in single bit or Dual data Instructions. IO2 in Quad mode. The signal has an internal pull-up resistor and may be left unconnected in the host system if not used for Quad Instructions
VSS		Ground
SI (IO0)	I/O	Serial Input for single bit data Instructions. IO0 for Dual or Quad Instructions
SCLK	I	Serial Clock
/HOLD/RESET (IO3)(1)	I/O	Hold (pause) serial transfer in single bit or Dual data Instructions when QE=0, HOLD/RST=0. IO3 in Quad-I/O/QPI mode. Also can be configured either as a /RESET pin when QE=0, HOLD/RST=1. The signal has an internal pull-up resistor and may be left unconnected in the host system if not used for Quad Instructions
/RESET(1)	I	Reset input
VCC		Core and I/O Power Supply

Notes:
1. Two reset functions exist in 16-pin packages at the same time

2.3 Chip Select (/CS)

The chip select signal indicates when an instruction for the device is in process and the other signals are relevant for the memory device. When the /CS signal is at the logic high state, the device is not selected and all input signals are ignored and all output signals are high impedance. Unless an internal Program, Erase or Write Status Registers embedded operation is in progress, the device will be in the Standby Power mode. Driving the /CS input to logic low state enables the device, placing it in the Active Power mode. After Power Up, a falling edge on /CS is required prior to the start of any instruction.

2.4 Serial Clock (SCLK)

This input signal provides the synchronization reference for the SPI interface. Instructions, addresses, or data input are latched on the rising edge of the SCLK signal. Data output changes after the falling edge of SCLK.

2.5 Serial Input (SI)/IO0

This input signal is used to transfer data serially into the device. It receives instructions, addresses, and data to be programmed. Values are latched on the rising edge of serial SCLK clock signal.

SI becomes IO0 an input and output during Dual and Quad Instructions for receiving instructions, addresses, and data to be programmed (values latched on rising edge of serial SCLK clock signal) as well as shifting out data (on the falling edge of SCLK).

2.6 Serial Data Output (SO)/IO1

This output signal is used to transfer data serially out of the device. Data is shifted out on the falling edge of the serial SCLK clock signal.

SO becomes IO1 an input and output during Dual and Quad Instructions for receiving instructions, addresses, and data to be programmed (values latched on rising edge of serial SCLK clock signal) as well as shifting out data (on the falling edge of SCLK).

2.7 Write Protect (/WP)/IO2

When /WP is driven Low (VIL), while the Status Register Protect bits (SRP1 and SRP0) of the Status Registers (SR2[0] and SR1[7]) are set to 0 and 1 respectively, it is not possible to write to the Status Registers. This prevents any alteration of the Status Registers. As a consequence, all the data bytes in the memory area that are protected by the Block Protect, BP4, BP3 bits in the status registers, are also hardware protected against data modification while /WP remains Low. The /WP function is not available when the Quad mode is enabled (QE) in Status Register 2 (SR2[1]=1).

The /WP function is replaced by IO2 for input and output during Quad mode for receiving addresses, and data to be programmed (values are latched on rising edge of the SCLK signal) as well as shifting out data (on the falling edge of SCLK). /WP has an internal pull-up resistance; when unconnected; /WP is at VIH and may be left unconnected in the host system if not used for Quad mode.

2.8 HOLD (/HOLD) /RESET /IO3

The /HOLD function is only available when QE=0, which can be configured either as a /HOLD pin or as a /RESET pin depending on Status Register setting. If QE=1, the /HOLD function is disabled, the pin acts as dedicated data I/O pin, and the /HOLD or /RESET function is not available.

When QE=0 and HOLD/RES= 0, the /HOLD signal goes low to stop any serial communications with the device, but doesn't stop the operation of write status register, programming, or erasing in progress.

The operation of HOLD, need /CS keep low, and starts on falling edge of the /HOLD signal, with SCLK signal being low (if SCLK is not being low, HOLD operation will not start until SCLK being low). The HOLD condition ends on rising edge of /HOLD signal with SCLK being low (If SCLK is not being low, HOLD operation will not end until SCLK being low).

2.9 RESET

The /RESET pin in 16-pin packages allows the device to be reset by the controller.

2.10 VCC Power Supply

VCC is the supply voltage. It is the single voltage used for all device functions including read, program, and erase.

2.11 VSS Ground

VSS is the reference for the VCC supply voltage.

3. Block/Sector Addresses

Table 2. Single Die (BY25Q256FS) Block/Sector Addresses of BY25QM1GFS

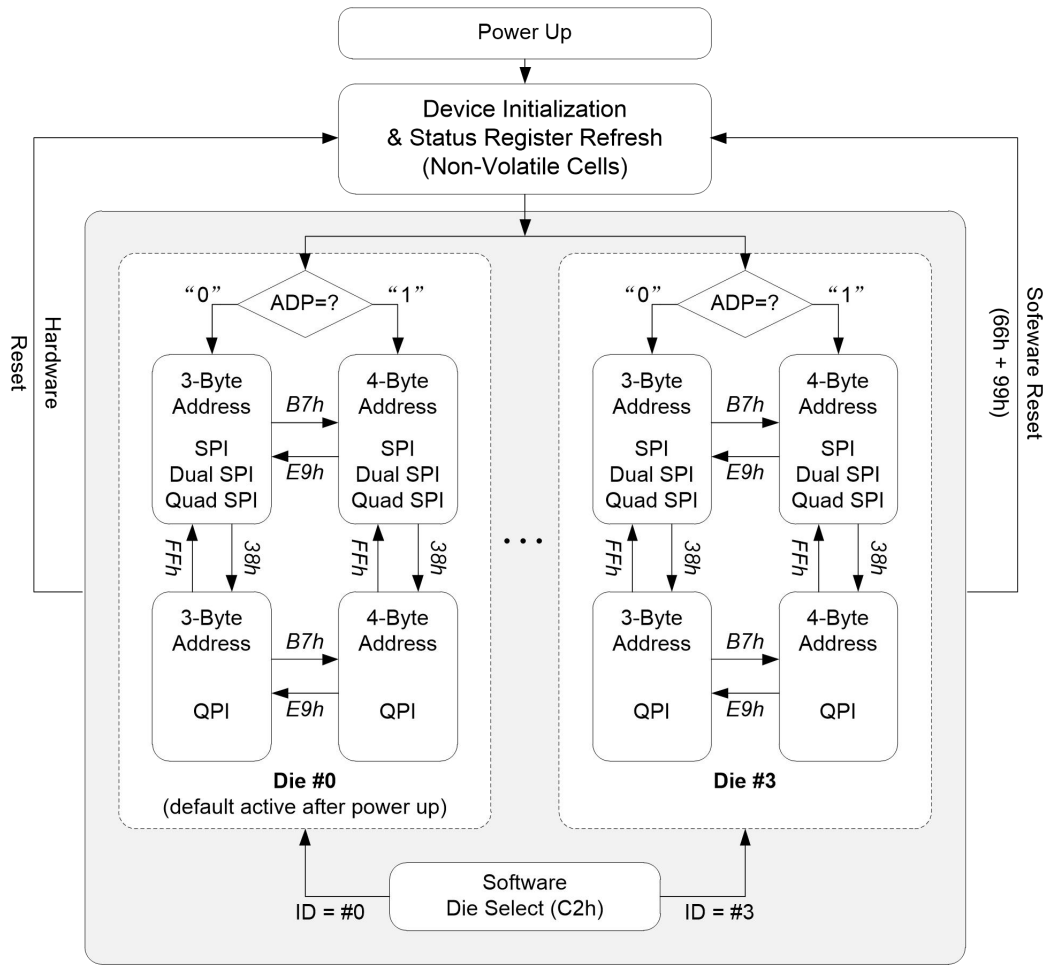
Memory Density	Big Block (4M bit)	Block (64k byte)	Block (32k byte)	Sector No.	Sector Size (KB)	Address range
256Mbit	Big Block 0	Block 0	Half block 0	Sector 0	4	0000000h-0000FFFh
				:	:	:
				Sector 7	4	0007000h-0007FFFh
			Half block 1	Sector 8	4	0008000h-0008FFFh
				:	4	:
				Sector 15	4	000F000h-000FFFFh
		:	:	:	:	:
		Block 7	Half block 14	Sector 112	4	0070000h-0070FFFh
				:	:	:
				Sector 119	4	0077000h-0077FFFh
			Half block 15	Sector 120	4	0078000h-0078FFFh
				:	:	:
				Sector 127	4	007F000h-007FFFFh
	:	:	:	:	:	:
	Big Block 63	Block 504	Half block 1008	Sector 8064	4	1F80000h-1F80FFFh
				:	:	:
				Sector 8071	4	1F87000h-1F87FFFh
			Half block 1009	Sector 8072	4	1F88000h-1F88FFFh
				:	:	:
				Sector 8079	4	1F8F000h-1F8FFFFh
		:	:	:	:	:
		Block 511	Half block 1022	Sector 8176	4	1FF0000h-1FF0FFFh
				:	:	:
				Sector 8183	4	1FF7000h-1FF7FFFh
			Half block 1023	Sector 8184	4	1FF8000h-1FF8FFFh
				:	:	:
				Sector 8191	4	1FFF000h-1FFFFFFh

Notes:

1. Big Block = Uniform Big Block, and the size is 4M bits.
2. Block = Uniform Block, and the size is 64K bytes.
3. Half block = Half Uniform Block, and the size is 32k bytes.
4. Sector = Uniform Sector, and the size is 4K bytes.

4. SPI/QPI Operation

Figure 5. BY25QM1GFS Serial Flash Memory Operation Diagram



Note: ADP bit in the Status Register is only used to determine 3-byte or 4-byte Address Modes during power up. Changing ADP bit value will not switch the address modes during normal operation.

4.1 Stacked Die Operations

Once the device is power on, Die #0 will be active and have control of the SPI bus. "Software Die Select (C2h)" instruction followed by the 8-bit Die ID can be used to select the active die. The active die is available to accept any instruction issued by the controller and perform specific operations. The inactive/idle die does not accept any other instructions except the "Software Die Select (C2h)", "Software Reset (66h + 99h)" and Hardware Reset. However, the inactive/idle die can still perform internal Program/Erase operation which was initiated when the die was active. Therefore, "Read (on Active die) while Program/Erase (on Idle die)" and "Multi-die Program/Erase (both Active & Idle dies)" concurrent operations are feasible in the BY25QM1GFS. "Software Die Select (C2h)" instruction will only change the active/idle status of the stacked dies, and it will not interrupt any on-going Program/Erase operations.

Because the device working modes (SPI, QPI) of Die #0 to Die #3 may be different when selecting the active die, it is necessary to adopt different "Software Die Select (C2h)" instruction sending methods according to the specific situation, which is shown in ***Table 3***.

Table 3. Instructions for using Software Die Select instruction in different modes

Situation	Description	Operation
SPI→SPI	Select from active Die# in SPI mode to inactive/idle Die# in SPI mode.	1. Send "Software Die Select (C2h)" instruction directly in SPI mode followed by the 8-bit Die ID (inactive/idle Die# in SPI mode).
SPI→QPI	Select from active Die# in SPI mode to inactive/idle Die# in QPI mode.	1. Send "Software Die Select (C2h)" instruction in SPI mode followed by the 8-bit Die ID (inactive/idle Die# in QPI mode). 2. Send "Software Die Select (C2h)" instruction in QPI mode followed by the 8-bit Die ID (inactive/idle Die# in QPI mode).
QPI→SPI	Select from active Die# in QPI mode to inactive/idle Die# in SPI mode.	1. Send "Software Die Select (C2h)" instruction in QPI mode followed by the 8-bit Die ID (inactive/idle Die# in SPI mode). 2. Send "Software Die Select (C2h)" instruction in SPI mode followed by the 8-bit Die ID (inactive/idle Die# in SPI mode).
QPI→QPI	Select from active Die# in QPI mode to inactive/idle Die# in QPI mode.	1. Send "Software Die Select (C2h)" instruction directly in QPI mode followed by the 8-bit Die ID (inactive/idle Die# in QPI mode).

Because the "Software Reset (66h + 99h)" instruction cannot be accepted at the same time in different working modes (SPI, QPI), in order to correctly reset all Die#, please send the "Software Reset (66h + 99h)" instruction according to the methods shown in ***Table 4***.

Table 4. Instructions for using Software Die Select instruction in different modes

Situation	Description	Operation
(SPI,SPI)	All Die# in SPI mode.	1. Send "Software Reset (66h + 99h)" instruction directly in SPI mode.
(SPI,QPI)	One or more Die# in SPI mode and the other Die# in QPI mode.	1. Send "Software Reset (66h + 99h)" instruction directly in SPI mode to reset Die# in SPI mode. 2. Send "Software Reset (66h + 99h)" instruction directly in QPI mode to reset the other Die# in QPI mode.
(QPI,QPI)	All Die# in QPI mode.	1. Send "Software Reset (66h + 99h)" instruction directly in QPI mode.

Because the Hardware Reset mode of /HOLD Pin cannot be used when QE bit=1 or HOLD/RES=0. SO when using /HOLD pin reset all Die# at the same time, please ensure QE bit=0 and HOLD/RES=1 of all Die#.

Because the Hardware Reset mode of independent /RESET pin can be used normally in all situations. Therefore, it is can to reset all Die# directly at the same time using the /RESET pin.

Because the Hardware Reset mode of JEDEC Standard Hardware Reset can be used normally in all situations. Therefore, it is can to reset all Die# directly at the same time using the JEDEC Standard Hardware Reset.

4.2 Standard SPI Instructions

The BY25QM1GFS features a serial peripheral interface on 4 signals bus: Serial Clock (SCLK), Chip Select (/CS), Serial Data Input (SI) and Serial Data Output (SO). Both SPI bus mode 0 and 3 are supported. Input data is latched on the rising edge of SCLK and data shifts out on the falling edge of SCLK.

4.3 Dual SPI Instructions

The BY25QM1GFS supports Dual SPI operation when using the “3BH”, “3CH”, “BBH”, “BDH”, “BCH”, and “92H” instructions. These instructions allow data to be transferred to or from the device at two times the rate of the standard SPI. When using the Dual SPI instruction the SI and SO pins become bidirectional I/O pins: IO0 and IO1.

4.4 Quad SPI Instructions

The BY25QM1GFS supports Quad SPI operation when using the “6BH”, “6CH”, “EBH”, “EDH”, “ECH”, “E7H”, “94H”, “32H”, and “34H” instructions. These instructions allow data to be transferred to or from the device at four times the rate of the standard SPI. When using the Quad SPI instruction the SI and SO pins become bidirectional I/O pins: IO0 and IO1, and /WP and /HOLD pins become IO2 and IO3. Quad SPI instructions require the non-volatile Quad Enable bit (QE) in Status Register to be set.

4.5 QPI Instructions

The BY25QM1GFS supports Quad Peripheral Interface (QPI) operations only when the device is switched from Standard/Dual/Quad SPI mode to QPI mode using the “Enter QPI (38h)” instruction. The typical SPI protocol requires that the byte-long instruction code being shifted into the device only via SI pin in eight serial clocks. The QPI mode utilizes all four IO pins to input the instruction code, thus only two serial clocks are required. Standard/Dual/Quad SPI mode and QPI mode are exclusive. Only one mode can be active at any given time. “Enter QPI (38h)” and “Exit QPI (FFh)” instructions are used to switch between these two modes. Upon power-up or after a software reset using “Reset (99h)” instruction or Hardware Reset, the default state of the device is Standard/Dual/Quad SPI mode. To enable QPI mode, the non-volatile Quad Enable bit (QE) in Status Register-2 is required to be set. When using QPI instructions, the SI and SO pins become bidirectional IO0 and IO1, and the /WP and /HOLD pins become IO2 and IO3 respectively. See ***Figure 5*** for the device operation modes.

4.6 3-Byte/4-Byte Address Modes

The BY25QM1GFS provides two Address Modes that can be used to specify any byte of data in the memory array. The 3-Byte Address Mode is backward compatible to older generations of serial flash memory that only support up to 128M-bit data. To address the 256M-bit or more data in 3-Byte Address Mode, Extended Address Register must be used in addition to the 3-Byte addresses.

4-Byte Address Mode is designed to support Serial Flash Memory devices from 256M-bit to 32G-bit. The extended Address Register is not necessary when the 4-Byte Address Mode is enabled.

Upon power up, the BY25QM1GFS can operate in either 3-Byte Address Mode or 4-Byte Address Mode, depending on the Non-Volatile Status Register Bit ADP (S17) setting. If ADP=0, the device will operate in 3-Byte Address Mode; if ADP=1, the device will operate in 4-Byte Address Mode. The factory default value for ADP is 0.

To switch between the 3-Byte and 4-Byte Address Modes, “Enter 4-Byte Address Mode (B7h)” or “Exit 4-Byte Address Mode (E9h)” instructions must be used. The current address mode is indicated by the Status Register Bit ADS (S16).

5. Operation Features

5.1 Supply Voltage

5.1.1 Operating Supply Voltage

Prior to selecting the memory and issuing instructions to it, a valid and stable VCC voltage within the specified [VCC(min), VCC(max)] range must be applied (see ***Electrical Characteristic***). In order to secure a stable DC supply voltage, it is recommended to decouple the VCC line with a suitable capacitor (usually of the order of 10*nF* to 100*nF*) close to the VCC/VSS package pins. This voltage must remain stable and valid until the end of the transmission of the instruction and, for a Write instruction, until the completion of the internal write cycle (tW).

5.1.2 Power-up Conditions

When the power supply is turned on, VCC rises continuously from VSS to VCC. During this time, the Chip Select (/CS) line is not allowed to float but should follow the VCC voltage, it is therefore recommended to connect the /CS line to VCC via a suitable pull-up resistor.

In addition, the Chip Select (/CS) input offers a built-in safety feature, as the /CS input is edge sensitive as well as level sensitive: after power-up, the device does not become selected until a falling edge has first been detected on Chip Select (/CS). This ensures that Chip Select (/CS) must have been High, prior to going Low to start the first operation.

5.1.3 Device Reset

In order to prevent inadvertent Write operations during power-up (continuous rise of VCC), a power on reset (POR) circuit is included. At Power-up, the device does not respond to any instruction until VCC has reached the power on reset threshold voltage (this threshold is lower than the minimum VCC operating voltage defined in ***Power-up Timing***).

When VCC is lower than V_{WI}, the device is reset.

5.1.4 Power-down

At Power-down (continuous decrease in VCC), as soon as VCC drops from the normal operating voltage to below the power on reset threshold voltage(V_{WI}), the device stops responding to any instruction sent to it. During Power-down, the device must be deselected (Chip Select (/CS) should be allowed to follow the voltage applied on VCC) and in Standby Power mode (that is there should be no internal Write cycle in progress).

5.2 Active Power and Standby Power Modes

When Chip Select (/CS) is Low, the device is selected, and in the Active Power mode. The device consumes ICC.

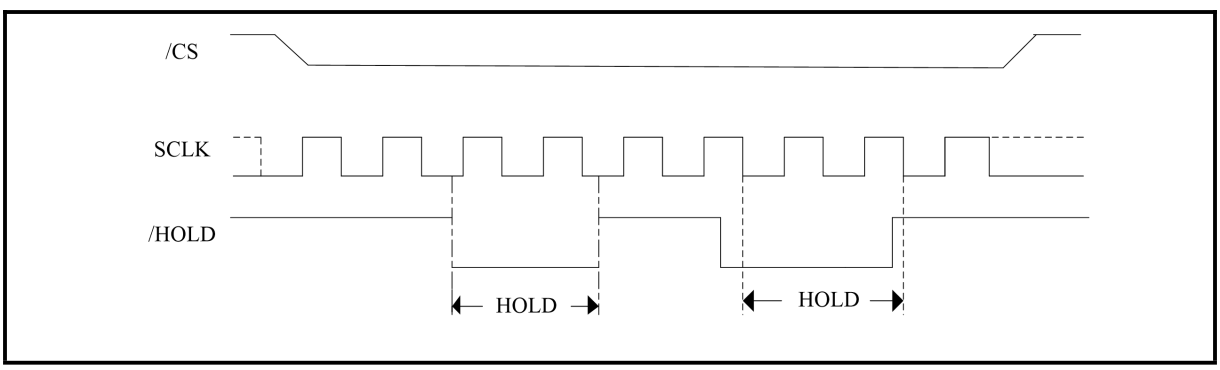
When Chip Select (/CS) is High, the device is deselected. If a Write cycle is not currently in progress, the device then goes in to the Standby Power mode, and the device consumption drops to ICC1.

5.3 Hold Condition

When QE=0, HOLD/RST=0, the Hold (/HOLD) signal is used to pause any serial communications with the device without resetting the clocking sequence. During the Hold condition, the Serial Data Output (SO) is high impedance, and Serial Data Input (SI) and Serial Clock (SCLK) are Don't Care. To enter the Hold condition, the device must be selected, with Chip Select (/CS) Low. Normally, the device is kept selected, for the whole duration of the Hold condition. Deselecting the device while it is in the Hold condition, has the effect of resetting the state of the device, and this mechanism can be used if it is required to reset any processes that had been in progress.

The Hold condition starts when the Hold (/HOLD) signal is driven Low at the same time as Serial Clock (SCLK) already being Low (as shown in ***Figure 6***).The Hold condition ends when the Hold (HOLD) signal is driven High at the same time as Serial Clock (C) already being Low. ***Figure 6*** also shows what happens if the rising and falling edges are not timed to coincide with Serial Clock (SCLK) being Low.

Figure 6. Hold condition activation



5.4 Software Reset & Hardware RESET

5.4.1 Software Reset

The BY25QM1GFS can be reset to the initial power-on state by a software reset sequence, either in SPI mode or QPI mode. This sequence must include two consecutive instructions: Enable Reset (66h) & Reset (99h). If the instruction sequence is successfully accepted, the device will take approximately 300uS (tRST) to reset. No instruction will be accepted during the reset period.

5.4.2 Hardware Reset (/HOLD pin or /RESET pin)

The BY25QM1GFS can also be configured to utilize hardware /RESET pin. The HOLD/RST bit in the Status Register-3 is the configuration bit for /HOLD pin function or /RESET pin function. When HOLD/RST=0 (factory default), the pin acts as a /HOLD pin as described above; when HOLD/RST=1, the pin acts as a /RESET pin. Drive the /RESET pin low for a minimum period of ~1us (tRESET(1)) will reset the device to its initial power-on state. Any on-going Program/Erase operation will be interrupted and data corruption may happen. While /RESET is low, the device will not accept any instruction input.

If QE bit is set to 1, the /HOLD or /RESET function will be disabled, the pin will become one of the four data I/O pin.

For the 16-pin package, BY25QM1GFS provides a dedicated /RESET pin in addition to the /HOLD/RST (IO3) pin. Drive the /RESET pin low for a minimum period of ~1us (tRESET(1)) will reset the device to its initial power-on state. The HOLD/RST bit or QE bit in the Status Register will not affect the function of this dedicated /RESET pin.

Hardware /RESET pin has the highest priority among all the input signals. Drive /RESET low for a minimum period of ~1us (tRESET(1)) will interrupt any on-going external/internal operations, regardless the status of other SPI signals (/CS, CLK, IOs, /WP and /HOLD).

Notes:

1. While a faster /RESET pulse (as short as a few hundred nanoseconds) will often reset the device, a 1us minimum pulse is recommended to ensure reliable operation.
2. There is an internal pull-up resistor for the dedicated /RESET pin on the 16-pin package. If the reset function is not used, this pin can be left floating in the system.

5.4.3 Hardware Reset (JEDEC Standard Hardware Reset)

The BY25QM1GFS supports JEDEC Standard Hardware Reset. The JEDEC Standard Hardware Reset sequence can also be used to reset the device to its power on state without cycling power.

The reset sequence does not use the SCLK pin. The SCLK has to be low (mode 0) or high (mode 3) through the entire reset sequence. This prevents any confusion with a instruction, as no instruction bits are transferred (clocked).

A reset is commanded when the data on the SI pin is 0101 on four consecutive positive edges of the /CS pin with no edge on the SCLK pin throughout. The is a sequence where

1. /CS is driven active low to select the device.
2. Clock (SCLK) remains stable in either a high or low state.
3. SI is driven low by the bus master, simultaneously with /CS going active low. No SPI bus slave drives SI during /CS low before a transition of SCLK i.e.: slave streaming output active is not allowed until after the first edge of SCLK.
4. /CS is driven inactive. The slave captures the state of SI on the rising edge of /CS.

The above steps are repeated 4 times, each time alternating the state of SI.

After the fourth /CS pulse, the slave triggers its internal reset. SI is low on the first /CS, high on the second, low on the third, high on the fourth. This provides a value of 5H, unlike random noise. Any activity on SCLK during this time will halt the sequence and a Reset will not be generated. Figure below illustrates the timing for hardware Reset operation.

Figure 7. JEDEC Standard Hardware Reset

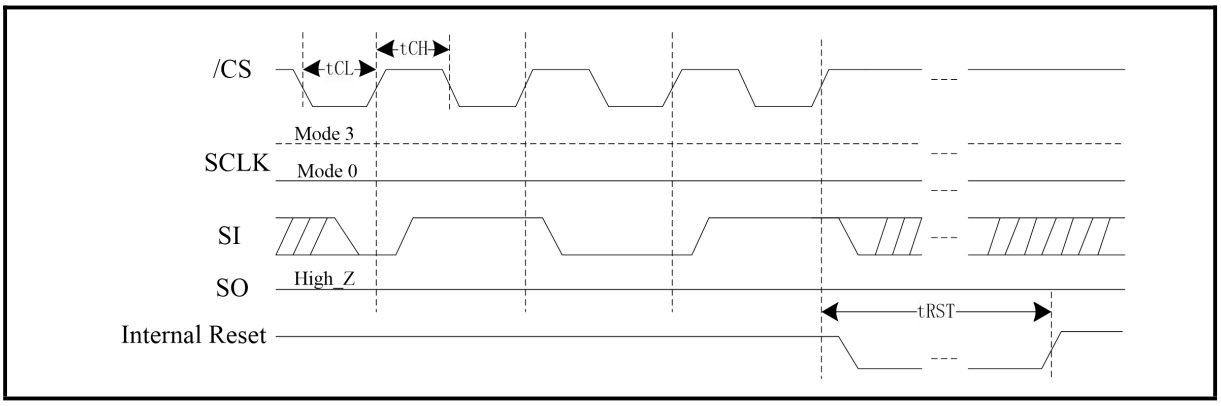


Table 5. JEDEC Standard Hardware Reset Timing Parameters

Parameter	Min.	Typ.	Max.	Unit.
tCL	20			ns
tCH	20			ns
Setup Time	5			ns
Hold Time	5			ns

5.5 Write Protect Features

1. Software Protection (Memory array):

   - The Block Protect (BP4, BP3, BP2, BP1, BP0) bits define the section of the memory array that can be read but not change.

   - Advanced Block/Sector Protection (Solid and Password Protect): The BY25QM1GFS also provides another Write Protect method using the Advanced Block/Sector Protection. Each 64KB block (except the top and bottom blocks, total of 510 blocks) and each 4KB sector within the top/bottom blocks (total of 32 sectors) are equipped with the Individual SPB and DPB bit. When the SPB or DPB bit is 0, the corresponding sector or block can be erased or programmed; when the SPB or DPB bit is set to 1, Erase or Program instructions issued to the corresponding sector or block will be ignored.

   The WPS bit in Status Register-3 is used to decide which Write Protect scheme should be used. When WPS=0 (factory default), the device will only utilize CMP, BP[4:0] bits to protect specific areas of the array; when WPS=1, the device will utilize the Advanced Block/Sector Protection for write protection.

2. Hardware Protection (Status register): /WP going low to protected the writable bits of Status Register.

3. Deep Power-Down: In Deep Power-Down Mode, all instructions are ignored except the Release from deep Power-Down Mode instruction.

4. Device resets when VCC is below threshold: Upon power-up or at power-down, the BY25QM1GFS will maintain a reset condition while VCC is below the threshold value of V_{WI}. While reset, all operations are disabled and no instructions are recognized.

5. Time delay write disable after Power-up: During power-up and after the VCC voltage exceeds $V_{CC\ (min)}$, all program and erase related instructions are further disabled for a time delay of tVSL. This includes the Write Enable, Page Program, Sector Erase, Block Erase, Chip Erase and the Write Status Register instructions.

6. Write Enable: The Write Enable instruction is set the Write Enable Latch bit. The WEL bit will return to reset by following situation:

   -Power –up
   -Write Disable
   -Write Status Register (Whether the SR is protected, WEL will return to reset)
   -Write Extended Address Register (when in 3-Byte Address Mode)
   -After some Advanced Block/Sector Protection instructions that need Write Enable instruction (see ***Table 20***) are executed correctly, WEL bit will return to reset (when WPS=1)
   -Page Program (Whether the program area is protected, WEL will return to reset)
   -Sector Erase/Block Erase/Chip Erase (Whether the erase area is protected, WEL will return to reset)
   -Software Reset
   -Hardware Reset

7. One Time Program (OTP) write protection for array and Security Registers using Status Register.

5.6 Status Register

5.6.1 Status Register Table

See ***Table 6*** for detail description of the Status Register bits.

Table 6. Single Die BY25Q256FS Status Register

	SR3							
	S23	**S22**	**S21**	**S20**	**S19**	**S18**	**S17**	**S16**
	HOLD/RST	**DRV1**	**DRV0**	**Reserved**	**Reserved**	**WPS**	**ADP**	**ADS**
Default (1)	0	0	0	×	×	0	0	0
						OTP		Read only

	SR2							
	S15	**S14**	**S13**	**S12**	**S11**	**S10**	**S9**	**S8**
	SUS1	**CMP**	**LB3**	**LB2**	**LB1**	**SUS2**	**QE**	**SRP1**
Default (1)	0	0	0	0	0	0	0	0
	Read Only		OTP	OTP	OTP	Read Only		

	SR1							
	S7	**S6**	**S5**	**S4**	**S3**	**S2**	**S1**	**S0**
	SRP0	**BP4**	**BP3**	**BP2**	**BP1**	**BP0**	**WEL**	**WIP**
Default (1)	0	0	0	0	0	0	0	0
							Read Only	Read Only

Notes:

1. The default value is set by Manufacturer during wafer sort, Marked as Default in following text

5.6.2 The Status and Control Bits

5.6.2.1 WIP bit

The Write in Progress (WIP) bit indicates whether the memory is busy in program/erase/write status register progress. When WIP bit sets to 1, means the device is busy in program/erase/write status register progress, when WIP bit sets 0, means the device is not in program/erase/write status register progress.

5.6.2.2 WEL bit

The Write Enable Latch (WEL) bit indicates the status of the internal Write Enable Latch. When set to 1 the internal Write Enable Latch is set, when set to 0 the internal Write Enable Latch is reset and no Write Status Register, Program or Erase, etc. instruction is accepted.

5.6.2.3 BP4, BP3, BP2, BP1, BP0 bits

The Block Protect (BP4, BP3, BP2, BP1, BP0) bits are non-volatile. They define the size of the area to be software protected against Program and Erase instructions. These bits are written with the Write Status Register instruction. When WPS=0, and the Block Protect (BP4, BP3, BP2, BP1, BP0) bits are set to 1, the relevant memory area (as defined in ***Table 9-Table 10***).becomes protected against Page Program, Sector Erase and Block Erase instructions. The Block Protect (BP4, BP3, BP2, BP1, BP0) bits can be written provided that the Hardware Protected mode has not been set. The Chip Erase instruction is executed, if the Block Protect (BP2, BP1, BP0) bits are 0 and CMP=0 or The Block Protect (BP2, BP1, BP0) bits are 1 and CMP=1.

5.6.2.4 SRP1, SRP0 bits

The Status Register Protect (SRP1 and SRP0) bits are non-volatile Read/Write bits in the status register. The SRP bits control the method of write protection: software protection, hardware protection, power supply lock-down or one time programmable protection.

Table 7. Status Register protect table

SRP1	SRP0	/WP	Status Register	Description
0	0	X	Software Protected	The Status Register can be written to after a Write Enable instruction, WEL=1.(Factory Default)
0	1	0	Hardware Protected	/WP=0, the Status Register locked and cannot be written.
0	1	1	Hardware Unprotected	/WP=1, the Status Register is unlocked and can be written to after a Write Enable instruction, WEL=1.
1	0	X	Power Supply Lock-Down(1)	Status Register is protected and cannot be written to again until the next Power-Down, Power-Up cycle.
1	1	X	One Time Program(2)	Status Register is permanently protected and cannot be written to.

Notes:

1. When SRP1, SRP0= (1, 0), a Power-Down, Power-Up cycle will change SRP1, SRP0 to (0, 0) state.
2. The One time Program feature is available upon special order. Please contact BY Technology for details.

5.6.2.5 QE bit

The Quad Enable (QE) bit is a non-volatile Read/Write bit in the Status Register that allows Quad operation. When the QE bit is set to 0 (Default) the /WP pin and /HOLD pin are enable. When the QE pin is set to 1, the Quad IO2 and IO3 pins are enabled. (The QE bit should never be set to 1 during standard SPI or Dual SPI operation if the /WP or /HOLD pins directly to the power supply or ground).

QE bit is required to be set to a 1 before issuing an “Enter QPI (38h)” to switch the device from Standard/Dual/Quad SPI to QPI; otherwise the instruction will be ignored. When the device is in QPI mode, QE bit will remain to be 1. A “Write Status Register” instruction in QPI mode cannot change QE bit from “1” to “0”.

5.6.2.6 LB3/LB2/LB1 bits

The Security Register Lock (LB3/LB2/LB1) bits are non-volatile One Time Program (OTP) bits in Status Register (S13–S11) that provide the write protect control and status to the Security Registers. The default state of LB is 0, the security registers are unlocked. LB can be set to 1 individually using the Write Register instruction. LB is One Time Programmable, once they are set to 1, the Security Registers will become read-only permanently.

5.6.2.7 CMP bit

The Complement Protect (CMP) bit is a non-volatile Read/Write bit in the Status Register (S14). It is used in conjunction the BP4-BP0 bits to provide more flexibility for the array protection. Please see the Status registers Memory Protection table for details. The default setting is CMP=0.

5.6.2.8 SUS1/SUS2 bits

The Suspend Status (SUS1 and SUS2) bits are read only bits in the status register2 (S15 and S10) that are set to 1 after executing a Program/Erase Suspend (75H) instruction (The Erase Suspend will set SUS1 to 1, and the Program Suspend will set the SUS2 to 1). The SUS1 and SUS2 bits are cleared to 0 by Program/Erase Resume (7AH) instruction as well as a power-down, power-up cycle.

5.6.2.9 ADS bit

The Current Address Mode (ADS) bit is a read only bit in the Status Register3 that indicates which address mode the device is currently operating in. When ADS=0, the device is in the 3-Byte Address Mode, when ADS=1, the device is in the 4-Byte Address Mode.

5.6.2.10 ADP bit

The Power-Up Address Mode (ADP) bit is a non-volatile bit that determines the initial address mode when the device is powered on or reset. This bit is only used during the power on or device reset initialization period, and it is only writable by the non-volatile Write Status sequence (06h + 11h). When ADP=0 (factory default), the device will power up into 3-Byte Address Mode, the Extended Address Register must be used to access memory regions beyond 128Mb. When ADP=1, the device will power up into 4-Byte Address Mode directly.

5.6.2.11 HOLD/RST bit

The /HOLD or /RESET Pin Function (HOLD/RST) bit is used to determine whether /HOLD or /RESET function should be implemented on the hardware pin. When HOLD/RST=0 (factory default), the pin acts as /HOLD; when HOLD/RST=1, the pin acts as /RESET. However, /HOLD or /RESET functions are only available when QE=0. If QE is set to 1, the /HOLD and /RESET functions are disabled, the pin acts as a dedicated data I/O pin.

5.6.2.12 WPS bit

There are two write memory array protection methods provided on BY25QM1GFS： Block Protection (BP) mode or Advanced Block/Sector Protection mode. The protection modes are mutually exclusive. The WPS bit selects which protection mode is enabled. Please note that the WPS bit is an OTP bit. Once WPS is set to “1”, it cannot be programmed back to “0”.

If WPS=0 (factory default), the BP mode is enabled and Advanced Block/Sector Protection mode is disabled. Please note that if WPS=0, all Advanced Block/Sector Protection instructions (***7.5.1-7.5.18***) are not available.

If WPS=1, the Advanced Block/Sector Protection mode is enabled and BP mode is disabled. Blocks or Sectors are individually protected by their own SPB or DPB. On power-up, all Blocks or Sectors are write protected by the Dynamic Protection Bits (DPB) by default. The Advanced Block/Sector Protection instructions (***7.5.1-7.5.18***) are activated. The CMP, BP[4:0] bits of the Status Register are disabled and have no effect.

5.6.2.13 DRV1/DRV0 bits

The Output Driver Strength (DRV1&DRV0) bits are used to determine the output driver strength for the Read instruction.

Table 8. The Output Driver Strength

DRV1,DRV0	Driver Strength
00	100%(default)
01	75%
10	50%
11	25%

5.7 Array Memory Protection

5.7.1 Block Protect Table (WPS=0)

Table 9. Single Die BY25Q256FS Block Memory Protection (WPS=0, CMP=0)

Status Register Content					Memory Content			
BP4	BP3	BP2	BP1	BP0	Blocks	Addresses	Density	Portion
X	0	0	0	0	NONE	NONE	NONE	NONE
0	0	0	0	1	511	01FF0000h -01FFFFFFh	64KB	Upper 1/512
0	0	0	1	0	510 to 511	01FE0000h -01FFFFFFh	128KB	Upper 1/256
0	0	0	1	1	508 to 511	01FC0000h -01FFFFFFh	256KB	Upper 1/128
0	0	1	0	0	504 to 511	01F80000h - 01FFFFFFh	512KB	Upper 1/64
0	0	1	0	1	496 to 511	01F00000h - 01FFFFFFh	1MB	Upper 1/32
0	0	1	1	0	480 to 511	01E00000h -01FFFFFFh	2MB	Upper 1/16
0	0	1	1	1	448 to 511	01C00000h -01FFFFFFh	4MB	Upper 1/8
0	1	0	0	0	384 to 511	01800000h - 01FFFFFFh	8MB	Upper 1/4
0	1	0	0	1	256 to 511	01000000h - 01FFFFFFh	16MB	Upper 1/2
1	0	0	0	1	0	00000000h - 0000FFFFh	64KB	Lower 1/512
1	0	0	1	0	0 to 1	00000000h - 0001FFFFh	128KB	Lower 1/256
1	0	0	1	1	0 to 3	00000000h - 0003FFFFh	256KB	Lower 1/128
1	0	1	0	0	0 to 7	00000000h - 0007FFFFh	512KB	Lower 1/64
1	0	1	0	1	0 to 15	00000000h - 000FFFFFh	1MB	Lower 1/32
1	0	1	1	0	0 to 31	00000000h - 001FFFFFh	2MB	Lower 1/16
1	0	1	1	1	0 to 63	00000000h - 003FFFFFh	4MB	Lower 1/8
1	1	0	0	0	0 to 127	00000000h - 007FFFFFh	8MB	Lower 1/4
1	1	0	0	1	0 to 255	00000000h - 00FFFFFFh	16MB	Lower 1/2
X	1	1	0	X	0 to 511	00000000h - 01FFFFFFh	32MB	ALL
X	1	X	1	X	0 to 511	00000000h - 01FFFFFFh	32MB	ALL

Table 10. Single Die BY25Q256FS Block Memory Protection (WPS=0, CMP=1)

Status Register Content					Memory Content			
BP4	BP3	BP2	BP1	BP0	Blocks	Addresses	Density	Portion
X	0	0	0	0	ALL	00000000h - 01FFFFFFh	ALL	ALL
0	0	0	0	1	0 to 510	00000000h - 01FEFFFFh	32,704KB	Lower 511/512
0	0	0	1	0	0 to 509	00000000h - 01FDFFFFh	32,640KB	Lower 255/256
0	0	0	1	1	0 to 507	00000000h - 01FBFFFFh	32,512KB	Lower 127/128
0	0	1	0	0	0 to 503	00000000h - 01F7FFFFh	32,256KB	Lower 63/64
0	0	1	0	1	0 to 495	00000000h - 01EFFFFFh	31MB	Lower 31/32
0	0	1	1	0	0 to 479	00000000h - 01DFFFFFh	30MB	Lower 15/16
0	0	1	1	1	0 to 447	00000000h - 01BFFFFFh	28MB	Lower 7/8
0	1	0	0	0	0 to 383	00000000h - 017FFFFFh	24MB	Lower 3/4
0	1	0	0	1	0 to 255	00000000h - 00FFFFFFh	16MB	Lower 1/2
1	0	0	0	1	1 to 511	00010000h - 01FFFFFFh	32,704KB	Upper 511/512
1	0	0	1	0	2 to 511	00020000h - 01FFFFFFh	32,640KB	Upper 255/256
1	0	0	1	1	4 to 511	00040000h - 01FFFFFFh	32,512KB	Upper 127/128
1	0	1	0	0	8 to 511	00080000h - 01FFFFFFh	32,256KB	Upper 63/64
1	0	1	0	1	16 to 511	00100000h - 01FFFFFFh	31MB	Upper 31/32
1	0	1	1	0	32 to 511	00200000h - 01FFFFFFh	30MB	Upper 15/16
1	0	1	1	1	64 to 511	00400000h - 01FFFFFFh	28MB	Upper 7/8
1	1	0	0	0	128 to 511	00800000h - 01FFFFFFh	24MB	Upper 3/4
1	1	0	0	1	256 to 511	01000000h - 01FFFFFFh	16MB	Upper 1/2
X	1	1	0	X	NONE	NONE	NONE	NONE
X	1	X	1	X	NONE	NONE	NONE	NONE

5.7.2 Advanced Block/Sector Protection (WPS=1)

Advanced Block/Sector Protection can protect individual 4KB sectors in the bottom and top 64KB of memory and protect individual 64KB blocks in the rest of memory.

There is one non-volatile Solid Protection Bit (SPB) and one volatile Dynamic Protection Bit (DPB) assigned to each 4KB sector at the bottom and top 64KB of memory and to each 64KB block in the rest of memory. A sector or block is write-protected from programming or erasing when its associated SPB or DPB is set to “1”. The Unprotect Solid Protect Bit (USPB) can temporarily override and disable the write-protection provided by the SPB bits.

There are two mutually exclusive implementations of Advanced Block/Sector Protection: Solid Protection mode (factory default) and Password Protection mode. Solid Protection mode permits the SPB bits to be modified after power-on or a reset. The Password Protection mode requires a valid password before allowing the SPB bits to be modified.

Please note that if WPS=0, all Advanced Block/Sector Protection instructions (***7.5.1-7.5.18***) are not available.

Figure 8. Solid Protection Mode and Password Protection Mode of Advanced Block/Sector Protection

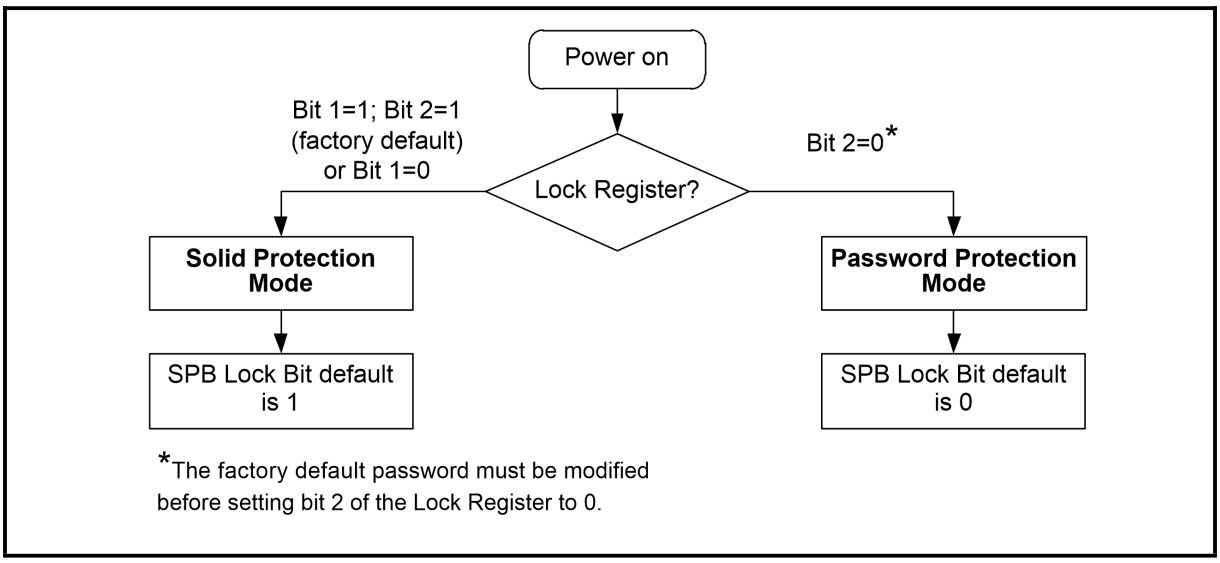


Figure 9. Enter Password Protection Mode

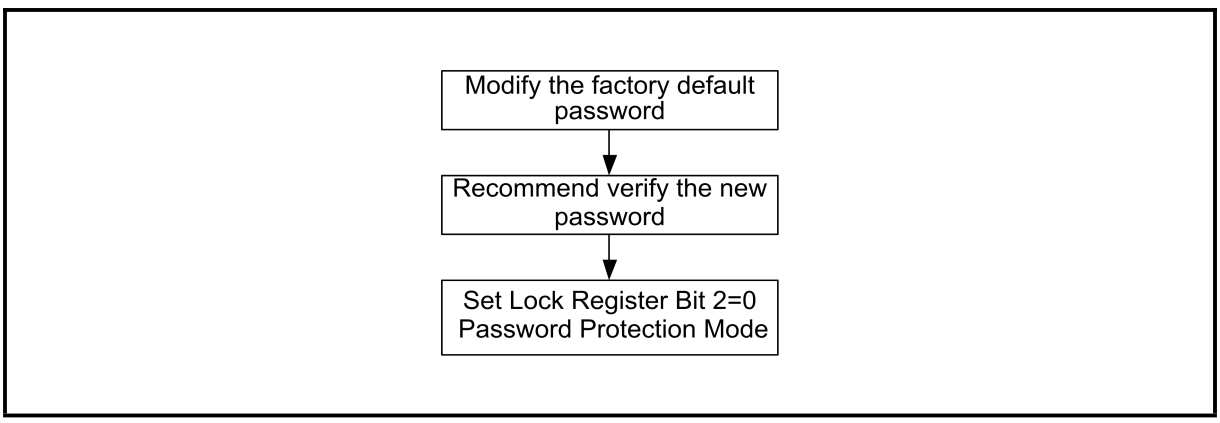
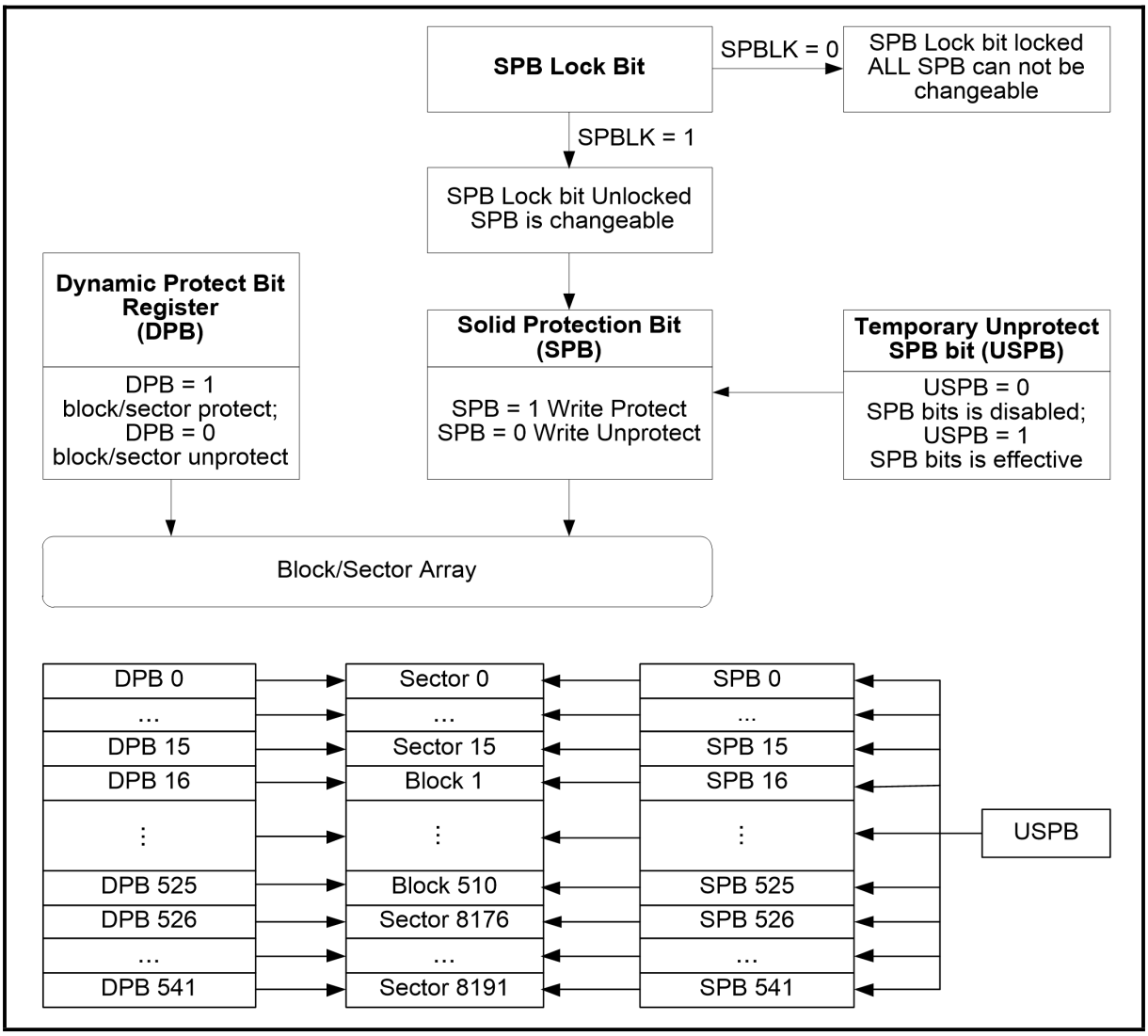


Figure 10. Single Die BY25Q256FS SPB, DPB and USPB protection for Block/Sector Array



5.7.2.1 Lock Register

The Lock Register is a 16-bit one-time programmable register. Lock Register bits [2:1] select between Solid Protection mode and Password Protection mode. When both bits are “1” (factory default), Solid Protection mode is enabled by default. The Lock Register is programmed using the Write Lock Register instruction. Programming Lock Register bit 1 to “0” permanently selects Solid Protection mode and permanently disables Password Protection mode. Conversely, programming bit 2 to “0” permanently selects Password Protection mode and permanently disables Solid Protection mode. Bits 1 and 2 cannot be programmed to “0” at the same time otherwise the device will abort the operation. A Write Enable instruction must be executed to set the WEL bit before sending the Write Lock Register instruction.

A password must be set prior to selecting Password Protection mode. The password can be set by issuing the Write Password Register instruction.

Table 11. Lock Register

Bit 15-3	Bit 2	Bit 1	Bit0
Reserved	Password Protection Mode Lock Bit	Solid Protection Mode Lock Bit	Reserved
×	0=Password Protection Mode Enable 1= Password Protection Mode not enable (Default =1)	0=Solid Protection Mode Enable 1= Solid Protection Mode not enable (Default =1)	×
OTP	OTP	OTP	OTP

Notes:
1. Once bit 2 or bit 1 has been programmed to "0", the other bit can't be changed any more.

5.7.2.2 SPB Lock Bit

The SPB Lock Bit (SPBLK) is a volatile bit located in bit 0 of the SPB Lock Register. The SPBLK bit controls whether the SPB bits can be modified or not. If SPBLK=1, the SPB bits are unprotected and can be modified. If SPBLK=0, the SPB bits are protected (“locked”) and cannot be modified. The power-on and reset status of the SPBLK bit is determined by Lock Register bits [2:1]. Refer to SPB Lock Register for SPBLK bit default power-on status. The Read SPB Lock Register instruction can be used to read the SPB Lock Register to determine the state of the SPBLK bit.

In Solid Protection mode, the SPBLK bit defaults to “1” after power-on or reset. When SPBLK=1, the SPB bits are unprotected (“unlocked”) and can be modified. The SPB Lock Bit Clear instruction can be used to write the SPBLK bit to “0” and protect the SPB bits. A Write Enable instruction must be executed to set the WEL bit before sending the SPB Lock Bit Clear instruction. Once the SPBLK has been written to “0”, there is no instruction (except a software reset) to set the bit back to “1”. A power-on cycle or reset is required to set the SPB lock bit back to “1”.

In Password Protection mode, the SPBLK bit defaults to “0” after power-on or reset. A valid password must be provided to set the SPBLK bit to “1” to allow the SPBs to be modified. After the SPBs have been set to the desired status, use the SPB Lock Bit Clear instruction to clear the SPBLK bit back to “0” in order to prevent further modification.

Please note that the SPBLK bit will automatically become “0” when entering the Password Protection mode from Solid Protection mode, even if the original value is “1”.

Table 12. SPB Lock Register

Bit	Description	Bit Status	Default	Type
7-1	Reserved	×	0000000	Volatile
0	SPBLK (SPB Lock Bit)	0 = SPBs protected 1= SPBs unprotected	Solid Protection Mode: 1 Password Protection Mode: 0	Volatile

5.7.2.3 Solid Protection Bits

The Solid Protection Bits (SPBs) are non-volatile bits for enabling or disabling write-protection to sectors and blocks. The SPB bits have the same endurance as the Flash memory. An SPB is assigned to each 4KB sector in the bottom and top 64KB of memory and to each 64KB block in the remaining memory. The factory default state of the SPB bits is “0”, which has the block/sector write-protection disabled.

When an SPB is set to “1”, the associated sector or block is write-protected. Program and erase operations on the sector or block will be inhibited. SPBs can be individually set to “1” by the SPB Program instruction. However, the SPBs cannot be individually cleared to “0”. Issuing the SPB Erase instruction clears all SPBs to “0”. A Write Enable instruction must be executed to set the WEL bit before sending the SPB Program or SPB Erase instruction.

The SPBLK bit must be “1” before any SPB can be modified. In Solid Protection mode the SPBLK bit defaults to “1” after power-on or reset. Under Password Protection mode, the SPBLK bit defaults to “0” after power-on or reset, and a Password Unlock instruction with a correct password is required to set the SPBLK bit to “1”.

The SPB Lock Bit Clear instruction clears the SPBLK bit to “0”, locking the SPB bits from further modification.

The Read SPB Status instruction reads the status of the SPB of a sector or block. The Read SPB Status instruction returns 00h if the SPB is “0”, indicating write-protection is disabled. The Read SPB Status instruction returns FFh if the SPB is “1”, indicating write-protection is enabled.

In Solid Protection mode, the Unprotect Solid Protect Bit (USPB) can temporarily mask the SPB bits and disable the write-protection provided by the SPB bits.

Note: If SPBLK=0, instructions to set or clear the SPB bits will be ignored.

Table 13. Solid Protection Bit

Description	Bit Status	Default	Type
Solid Protection Bit (SPB)	0 = Unprotect Sector / Block 1 = Protect Sector / Block	0	Non-volatile

5.7.2.4 Dynamic Protection Bits

The Dynamic Protection Bits (DPBs) are volatile bits for quickly and easily enabling or disabling write-protection to sectors and blocks. A DPB is assigned to each 4KB sector in the bottom and top 64KB of memory and to each 64KB block in the rest of the memory. The DBPs can enable write-protection on a sector or block regardless of the state of the corresponding SPB. However, the DPB bits can only unprotect sectors or blocks whose SPB bits are “0” (unprotected).

When a DPB is “1”, the associated sector or block will be write-protected, preventing any program or erase operation on the sector or block. All DPBs default to “1” after power-on or reset. When a DPB is cleared to “0”, the associated sector or block will be unprotected if the corresponding SPB is also “0”.

DPB bits can be individually set to “1” or “0” by the Dynamic Protection Block/Sector Lock/ Dynamic Protection Block/Sector Unlock instruction. The DBP bits can also be globally cleared to “0” with the Global Block/Sector Unlock instruction or globally set to “1” with the Global Block/Sector Lock instruction. A Write Enable instruction must be executed to set the WEL bit before sending the Dynamic Protection Block/Sector Lock, Dynamic Protection Block/Sector Unlock, Global Block/Sector Lock, or Global Block/Sector Unlock instruction.

The Read DPB Status instruction reads the status of the DPB of a sector or block. The Read DPB Status instruction returns 00h if the DPB is “0”, indicating write-protection is disabled. The Read DPB Status instruction returns FFh if the DPB is “1”, indicating write-protection is enabled.

Table 14. Dynamic Protection Bit

Description	Bit Status	Default	Type
Dynamic Protection Bit (DPB)	0 = Unprotect Sector / Block 1 = Protect Sector / Block	1	Volatile

5.7.2.5 Unprotect Solid Protect Bit

The Unprotect Solid Protect Bit (USPB) is a volatile bit that defaults to “1” after power-on or reset. When USPB=1, the SPBs have their normal function. When USPB=0 all SPBs are masked and their write-protected sectors and blocks are temporarily unprotected (as long as their corresponding DPBs are “0”). The USPB provides a means to temporarily override the SPBs without having to issue the SPB Erase and SPB Program instructions to clear and set the SPBs.

The USPB can be read as often as needed in Solid Protection mode or Password Protection mode and can be set or cleared as often as needed in Solid Protection mode or after providing a valid password in Password Protection mode.

Please refer to ***Table 15*** for the sector state with the protection status of DPB/SPB/USPB bits

Table 15. Block/Sector Protection States Summary Table

Protection Status			Block/Sector Protection State
DPB	SPB	USPB	
0	0	0	Unprotected
0	0	1	Unprotected
0	1	0	Unprotected
0	1	1	Protected
1	0	0	Protected
1	0	1	Protected
1	1	0	Protected
1	1	1	Protected

5.7.2.6 Password Protection Mode

Password Protection mode potentially provides a higher level of security than Solid Protection mode. In Password Protection mode, the SPBLK bit defaults to “0” after a power-on cycle or reset. When SPBLK=0, the SPBs are locked and cannot be modified. A 64-bit password must be provided to unlock the SPBs.

The Password Unlock instruction with the correct password will set the SPBLK bit to “1” and unlock the SPB bits. After the correct password is given, a wait of tPW1 (typical value is 2us) is necessary for the SPB bits to unlock. The Status Register WIP bit will clear to “0” upon completion of the Password Unlock instruction. Once unlocked, the SPB bits can be modified. A Write Enable instruction must be executed to set the WEL bit before sending the Password Unlock instruction.

Several steps are required to place the device in Password Protection mode. Prior to entering the Password Protection mode, it is necessary to set the 64-bit password and recommend verify it via use Read Password Register instruction. The Write Password Register instruction writes the password and the Read Password Register instruction reads back the password. Password verification is permitted until the Password Protection Mode Lock Bit has been written to “0”. Password Protection mode is activated by programming the Password Protection Mode Lock Bit to “0”. This operation is not reversible. Once the bit is programmed, it cannot be erased. The device remains permanently in Password Protection mode and the 64-bit password can neither be retrieved nor reprogrammed.

The password is all “1’s” when shipped from the factory. The Write Password Register instruction can only program password bits to “0”. The Write Password Register instruction cannot program “0’s” back to “1’s”. All 64-bit password combinations are valid password options. A Write Enable instruction must be executed to set the WEL bit before sending the Write Password Register instruction.

- The unlock operation will fail if the password provided by the Password Unlock instruction does not match the stored password. This will insert a tPW2 (100us ± 20us) delay before clearing the WIP bit to “0”.
- The Password Unlock instruction is prohibited from being executed faster than once every tPW2 (100us ± 20us). This restriction makes it impractical to attempt all combinations of a 64-bit password (such an effort would take ~58 million years). Monitor the WIP bit to determine whether the device has completed the Password Unlock instruction.
- When a valid password is provided, the Password Unlock instruction does not insert the tPW2 (100us ± 20us) delay before returning the WIP bit to zero. The SPBLK bit will set to “1”.
- The factory default password must be modified before enter the Password Protection mode (setting bit 2 of the Lock Register to 0). Otherwise, the chip will not be able to enter the Password Protection mode, that is, cannot set bit 2 of the Lock Register to 0.

Table 16. Password Register

Bits	Field Name	Function	Type	Default State	Description
63 to 0	PWD	Hidden Password	OTP	FFFFFFFFFFFFFFFFh	Non-volatile OTP storage of 64 bit password. The password is no longer readable after the Password Protection mode is selected by programming Lock Register bit 2 to zero.

5.8 Single Die BY25Q256FS Extended Address Register

In addition to the Status Registers, the BY25Q256FS also provides a volatile Extended Address Register that allows the 256M area of the device to be used normally in 3-Byte Address Mode. The value of the Extended Address Register and the 24-bit address input in the 3-Byte Address Mode together form the complete start address of the instruction operation. That is, when A24 = 0, the starting address of the instruction operation selects the lower 128Mb memory array (00000000h-00FFFFFFh). When A24 = 1, the start address of the instruction operation will select the high 128Mb memory array (01000000h-01FFFFFFh).

Please note that:

1. In 3-Byte Address Mode, When A24 = 0/1, the starting address of the instruction operation selects the lower/ high 128Mb memory array. However, as the instruction operation address continues to be carried, the address of the instruction operation can enter the high/lower 128Mb memory array. At this time, the value of the Extended Address Register does not change with the carry of the address, that is, the value of Extended Address Register can only be modified by the Write Extended Address Register instruction.
2. In 4-Byte Address Mode, Extended Address Register is not available. The value of Extended Address Register has no effect on the instruction operation. The device will require 4-Byte address input for all address related instructions, and the Extended Address Register setting will be ignored. The Read Extended Address Register and Write Extended Address Register instructions are not available in the 4-Byte Address Mode. At the same time, during the instruction operation, the same as in the 3-Byte Address Mode, the carry of the address does not have any effect on the Extended Address Register.

Table 17. Extended Address Register

EA7	EA6	EA5	EA4	EA3	EA2	EA1	EA0
A31(1)	A30(1)	A29(1)	A28(1)	A27(1)	A26(1)	A25(1)	A24(2)

Notes:
1. Reserved for higher densities: 512Mb ~ 32Gb.
2. Address Bit #24:A24=0: Select lower 128Mb; A24=1: Select upper 128Mb.

6. Device Identification

Three legacy Instructions are supported to access device identification that can indicate the manufacturer, device type, and capacity (density). The returned data bytes provide the information as shown in the below table.

Table 18. Single Die BY25Q256FS ID Definition table

Operation Code	M7-M0(SPI)	ID15-ID8(SPI)	ID7-ID0(SPI)
9FH	68	49	19
90H/92H/94H	68		18
ABH			18

Operation Code	M7-M0(QPI)	ID15-ID8(QPI)	ID7-ID0(QPI)
9FH	68	48	19
90H/92H/94H	68		18
ABH			18

7. Instructions Description

All instructions, addresses and data are shifted in and out of the device, beginning with the most significant bit on the first rising edge of SCLK after /CS is driven low. Then, the one byte instruction code must be shifted in to the device, most significant bit first on SI, each bit being latched on the rising edges of SCLK.

See ***Table 19***, every instruction sequence starts with a one-byte instruction code. Depending on the instruction, this might be followed by address bytes, or by data bytes, or by both or none. /CS must be driven high after the last bit of the instruction sequence has been shifted in. For the instruction of Read, Fast Read, Read Status Register or Release from Deep Power Down, and Read Device ID, the shifted-in instruction sequence is followed by a data out sequence. /CS can be driven high after any bit of the data-out sequence is being shifted out.

For the instruction of Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register, Write Enable, Write Disable or Deep Power-Down instruction, etc. /CS must be driven high exactly at a byte boundary, otherwise the instruction is rejected, and is not executed. That is /CS must drive high when the number of clock pulses after /CS being driven low is an exact multiple of eight. For Page Program, if at any time the input byte is not a full byte, nothing will happen and WEL will not be reset.

Table 19. Instruction Set Table

Instruction Set Table-Standard/Dual/Quad SPI Instructions, 3-Byte & 4-Byte Address Mode(1)

Data Input Output	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
Clock Number	**(0-7)**	**(8-15)**	**(16-23)**	**(24-31)**	**(32-39)**	**(40-47)**	**(48-55)**
Software Die Select	C2h	(Die ID#)					
Read Active Die ID#	F8h	(Die ID#)					
Write Enable	06h						
Volatile SR Write Enable	50h						
Write Disable	04h						
Read Status Register-1	05h	(S7-S0)(2)					
Write Status Register(4)	01h	(S7-S0)(4)	(S15-S8)				
Read Status Register-2	35h	(S15-S8)(2)					
Write Status Register-2	31h	(S15-S8)					
Read Status Register-3	15h	(S23-S16)(2)					
Write Status Register-3	11h	(S23-S16)					
Chip Erase	C7h/60h						
Program/Erase Suspend	75h						
Program/Erase Resume	7Ah						
Deep Power-down	B9h						
Release Power-down / ID	ABh	Dummy	Dummy	Dummy	(ID7-ID0)(2)		
Release Power-down	ABH						
Manufacturer/Device ID	90h	Dummy	Dummy	00/01h	(MF7-MF0)/ (ID7-ID0)	(ID7-ID0)/ (MF7-MF0)	
Read JEDEC ID	9Fh	(MF7-MF0)	(ID15-ID8)	(ID7-ID0)(9)			
Read Serial Flash Discoverable Parameter	5Ah	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)	
Enter QPI Mode	38h						
Enable Reset	66h						
Reset Device	99h						
Read Data with 4-Byte Address	13h	A31-A24	A23-A16	A15-A8	A7-A0	(D7-D0)	
Fast Read with 4-Byte Address	0Ch	A31-A24	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)
Fast Read Dual Output with 4-Byte Address	3Ch	A31-A24	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0, …)(7)
Fast Read Quad Output with 4-Byte Address	6Ch	A31-A24	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0, …)(9)
Data Input Output	**Byte 1**	**Byte 2**	**Byte 3**	**Byte 4**	**Byte 5**	**Byte 6**	**Byte 7**
Clock Number	**(0-7)**	**(8-11)**	**(12-15)**	**(16-19)**	**(20-23)**	**(24-27)**	**(28-31)**
Fast Read Dual I/O with 4-Byte Address	BCh	A31-A24	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)

Data Input Output	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7	Byte 8	Byte 9
Clock Number	**(0-7)**	**(8-9)**	**(10-11)**	**(12-13)**	**(14-15)**	**(16-17)**	**(18-19)**	**(20-21)**	**(22-23)**
Fast Read Quad I/O with 4-Byte Address	ECh	A31-A24	A23-A16	A15-A8	A7-A0	M7-M0	Dummy	Dummy	(D7-D0)

Data Input Output	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
Clock Number	**(0-7)**	**(8-9)**	**(10-11)**	**(12-13)**	**(14-15)**	**(16-17)**	**(18-19)**

Page Program with 4-Byte Address	12h	A31-A24	A23-A16	A15-A8	A7-A0	(D7-D0)	(D7-D0)[3]			
Quad Page Program with 4-Byte Address	34h	A31-A24	A23-A16	A15-A8	A7-A0	(D7-D0)				
Sector Erase (4KB) with 4-Byte Address	21h	A31-A24	A23-A16	A15-A8	A7-A0					
Block Erase(32K) with 4-Byte Address	5Ch	A31-A24	A23-A16	A15-A8	A7-A0					
Block Erase(64K) with 4-Byte Address	DCh	A31-A24	A23-A16	A15-A8	A7-A0					
Read Lock Register	2Dh	(S7-S0)	Next Byte							
Write Lock Register	2Ch	(S7-S0)	(S15-S8)							
SPB Lock Bit Clear	A6h									
Read SPB Lock Register	A7h	(S7-S0)	Next Byte							
SPB Erase	E4h									
Global Block/Sector Lock	7Eh									
Global Block/Sector Unlock	98h									
Read Unprotect Solid Protect Bit	AAh	(S7-S0)	Next Byte							
Unprotect Solid Protect Bit Set	A8h									
Unprotect Solid Protect Bit Clear	A9h									

Data Input Output	**Byte 1**	**Byte 2**	**Byte 3**	**Byte 4**	**Byte 5**	**Byte 6**	**Byte 7**	**Byte 8**	**Byte 9**	**Byte 10**
Clock Number	**（0-7）**	**（8-9）**	**（10-11）**	**（12-13）**	**（14-15）**	**（16-17）**	**（18-19）**	**（18-19）**	**（18-19）**	**（18-19）**
Read Password Register	27h	(P7-P0)	(P15-P8	(P23-P16)	(P31-P24)	(P39-P32)	(P47-P40)	(P55-P48)	(P63-P56)	Next Byte
Write Password Register	28h	(P7-P0)	(P15-P8	(P23-P16)	(P31-P24)	(P39-P32)	(P47-P40)	(P55-P48)	(P63-P56)	
Password Unlock	29h	(P7-P0)	(P15-P8	(P23-P16)	(P31-P24)	(P39-P32)	(P47-P40)	(P55-P48)	(P63-P56)	

Instruction Set Table-Standard/Dual/Quad SPI Instructions, 3-Byte Address Mode (1)

Data Input Output	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6
Clock Number	**(0-7)**	**(8-15)**	**(16-23)**	**(24-31)**	**(32-39)**	**(40-55)**
Read Unique ID Number	4Bh	Dummy	Dummy	Dummy	Dummy	(ID127-ID0)
Clock Number	**(0-7)**	**(8-15)**	**(16-23)**	**(24-31)**	**(32-39)**	**(40-47)**
Page Program	02h	A23-A16	A15-A8	A7-A0	(D7-D0)	(D7-D0)(3)
Quad Page Program	32h	A23-A16	A15-A8	A7-A0	(D7-D0, …)(9)	(D7-D0, …)(3)
Sector Erase (4KB)	20h	A23-A16	A15-A8	A7-A0		
Block Erase (32KB)	52h	A23-A16	A15-A8	A7-A0		
Block Erase (64KB)	D8h	A23-A16	A15-A8	A7-A0		
Normal Read Data	03h	A23-A16	A15-A8	A7-A0	(D7-D0)	(Next Byte)
Fast Read	0Bh	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)
Dual Output Fast read	3Bh	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)(7)
Quad Output Fast read	6Bh	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)(9)
Erase Security Registers(5)	44h	A23-A16(8)	A15-A8(8)	A7-A0(8)		
Program Security Registers(5)	42h	A23-A16(8)	A15-A8(8)	A7-A0(8)	D7-D0	Next Byte
Read Security Registers(5)	48h	A23-A16(8)	A15-A8(8)	A7-A0(8)	Dummy	D7-D0

Data Input Output	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
Clock Number	**(0-7)**	**(8-11)**	**(12-15)**	**(16-19)**	**(20-23)**	**(24-27)**	**(28-31)**
Dual I/O Fast read	BBh	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)	
Mftr./Device ID Dual I/O	92h	A23-A16	A15-A8	A7-A0	Dummy	(MF7-MF0)	(ID7-ID0)

Data Input Output	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7	Byte 8	Byte 9
Clock Number	**(0-7)**	**(8-9)**	**(10-11)**	**(12-13)**	**(14-15)**	**(16-17)**	**(18-19)**	**(20-21)**	**(22-23)**
Set Burst With Wrap	77h	Dummy	Dummy	Dummy	W6-W4				
Quad I/O Fast read	EBh	A23-A16	A15-A8	A7-A0	M7-M0	Dummy	Dummy	(D7-D0)	(D7-D0)
Word Read Quad I/O(12)	E7h	A23-A16	A15-A8	A7-A0	M7-M0	Dummy	(D7-D0)	(D7-D0)	(D7-D0)
Mftr./Device ID Quad I/O	94h	A23-A16	A15-A8	A7-A0	M7-M0	Dummy	Dummy	(MF7-MF0)	(ID7-ID0)
Read SPB Status	E2h	A23-A16	A15-A8	A7-A0	(D7-D0)				
SPB Program	E3h	A23-A16	A15-A8	A7-A0					
Read DPB Status	3Dh	A23-A16	A15-A8	A7-A0	(D7-D0)				
Dynamic Protection Block/Sector Lock	36h	A23-A16	A15-A8	A7-A0					
Dynamic Protection Block/Sector Unlock	39h	A23-A16	A15-A8	A7-A0					
Enter 4-Byte Address Mode	B7h								
Read Extended Addr. Register	C8h	(EA7-EA0)(2)							
Write Extended Addr. Register	C5h	(EA7-EA0)							

Instruction Set Table-Standard/Dual/Quad SPI Instructions, 4-Byte Address Mode [1]

Data Input Output	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
Clock Number	**(0-7)**	**(8-15)**	**(16-23)**	**(24-31)**	**(32-39)**	**(40-47)**	**(48-63)**
Read Unique ID Number	4Bh	Dummy	Dummy	Dummy	Dummy	Dummy	(ID127-ID0)
Clock Number	**(0-7)**	**(8-15)**	**(16-23)**	**(24-31)**	**(32-39)**	**(40-47)**	**(48-55)**
Page Program	02h	A31-A24	A23-A16	A15-A8	A7-A0	(D7-D0)	(D7-D0)[3]
Quad Page Program	32h	A31-A24	A23-A16	A15-A8	A7-A0	(D7-D0, …)[9]	(D7-D0, …)[3]
Sector Erase (4KB)	20h	A31-A24	A23-A16	A15-A8	A7-A0		
Block Erase (32KB)	52h	A31-A24	A23-A16	A15-A8	A7-A0		
Block Erase (64KB)	D8h	A31-A24	A23-A16	A15-A8	A7-A0		
Normal Read Data	03h	A31-A24	A23-A16	A15-A8	A7-A0	(D7-D0)	(Next Byte)
Fast Read	0Bh	A31-A24	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)
Dual Output Fast read	3Bh	A31-A24	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)[7]
Quad Output Fast read	6Bh	A31-A24	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)[9]
Erase Security Registers[5]	44h	A31-A24	A23-A16[8]	A15-A8[8]	A7-A0[8]		
Program Security Registers[5]	42h	A31-A24	A23-A16[8]	A15-A8[8]	A7-A0[8]	D7-D0	Next Byte
Read Security Registers[5]	48h	A31-A24	A23-A16[8]	A15-A8[8]	A7-A0[8]	Dummy	D7-D0

Data Input Output	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7	Byte 8
Clock Number	**(0-7)**	**(8-11)**	**(12-15)**	**(16-19)**	**(20-23)**	**(24-27)**	**(28-31)**	**(22-35)**
Dual I/O Fast read	BBh	A31-A24	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)	(D7-D0)
Mftr./Device ID Dual I/O	92h	A31-A24	A23-A16	A15-A8	A7-A0	Dummy	(MF7-MF0)	(ID7-ID0)

Data Input Output	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7	Byte 8	Byte 9	Byte 10
Clock Number	**(0-7)**	**(8-9)**	**(10-11)**	**(12-13)**	**(14-15)**	**(16-17)**	**(18-19)**	**(20-21)**	**(22-23)**	**(24-25)**
Set Burst With Wrap	77h	Dummy	Dummy	Dummy	Dummy	W6-W4				
Quad I/O Fast read	EBh	A31-A24	A23-A16	A15-A8	A7-A0	M7-M0	Dummy	Dummy	(D7-D0)	(D7-D0)
Word Read Quad I/O[12]	E7h	A31-A24	A23-A16	A15-A8	A7-A0	M7-M0	Dummy	(D7-D0)	(D7-D0)	(D7-D0)
Mftr./Device ID Quad I/O	94h	A31-A24	A23-A16	A15-A8	A7-A0	M7-M0	Dummy	Dummy	(MF7-MF0)	(D7-D0)
Read SPB Status	E2h	A31-A24	A23-A16	A15-A8	A7-A0	(D7-D0)				
SPB Program	E3h	A31-A24	A23-A16	A15-A8	A7-A0					
Read DPB Status	3Dh	A31-A24	A23-A16	A15-A8	A7-A0	(D7-D0)				
Dynamic Protection Block/Sector Lock	36h	A31-A24	A23-A16	A15-A8	A7-A0					
Dynamic Protection Block/Sector Unlock	39h	A31-A24	A23-A16	A15-A8	A7-A0					
Exit 4-Byte Address Mode	E9h									

Instruction Set Table-QPI Instructions, 3-Byte & 4-Byte Address Mode (14)

Data Input Output	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7	Byte 8
Clock Number	(0-1)	(2-3)	(4- 5)	(6- 7)	(8-9)	(10-11)	(12-13)	(14-15)
Write Enable	06h							
Volatile SR Write Enable	50h							
Write Disable	04h							
Read Status Register-1	05h	(S7-S0)(2)						
Write Status Register(4)	01h	(S7-S0)(4)	(S15-S8)					
Read Status Register-2	35h	(S15-S8)(2)						
Write Status Register-2	31h	(S15-S8)						
Read Status Register-3	15h	(S23-S16)(2)						
Write Status Register-3	11h	(S23-S16)						
Chip Erase	C7h/60h							
Erase / Program Suspend	75h							
Erase / Program Resume	7Ah							
Power-down	B9h							
Set Read Parameters	C0h	P7-P0						
Release Powerdown / ID	ABh	Dummy	Dummy	Dummy	(ID7-ID0)(2)			
Manufacturer/Device ID	90h	Dummy	Dummy	00h	(MF7-MF0)	(ID7-ID0)		
JEDEC ID	9Fh	(MF7-MF0)	(ID15-ID8)	(ID7-ID0)				
Exit QPI Mode	FFh							
Enable Reset	66h							
Reset Device	99h							
Fast Read Quad I/O with 4-Byte Address	ECh	A31-A24	A23-A16	A15-A8	A7-A0	M7-M0(15)	Dummy	(D7-D0)
Read Serial Flash Discoverable Parameter	5Ah	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)		
Page Program with 4-Byte Address	12h	A31-A24	A23-A16	A15-A8	A7-A0	(D7-D0)	(D7-D0)(3)	
Sector Erase (4KB) with 4-Byte Address	21h	A31-A24	A23-A16	A15-A8	A7-A0			
Block Erase(32K) with 4-Byte Address	5Ch	A31-A24	A23-A16	A15-A8	A7-A0			
Block Erase(64K) with 4-Byte Address	DCh	A31-A24	A23-A16	A15-A8	A7-A0			
Read Lock Register	2Dh	(S7-S0)	Next Byte					
Write Lock Register	2Ch	(S7-S0)	(S15-S8)					
SPB Lock Bit Clear	A6h							
Read SPB Lock Register	A7h	(S7-S0)	Next Byte					
SPB Erase	E4h							
Read Unprotect Solid Protect Bit	AAh	(S7-S0)	Next Byte					
Unprotect Solid Protect Bit Set	A8h							
Unprotect Solid Protect Bit Clear	A9h							

Data Input Output	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7	Byte 8	Byte 9	Byte 10
Clock Number	(0-1)	(2-3)	(4- 5)	(6- 7)	(8-9)	(10-11)	(10-11)	(12-13)	(14-15)	(16-17)
Read Password Register	27h	(P7-P0)	(P15-P8	(P23-P16)	(P31-P24)	(P39-P32)	(P47-P40)	(P55-P48)	(P63-P56)	Next Byte
Write Password Register	28h	(P7-P0)	(P15-P8	(P23-P16)	(P31-P24)	(P39-P32)	(P47-P40)	(P55-P48)	(P63-P56)	
Password Unlock	29h	(P7-P0)	(P15-P8	(P23-P16)	(P31-P24)	(P39-P32)	(P47-P40)	(P55-P48)	(P63-P56)	

Instruction Set Table-QPI Instructions, 3-Byte Address Mode (14)

Data Input Output	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
Clock Number	**(0-1)**	**(2-3)**	**(4-5)**	**(6-7)**	**(8-9)**	**(10-11)**	**(12-13)**
Page Program	02h	A23-A16	A15-A8	A7-A0	D7-D0(9)	D7-D0(3)	
Sector Erase (4KB)	20h	A23-A16	A15-A8	A7-A0			
Block Erase (32KB)	52h	A23-A16	A15-A8	A7-A0			
Block Erase (64KB)	D8h	A23-A16	A15-A8	A7-A0			
Fast Read	0Bh	A23-A16	A15-A8	A7-A0	Dummy(15)	(D7-D0)	
Burst Read with Wrap(16)	0Ch	A23-A16	A15-A8	A7-A0	Dummy(15)	(D7-D0)	
Fast Read Quad I/O	EBh	A23-A16	A15-A8	A7-A0	M7-M0(15)	Dummy	(D7-D0)
Read Unique ID Number	4Bh	Dummy	Dummy	Dummy	Dummys*	(ID127-ID0)	
Read Security Registers(5)	48h	A23-A16(8)	A15-A8(8)	A7-A0(8)	Dummy	D7-D0	
Erase Security Registers(5)	44h	A23-A16(8)	A15-A8(8)	A7-A0(8)			
Program Security Registers(5)	42h	A23-A16(8)	A15-A8(8)	A7-A0(8)	D7-D0	Next Byte	
Read SPB Status	E2h	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)	
SPB Program	E3h	A23-A16	A15-A8	A7-A0			
Read DPB Status	3Dh	A23-A16	A15-A8	A7-A0	(D7-D0)		
Dynamic Protection Block/Sector Lock	36h	A23-A16	A15-A8	A7-A0			
Dynamic Protection Block/Sector Unlock	39h	A23-A16	A15-A8	A7-A0			
Enter 4-Byte Address Mode	B7h						
Read Extended Addr. Register	C8h	(EA7-EA0)(2)					
Write Extended Addr. Register	C5h	(EA7-EA0)					

Instruction Set Table-QPI Instructions, 4-Byte Address Mode (14)

Data Input Output	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7	Byte 8
Clock Number	**(0-1)**	**(2-3)**	**(4-5)**	**(6-7)**	**(8-9)**	**(10-11)**	**(12-13)**	**(13-14)**
Page Program	02h	A31-A24	A23-A16	A15-A8	A7-A0	D7-D0(9)	D7-D0(3)	
Sector Erase (4KB)	20h	A31-A24	A23-A16	A15-A8	A7-A0			
Block Erase (32KB)	52h	A31-A24	A23-A16	A15-A8	A7-A0			
Block Erase (64KB)	D8h	A31-A24	A23-A16	A15-A8	A7-A0			
Fast Read	0Bh	A31-A24	A23-A16	A15-A8	A7-A0	Dummy(15)	(D7-D0)	
Burst Read with Wrap(16)	0Ch	A31-A24	A23-A16	A15-A8	A7-A0	Dummy(15)	(D7-D0)	
Fast Read Quad I/O	EBh	A31-A24	A23-A16	A15-A8	A7-A0	M7-M0(15)	Dummy	(D7-D0)
Read Unique ID Number	4Bh	Dummy	Dummy	Dummy	Dummy	Dummys*	(ID127-ID0)	
Read Security Registers(5)	48h	A31-A24	A23-A16(8)	A15-A8(8)	A7-A0(8)	Dummy	D7-D0	
Erase Security Registers(5)	44h	A31-A24	A23-A16(8)	A15-A8(8)	A7-A0(8)			
Program Security Registers(5)	42h	A31-A24	A23-A16(8)	A15-A8(8)	A7-A0(8)	D7-D0	Next Byte	
Read SPB Status	E2h	A31-A24	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)	
SPB Program	E3h	A31-A24	A23-A16	A15-A8	A7-A0			
Read DPB Status	3Dh	A31-A24	A23-A16	A15-A8	A7-A0	(D7-D0)		
Dynamic Protection Block/Sector Lock	36h	A31-A24	A23-A16	A15-A8	A7-A0			
Dynamic Protection Block/Sector Unlock	39h	A31-A24	A23-A16	A15-A8	A7-A0			
Exit 4-Byte Address Mode	E9h							

Instruction Set Table-DTR with SPI Instructions, 3-Byte & 4-Byte Address Mode (14)

Data Input Output	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
Clock Number(1-1-1)	**8**	**4**	**4**	**4**	**6**	**4**	**4**
DTR Quad I/O Fast Read with 4- Byte Address	EEh	A31-A24	A23-A16	A15-A8	A7-A0	M7-M0	(D7-D0)

Instruction Set Table-DTR with QPI Instructions, 3-Byte & 4-Byte Address Mode (14)

Data Input Output	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
Clock Number(1-1-1)	**8**	**4**	**4**	**4**	**6**	**4**	**4**
DTR Quad I/O Fast Read with 4- Byte Address	EEh	A31-A24	A23-A16	A15-A8	A7-A0	M7-M0	(D7-D0)

Instruction Set Table-DTR with SPI Instructions, 3-Byte Address Mode (14)

Data Input Output	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
Clock Number(1-1-1)	**8**	**4**	**4**	**4**	**6**	**4**	**4**
DTR Fast Read	0Dh	A23-A16	A15-A8	A7-A0	Dummy	D7-D0	
Clock Number(1-2-2)	**8**	**2**	**2**	**2**	**2**	**4**	**2**
DTR Fast Read Dual I/O	BDh	A23-A16	A15-A8	A7-A0	M7-M0	Dummy	(D7-D0)
Clock Number(1-4-4)	**8**	**1**	**1**	**1**	**1**	**7**	**1**
DTR Fast Read Quad I/O	EDh	A23-A16	A15-A8	A7-A0	M7-M0	Dummy	(D7-D0)

Instruction Set Table-DTR with SPI Instructions, 4-Byte Address Mode (14)

Data Input Output	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
Clock Number(1-1-1)	**8**	**4**	**4**	**4**	**6**	**4**	**4**
DTR Fast Read	0Dh	A31-A24	A23-A16	A15-A8	A7-A0	Dummy	D7-D0
Clock Number(1-2-2)	**8**	**2**	**2**	**2**	**2**	**4**	**2**
DTR Fast Read Dual I/O	BDh	A31-A16	A15-A0	M7-M0	Dummy	(D7-D0)	
Clock Number(1-4-4)	**8**	**1**	**1**	**1**	**1**	**7**	**1**
DTR Fast Read Quad I/O	EDh	A31-A16	A15-A0	M7-M0	Dummy	(D7-D0)	

Instruction Set Table-DTR with QPI Instructions, 3-Byte Address Mode (14)

Data Input Output	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
Clock Number(4-4-4)	**2**	**1**	**1**	**1**	**8**	**1**	**1**
DTR Read with Wrap(13)	0Eh	A23-A16	A15-A8	A7-A0	Dummy	D7-D0	
DTR Fast Read	0Dh	A23-A16	A15-A8	A7-A0	Dummy	D7-D0	
Clock Number(4-4-4)	**2**	**1**	**1**	**1**	**1**	**7**	**1**
DTR Fast Read Quad I/O	EDh	A23-A16	A15-A8	A7-A0	M7-M0	Dummy	(D7-D0)

Instruction Set Table-DTR with QPI Instructions, 4-Byte Address Mode (14)

Data Input Output	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7	Byte 8
Clock Number(4-4-4)	**2**	**1**	**1**	**1**	**61**	**8**	**1**	**1**
DTR Read with Wrap(13)	0Eh	A31-A24	A23-A16	A15-A8	A7-A0	Dummy	D7-D0	
DTR Fast Read	0Dh	A31-A24	A23-A16	A15-A8	A7-A0	Dummy	D7-D0	
Clock Number(4-4-4)	**2**	**1**	**1**	**1**	**1**	**1**	**7**	**1**
DTR Fast Read Quad I/O	EDh	A31-A24	A23-A16	A15-A8	A7-A0	M7-M0	Dummy	(D7-D0)

Notes:

1. Data bytes are shifted with Most Significant Bit first. Byte fields with data in parenthesis “( )” indicate data output from the device on either 1, 2 or 4 IO pins.

2. The Status Register contents and Device ID will repeat continuously until /CS terminates the instruction.

3. At least one byte of data input is required for Page Program, Quad Page Program and Program Security Registers, up to 256 bytes of data input. If more than 256 bytes of data are sent to the device, the addressing will wrap to the beginning of the page and overwrite previously sent data.

4. When the Write Status Register instruction 01h is followed by 1 byte data, the data will be written to Status Register-1. When the Write Status Register instruction 01h is followed by 2 bytes of data, the first byte data will be written to Status Register-1, and the second byte data will be written to Status Register-2, see ***Write Status Register (01H or 31H or 11H)***.

5. Security Register Address:
Security Register 1: A23-16=00h; A15-12=0001; A11-9=000; A8-0=byte address
Security Register 2: A23-16=00h; A15-12=0010; A11-9=000; A8-0=byte

address
Security Register 3: A23-16=00h; A15-12=0011; A11-9=000; A8-0=byte address

6. Dual SPI address input format:
IO0 = A22, A20, A18, A16, A14, A12, A10, A8 A6, A4, A2, A0, M6, M4, M2, M0
IO1 = A23, A21, A19, A17, A15, A13, A11, A9 A7, A5, A3, A1, M7, M5, M3, M1

7. Dual SPI data output format:
IO0 = (D6, D4, D2, D0)
IO1 = (D7, D5, D3, D1)

8. Quad SPI address input format:
IO0 = A20, A16, A12, A8, A4, A0, M4, M0
IO1 = A21, A17, A13, A9, A5, A1, M5, M1
IO2 = A22, A18, A14, A10, A6, A2, M6, M2
IO3 = A23, A19, A15, A11, A7, A3, M7, M3

Set Burst with Wrap input format:
IO0 = x, x, x, x, x, x, W4, x
IO1 = x, x, x, x, x, x, W5, x
IO2 = x, x, x, x, x, x, W6, x
IO3 = x, x, x, x, x, x, x, x

9. Quad SPI data input/output format:
IO0 = (D4, D0, …..)
IO1 = (D5, D1, …..)
IO2 = (D6, D2, …..)
IO3 = (D7, D3, …..)

10. Fast Read Quad I/O data output format:
IO0 = (x, x, x, x, D4, D0, D4, D0)
IO1 = (x, x, x, x, D5, D1, D5, D1)
IO2 = (x, x, x, x, D6, D2, D6, D2)
IO3 = (x, x, x, x, D7, D3, D7, D3)

11. Word Read Quad I/O data output format:
IO0 = (x, x, D4, D0, D4, D0, D4, D0)
IO1 = (x, x, D5, D1, D5, D1, D5, D1)
IO2 = (x, x, D6, D2, D6, D2, D6, D2)
IO3 = (x, x, D7, D3, D7, D3, D7, D3)

12. For Word Read Quad I/O, the lowest address bit must be 0. (A0 = 0)

13. For Octal Word Read Quad I/O, the lowest four address bits must be 0. (A3, A2, A1, A0 = 0)

14. QPI Instruction, Address, Data input/output format:

CLK # 0	1	2	3	4	5	6	7	8	9	10	11
IO0 = C4, C0,		A20, A16,		A12, A8,		A4, A0,		D4, D0,		D4, D0	
IO1 = C5, C1,		A21, A17,		A13, A9,		A5, A1,		D5, D1,		D5, D1	
IO2 = C6, C2,		A22, A18,		A14, A10,		A6, A2,		D6, D2,		D6, D2	
IO3 = C7, C3,		A23, A19,		A15, A11,		A7, A3,		D7, D3,		D7, D3	

15. The number of dummy clocks for QPI Fast Read, QPI Fast Read Quad I/O & QPI Burst Read with Wrap is controlled by read parameter P7 – P4.

16. The wrap around length for QPI Burst Read with Wrap is controlled by read parameter P3 – P0.

Table 20. Instructions that need to send the Write Enable/Write Enable for Volatile Status Register instruction

Mode	Instruction		Write
SPI/QPI	Write Status Register	01h/31h/11h	06H/50H
	Write Extended Address Register	C5h	06H
	Erase Security Registers	44h	06H
	Program Security Registers	42h	06H
	Page Program	02h	06H
	Page Program with 4-Byte Address	12h	06H
SPI	Quad Page Program	32h	06H
	Quad Input Page Program with 4-Byte Address	34h	06H
SPI/QPI	Sector Erase	20h	06H
	Sector Erase with 4-Byte Address	21h	06H
	32KB Block Erase	52h	06H
	32KB Block Erase with 4-Byte Address	5Ch	06H
	64KB Block Erase	D8h	06H
	64KB Block Erase with 4-Byte Address	DCh	06H
	Chip Erase	60h/C7h	06H
	Write Lock Register	2Ch	06H
	SPB Lock Bit Clear	A6h	06H
	SPB Program	E3h	06H
	SPB Erase	E4h	06H
	Dynamic Protection Block/Sector Lock	36h	06H
	Dynamic Protection Block/Sector Unlock	39h	06H
	Unprotect Solid Protect Bit Set	A8h	06H
	Unprotect Solid Protect Bit Clear	A9h	06H
	Global Block/Sector Lock	7Eh	06H
	Global Block/Sector Unlock	98h	06H
	Write Password Register	28h	06H
	Password Unlock	29h	06H

7.1 Configuration and Status Instructions

7.1.1 Software Die Select (C2H)

Each stacked die has a pre-assigned “Die ID#” by the factory, in the sequence of 0x00, 0x01, etc. At any given time, there can only be one Active Die within the BY25QM1GFS package, to communicate with the external SPI controller. After power-up, Die #0 is always the Active Die. Software Die Select (C2h) instruction is used to select a specific die to be active, according to the 8-bit Die ID following the C2h instruction as shown in ***Figure 11-Figure 12.***

“ Concurrent Operations” can be realized by assigning the current Active Die to perform an Erase/Program operation which requires some amount of time to finish. While the internal Program/Erase operation is ongoing, the controller can issue a “Software Die Select (C2h)” instruction to select another die to be active. Depending on the system requirement, a Read, Program or Erase operation can be performed on the newly selected Active Die. “Read while Program/Erase” or “Multi-Die Program/Erase” can be performed in such fashion, to improve system Program/Erase throughput and to avoid constant Program/Erase Suspend and Resume activities in certain applications.

The Software Die Select instruction sequence: /CS goes low sending the Software Die Select instruction and Die ID, /CS goes high.

Figure 11. Software Die Select Sequence Diagram (SPI Mode)

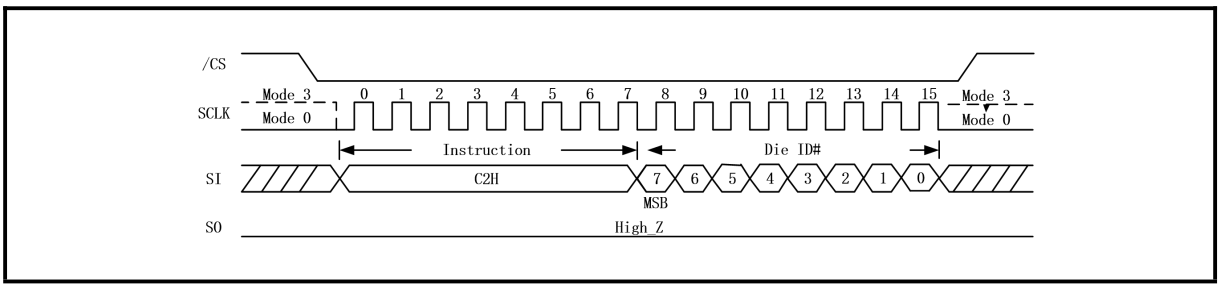
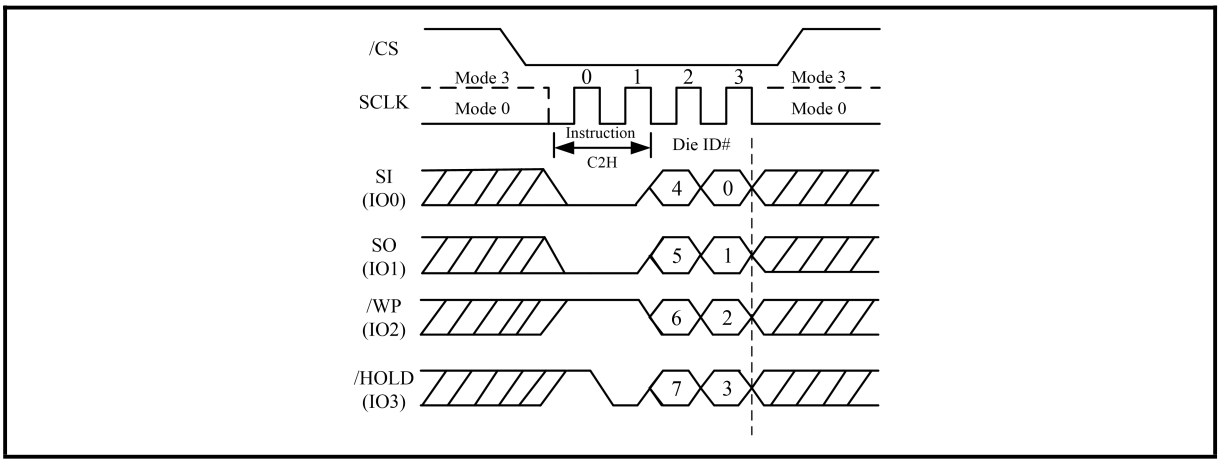


Figure 12. Software Die Select Sequence Diagram (QPI Mode)



7.1.2 Read Active Die ID# (F8H)

The Read Active Die ID# command is used to read ID of active die within the MCP package, and each bit being latched-in on the rising edge of SCLK. Then the active die ID# is shifted out on SO, and each bit being shifted out, at a Max frequency fR, on the falling edge of SCLK. The Active Die ID# may be read at any time, even while a Program, Erase or Read cycle is in progress.

Figure 13. Read Active Die ID# Sequence Diagram (SPI Mode)

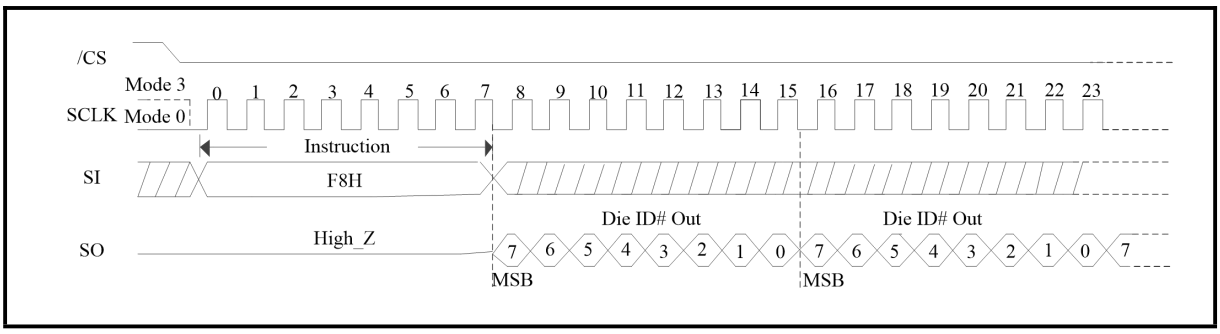
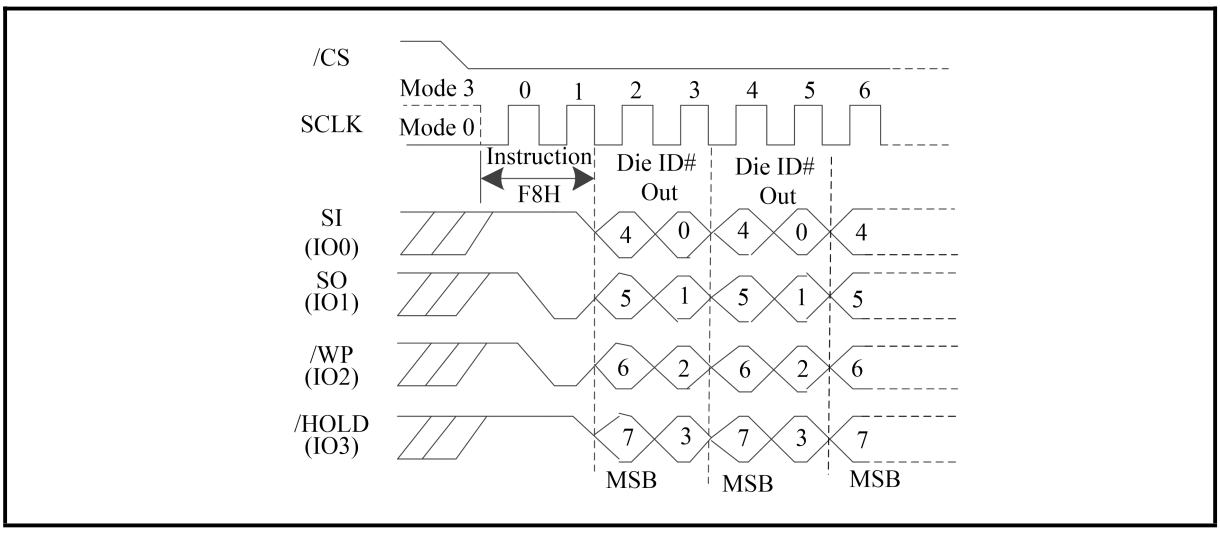


Figure 14. Read Active Die ID# Sequence Diagram (QPI Mode)



7.1.3 Write Enable (06H)

See ***Figure 15-Figure 16***， the Write Enable instruction is for setting the Write Enable Latch bit. The Write Enable Latch bit must be set prior to every Write Status Register, Program, Erase and some Advanced Block/Sector Protection instruction (see ***Table 20***). The Write Enable instruction sequence: /CS goes low sending the Write Enable instruction, /CS goes high.

Please note that the Write Enable instruction sent when the Write Enable for Volatile Status Register instruction is valid is not accepted. Therefore, when need to send the Write Enable instruction, but do not know if the Write Enable for Volatile Status Register instruction is valid, please send the Write Disable instruction first.

Figure 15. Write Enable Sequence Diagram (SPI Mode)

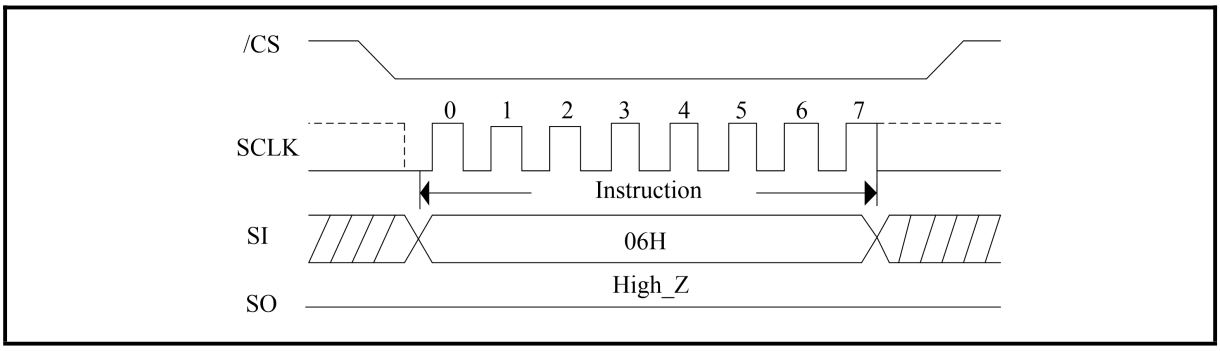
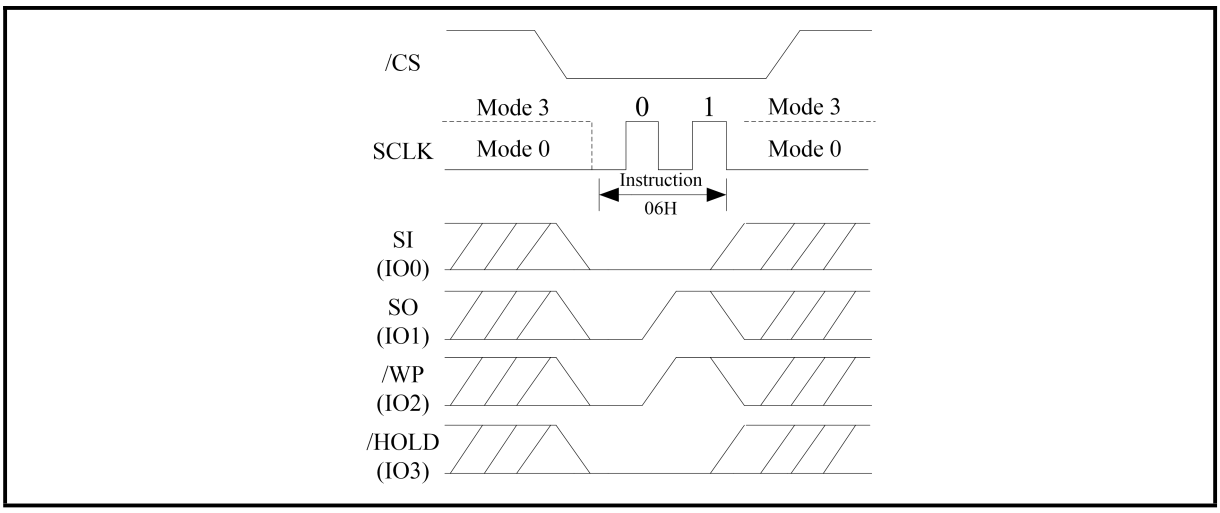


Figure 16. Write Enable Sequence Diagram (QPI Mode)



7.1.4 Write Enable for Volatile Status Register (50H)

See ***Figure 17-Figure 18***, the non-volatile Status Register bits can also be written to as volatile bits (HOLD/RES, DRV1, DRV0, CMP, QE, SRP1, SRP0, BP4, BP3, BP2, BP1, BP0). This gives more flexibility to change the system configuration and memory protection schemes quickly without waiting for the typical non-volatile bit write cycles or affecting the endurance of the Status Register non-volatile bits. Write Enable for Volatile Status Register instruction will not set the Write Enable Latch bit, it is only valid for the Write Status Registers instruction to change the volatile Status Register bit values (After the software/hardware reset or re-powered, the volatile Status Register bit values will be restored to the default value or the value input by the Write Enable instruction).

Please note that the Write Enable for Volatile Status Register instruction sent when the Write Enable instruction is valid is not accepted. Therefore, when need to send the Write Enable for Volatile Status Register instruction, please first determine whether the Write Enable instruction is not valid.

Figure 17. Write Enable for Volatile Status Register (SPI Mode)

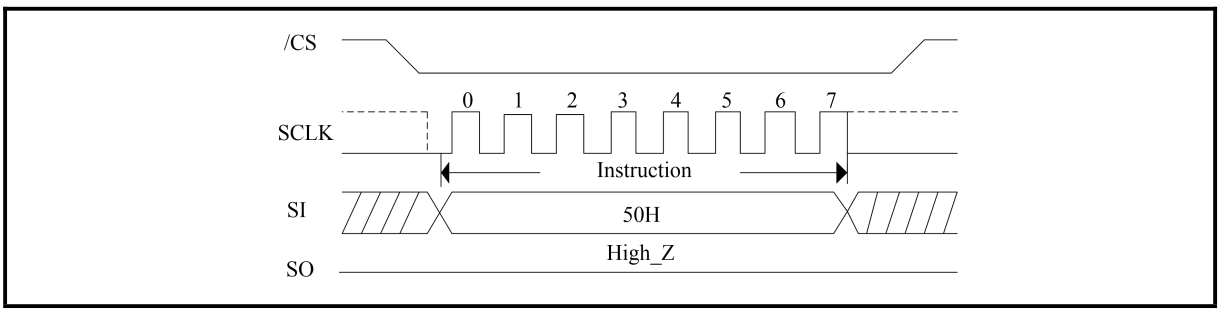
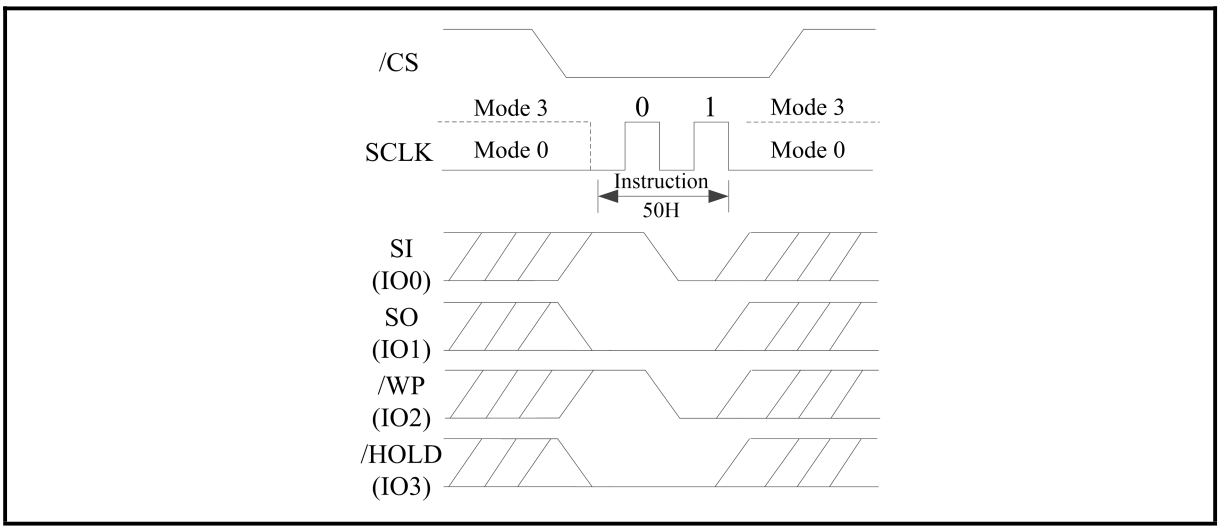


Figure 18. Write Enable for Volatile Status Register (QPI Mode)



7.1.5 Write Disable (04H)

See ***Figure 19-Figure 20***, the Write Disable instruction is for resetting the Write Enable Latch bit or invalidate the Write Enable for Volatile Status Register instruction. The Write Disable instruction sequence: /CS goes low -> sending the Write Disable instruction -> /CS goes high. The WEL bit is reset by following condition: Power-up and upon completion of the Write Status Register, Page Program, Sector Erase, Block Erase and Chip Erase, Program/Erase Security Registers and Reset instructions.

Figure 19. Write Disable Sequence Diagram (SPI Mode)

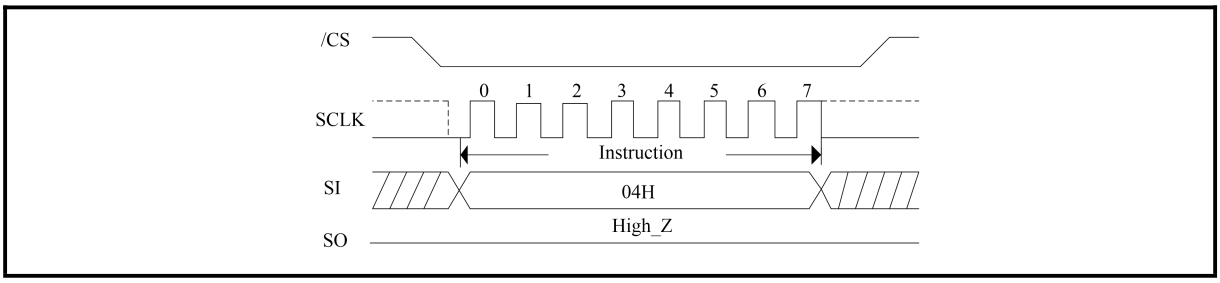
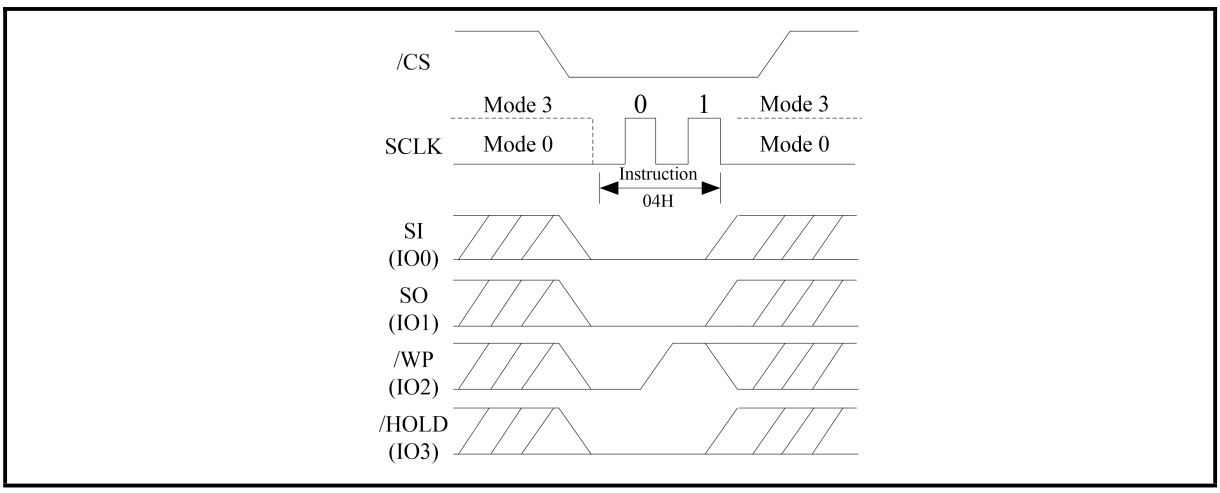


Figure 20. Write Disable Sequence Diagram (QPI Mode)



7.1.6 Read Status Register (05H or 35H or 15H)

See ***Figure 21-Figure 22***, the Read Status Register (RDSR) instruction is for reading the Status Register. The Status Register may be read at any time, even while a Program, Erase or Write Status Register cycle is in progress. When one of these cycles is in progress, it is recommended to check the Write in Progress (WIP) bit before sending a new instruction to the device. It is also possible to read the Status Register continuously. For instruction code “05H”, the SO will output Status Register bits S7~S0. The instruction code “35H”, the SO will output Status Register bits S15~S8, The instruction code “15H”, the SO will output Status Register bits S23~16.

Figure 21. Read Status Register Sequence Diagram (SPI Mode)

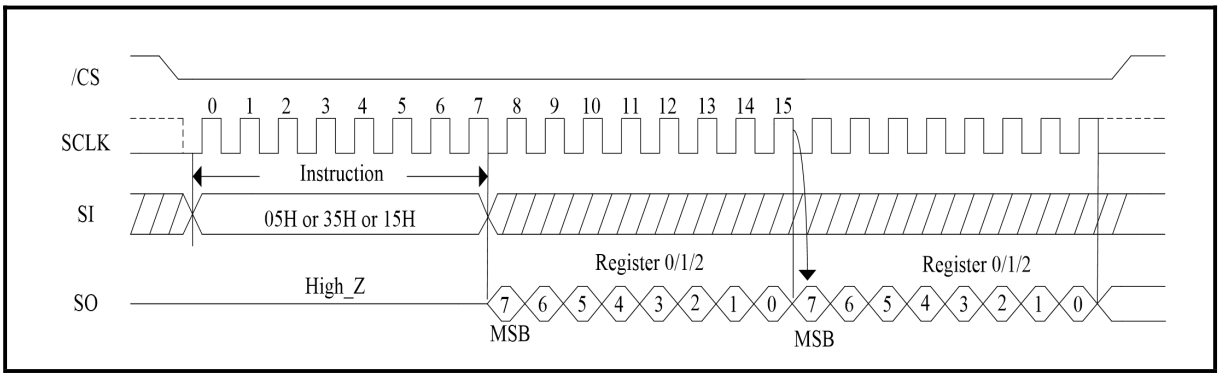
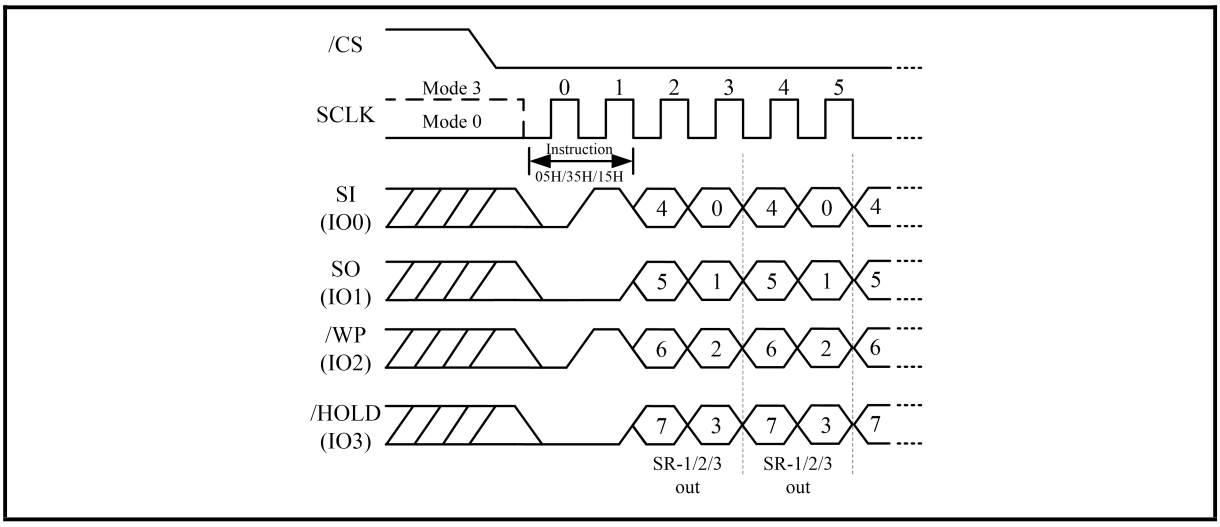


Figure 22. Read Status Register Sequence Diagram (QPI Mode)



7.1.7 Write Status Register (01H or 31H or 11H)

The Write Status Register instruction allows the Status Registers to be written. The Status Register-1 can be written by the Write Status Register 01h instruction; The Status Register-2 be written by the Write Status Register 01h or 31h instruction; Status Register-3 can be written by the Write Status Register 11h instruction. When the Write Status Register instruction 01h is followed by 1 byte data, the data will be written to Status Register-1. When the Write Status Register instruction 01h is followed by 2 bytes of data, the first byte data will be written to Status Register-1, and the second byte data will be written to Status Register-2; And Write Status Register instruction 31h or 11h can only follow 1 byte data, the data will be written to Status Register-2、Status Register-3 respectively. The writable Status Register bits include: SRP0, BP[4:0] in Status Register-1; CMP, LB[3:1], QE, SRP1 in Status Register- 2; ADS, ADP, DRV1, DRV0, Hold/RES in Status Register- 3. All other Status Register bit locations are read-only and will not be affected by the Write Status Register instruction. LB[3:1] are non-volatile OTP bits, once it is set to 1, it cannot be cleared to 0.

The Write Status Register instruction allows new values to be written to the Status Register. Before it can be accepted, a Write Enable or Write Enable For Volatile SR instruction must previously have been executed After the Write Enable instruction has been decoded and executed, the device sets the Write Enable Latch (WEL).

The Write Status Register instruction has no effect on S15 (SUS1), S10 (SUS2), S1 (WEL) and S0 (WIP) of the Status Register. /CS must be driven high after the 8 or 16 bit of the data byte has been latched in. If not, the Write Status Register (WRSR) instruction is not executed. As soon as /CS is driven high, the self-timed Write Status Register cycle (whose duration is tW) is initiated. While the Write Status Register cycle is in progress, the Status Register may still be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Write Status Register cycle, and is 0 when it is completed. When the cycle is completed, the Write Enable Latch (WEL) is reset.

The Write Status Register instruction allows the user to change the values of the Block Protect (BP4, BP3, BP2, BP1, and BP0) bits, to define the size of the area that is to be treated as read-only, as defined in ***Table 9*** and ***Table 10***. The Write Status Register (WRSR) instruction also allows the user to set or reset the Status Register Protect (SRP1 and SRP0) bits in accordance with the Write Protect (/WP) signal. The Status Register Protect (SRP1 and SRP0) bits and Write Protect (/WP) signal allow the device to be put in the Hardware Protected Mode. The Write Status Register instruction is not executed once the Hardware Protected Mode is entered.

The sequence of issuing WRSR instruction is: /CS goes low→ sending WRSR instruction code→ Status Register data on SI→/CS goes high.

The /CS must go high exactly at the 8 bits or 16 bits data boundary; otherwise, the instruction will be rejected and not executed. The self-timed Write Status Register cycle time (tW) is initiated as soon as Chip Select (/CS) goes high. The Write in Progress (WIP) bit still can be checked during the Write Status Register cycle is in progress. The WIP is set 1 during the tW timing, and is set 0 when Write Status Register Cycle is completed, and the Write Enable Latch (WEL) bit is reset.

Figure 23. Write Status Register Sequence Diagram-01H 2byte (SPI Mode)

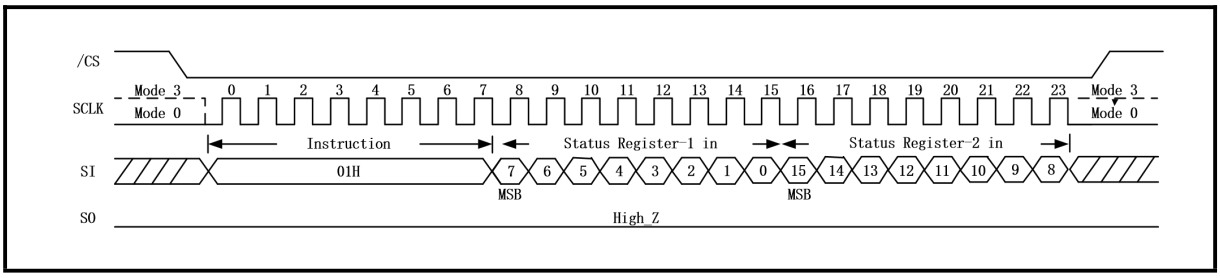


Figure 24. Write Status Register Sequence Diagram-01H 2byte (QPI Mode)

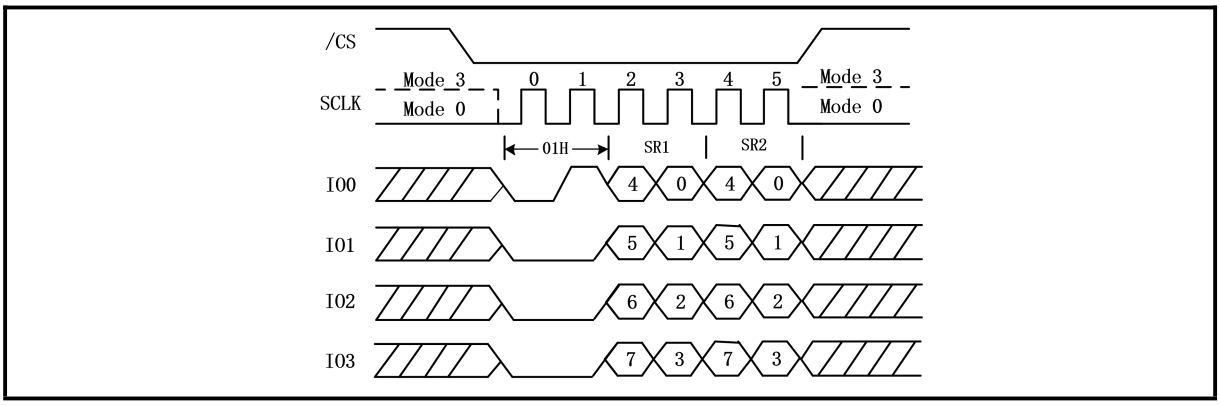


Figure 25. Write Status Register Sequence Diagram-01/31/11H 1byte (SPI Mode)

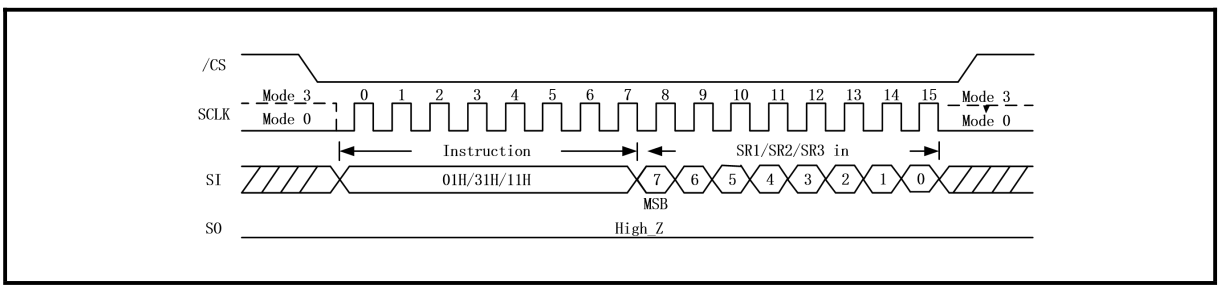
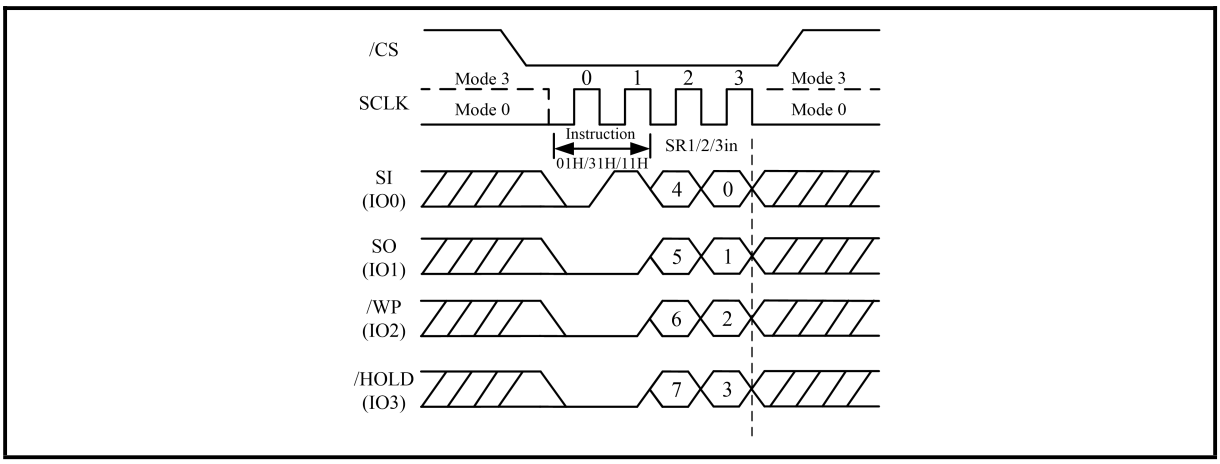


Figure 26. Write Status Register Sequence Diagram-01/31/11H 1byte (QPI Mode)



7.1.8 Read Extended Address Register (C8H)

When the device is in the 3-Byte Address Mode, the Extended Address Register is used as the 4th address byte A[31:24] to access memory regions beyond 128Mb. The Read Extended Address Register instruction is entered by driving /CS low and shifting the instruction code “C8h” into the SI pin on the rising edge of CLK. The Extended Address Register bits are then shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first as shown in ***Figure 27-Figure 28***.

When the device is in the 4-Byte Address Mode, the Extended Address Register is not used.

Figure 27. Read Extended Address Register (SPI Mode)

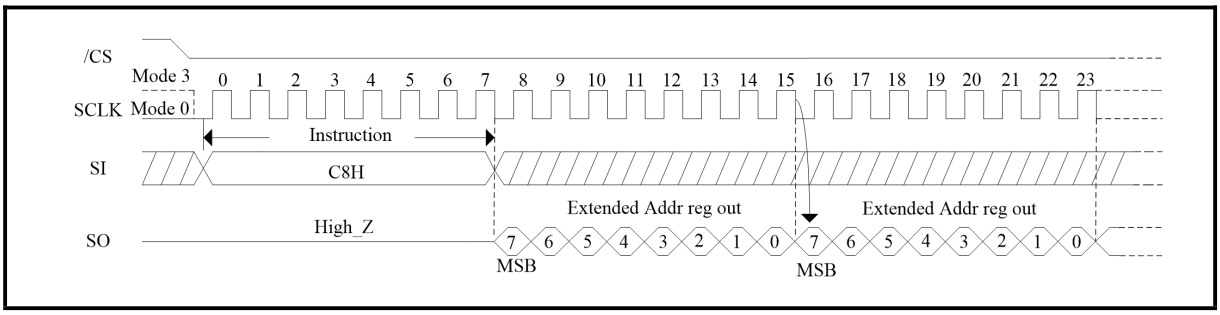
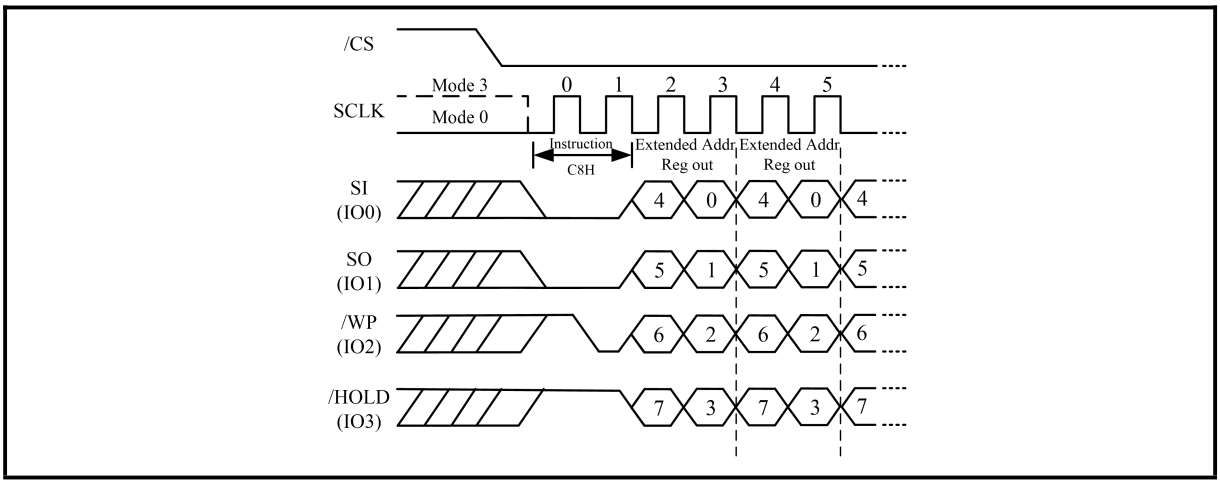


Figure 28. Read Extended Address Register (QPI Mode)



7.1.9 Write Extended Address Register (C5H)

The Extended Address Register is a volatile register that stores the 4th byte address (A31-A24) when the device is operating in the 3-Byte Address Mode (ADS=0). To write the Extended Address Register bits, a Write Enable (06h) instruction must previously have been executed for the device to accept the Write Extended Address Register instruction (Status Register bit WEL must equal 1). Once write enabled, the instruction is entered by driving /CS low, sending the instruction code "C5h", and then writing the Extended Address Register data byte as shown in ***Figure 29-Figure 30***.

Upon power up or the execution of a Software reset, the Extended Address Register bit values will be cleared to 0.

The Extended Address Register is only effective when the device is in the 3-Byte Address Mode. When the device operates in the 4-Byte Address Mode (ADS=1), any instruction with address input of A31-A24 will replace the Extended Address Register values. It is recommended to check and update the Extended Address Register if necessary when the device is switched from 4-Byte to 3-Byte Address Mode.

Figure 29. Write Extended Address Register (SPI Mode)

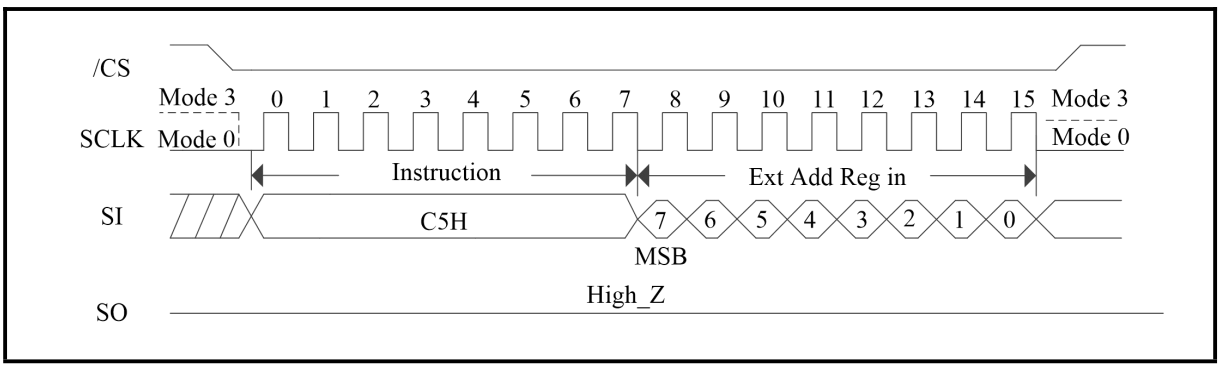
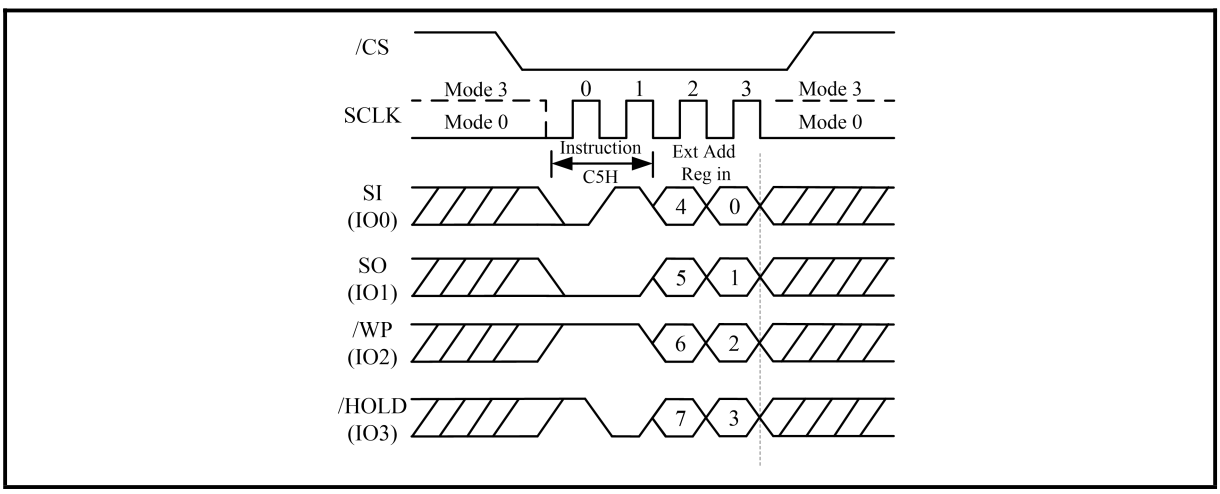


Figure 30. Write Extended Address Register (QPI Mode)



7.1.10 Enter 4-Byte Address Mode (B7H)

The Enter 4-Byte Address Mode instruction (***Figure 31-Figure 32***) will allow 32-bit address (A31-A0) to be used to access the memory array beyond 128Mb. The Enter 4-Byte Address Mode instruction is entered by driving /CS low, shifting the instruction code "B7h" into the SI pin and then driving /CS high.

Figure 31. Enter 4-Byte Address Mode instruction (SPI Mode)

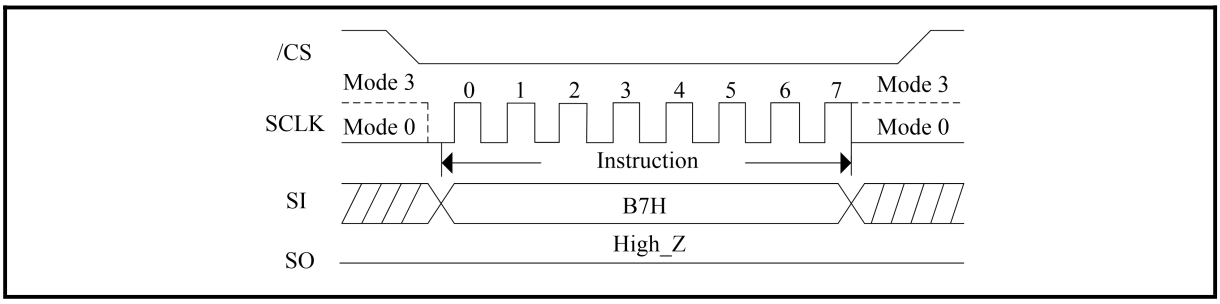
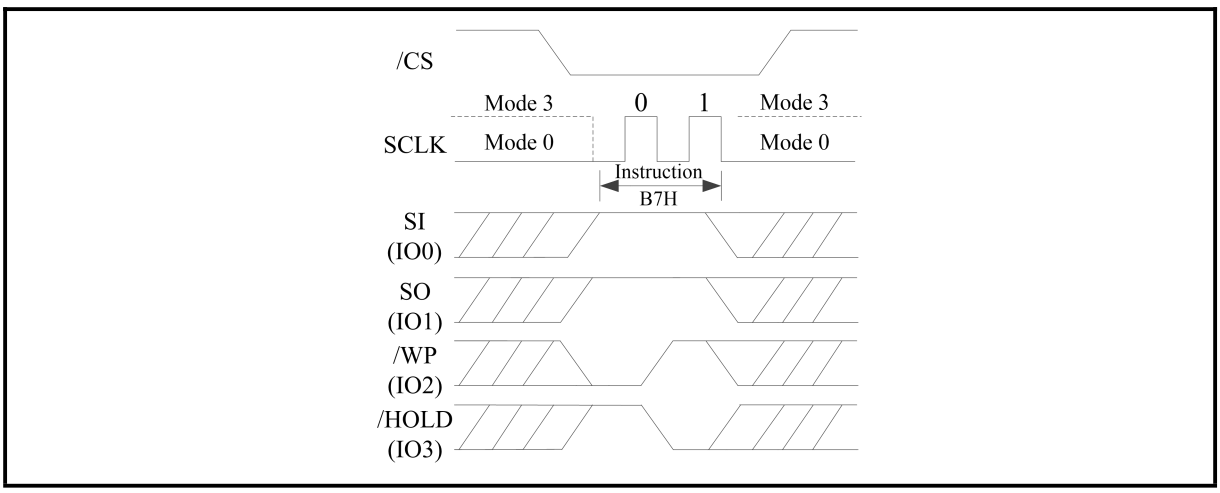


Figure 32. Enter 4-Byte Address Mode instruction (QPI Mode)



7.1.11 Exit 4-Byte Address Mode (E9H)

In order to be backward compatible, the Exit 4-Byte Address Mode instruction (***Figure 33-Figure 34***) will only allow 24-bit address (A23-A0) to be used to access the memory array up to 128Mb. The Extended Address Register must be used to access the memory array beyond 128Mb. The Exit 4-Byte Address Mode instruction is entered by driving /CS low, shifting the instruction code “E9h” into the SI pin and then driving /CS high.

Figure 33. Exit 4-Byte Address Mode (SPI Mode)

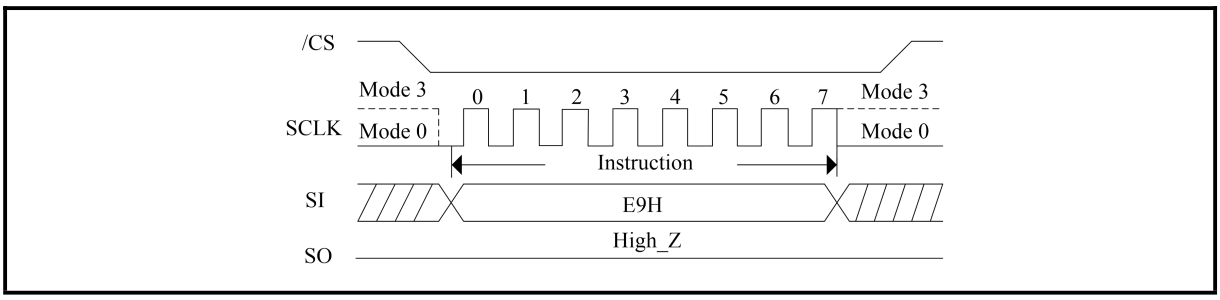
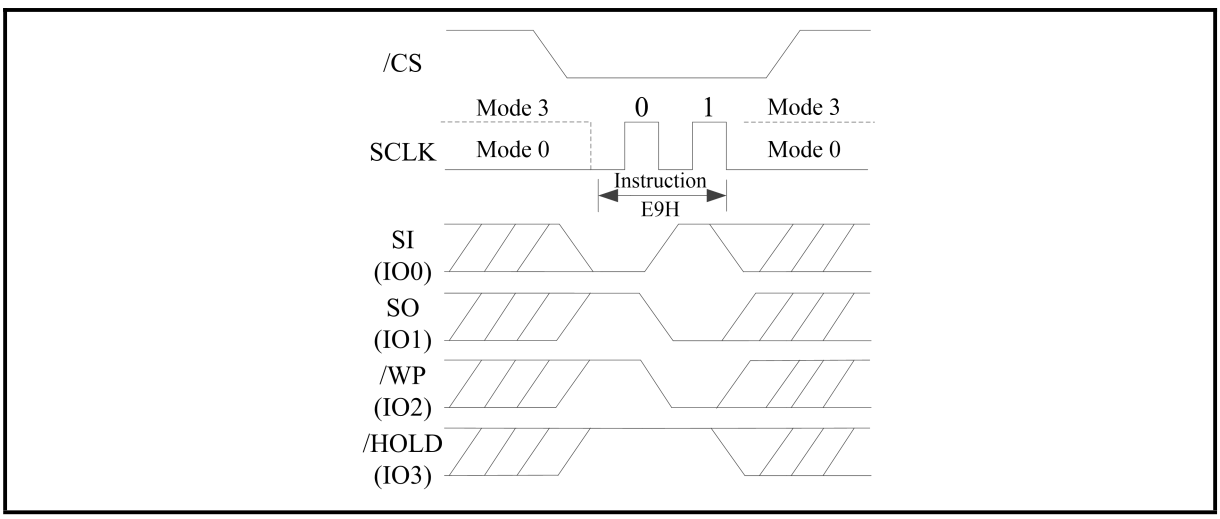


Figure 34. Exit 4-Byte Address Mode (QPI Mode)



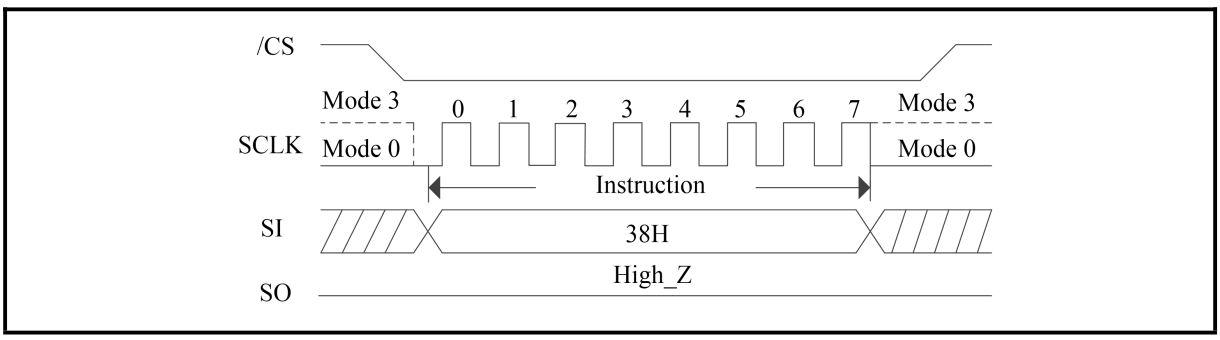
7.1.12 Enter QPI Mode (38H)

The BY25QM1GFS support both Standard/Dual/Quad Serial Peripheral Interface (SPI) and Quad Peripheral Interface (QPI). However, SPI mode and QPI mode cannot be used at the same time. “Enter QPI (38h)” instruction is the only way to switch the device from SPI mode to QPI mode.

Upon power-up, the default state of the device upon is Standard/Dual/Quad SPI mode. This provides full backward compatibility with earlier generations of BY Technology serial flash memories. See Instruction Set ***Table 19*** for all supported SPI instructions. In order to switch the device to QPI mode, the Quad Enable (QE) bit in Status Register-2 must be set to 1 first, and an “Enter QPI (38h)” instruction must be issued. If the Quad Enable (QE) bit is 0, the “Enter QPI (38h)” instruction will be ignored and the device will remain in SPI mode.

When the device is switched from SPI mode to QPI mode, the existing Write Enable and Program/Erase Suspend status, and the Wrap Length setting will remain unchanged.

Figure 35. Enter QPI Mode (SPI Mode)

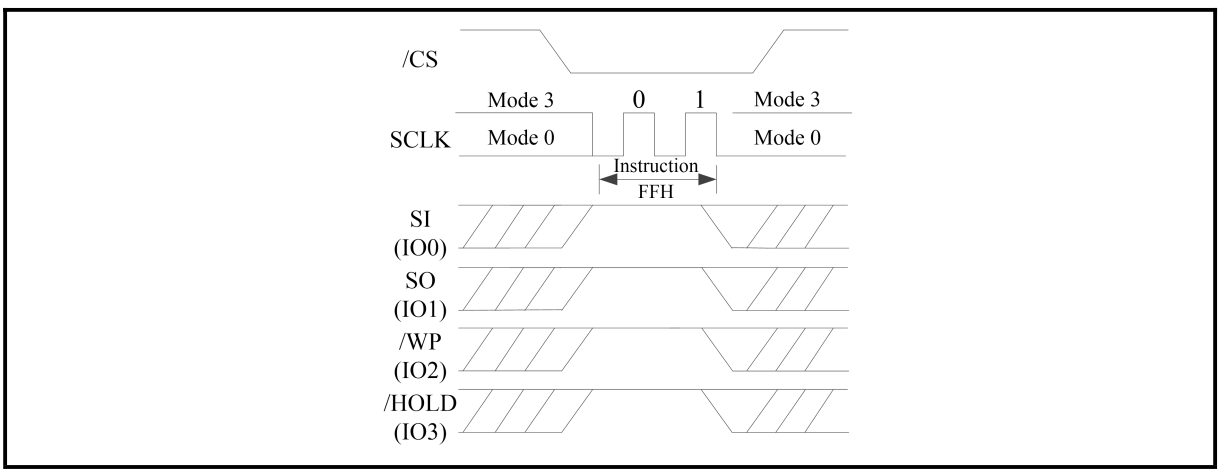


7.1.13 Exit QPI Mode (FFH)

In order to exit the QPI mode and return to the Standard/Dual/Quad SPI mode, an “Exit QPI (FFh)” instruction must be issued.

When the device is switched from QPI mode to SPI mode, the existing Write Enable Latch (WEL) and Program/Erase Suspend status, and the Wrap Length setting will remain unchanged.

Figure 36. Exit QPI Mode (QPI Mode)



7.1.14 Enable Reset (66H) and Reset Device (99H)

Because of the small package and the limitation on the number of pins, the BY25QM1GFS provides a software reset instruction instead of a dedicated RESET pin. Once the software reset instruction is accepted, any on-going internal operations will be terminated and the device will return to its default power-on state and lose all the current volatile settings, such as Volatile Status Register bits, Write Enable Latch (WEL) status, Program/Erase Suspend status, Continuous Read Mode bit setting (M7-M0) and Wrap Bit setting (W6-W4).

To avoid accidental reset, both “Enable Reset (66h)” and “Reset (99h)” instructions must be issued in sequence. Any other instructions other than “Reset (99h)” after the “Enable Reset (66h)” instruction will disable the “Reset Enable” state. A new sequence of “Enable Reset (66h)” and “Reset (99h)” is needed to reset the device. Once the Reset instruction is accepted by the device, the device will take approximately 300us to reset. During this period, no instruction will be accepted.

The Enable Reset (66h) and Reset (99h) instruction sequence is shown in ***Figure 37-Figure 38***.

Data corruption may happen if there is an on-going or suspended internal Erase or Program operation when Reset instruction sequence is accepted by the device. It is recommended to check the BUSY bit and the SUS bit in Status Register before issuing the Reset instruction sequence.

Figure 37. Enable Reset (66h) and Reset (99h) Instruction Sequence (SPI Mode)

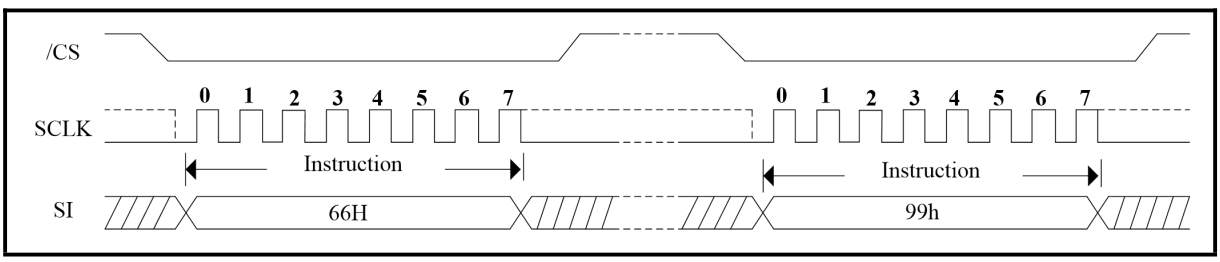
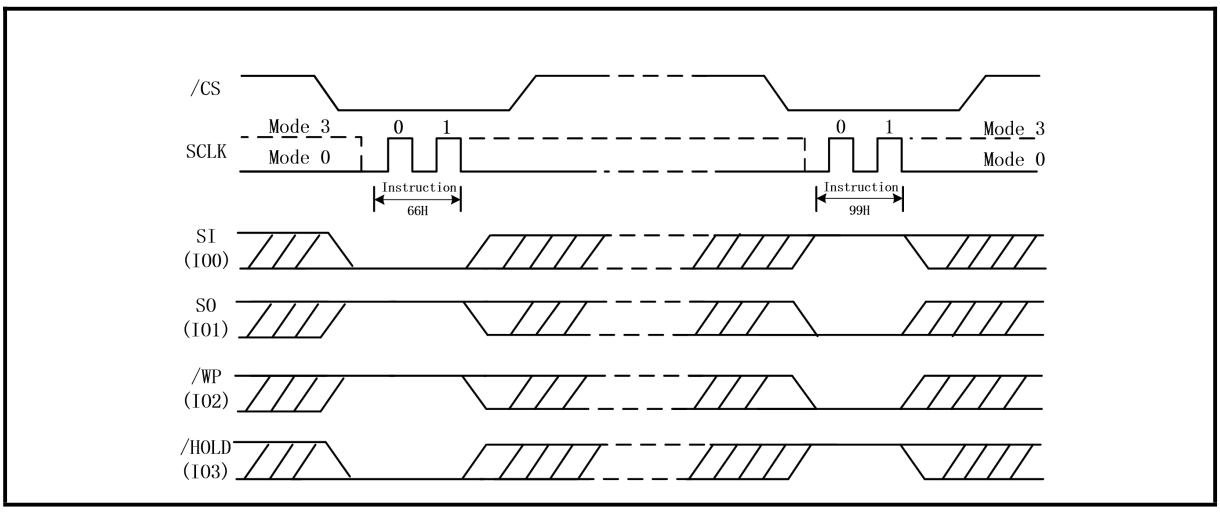


Figure 38. Enable Reset (66h) and Reset (99h) Instruction Sequence (QPI Mode)



7.2 Read Instructions

7.2.1 Read Data (03H)

See ***Figure 39-Figure 40***, the Read Data Bytes (READ) instruction is followed by a 3-byte/4-byte address (A23/31-A0), each bit being latched-in during the rising edge of SCLK. Then the memory content, at that address, is shifted out on SO, each bit being shifted out, at a Max frequency fR, during the falling edge of SCLK. The address is automatically incremented to the next higher address after each byte of data is shifted out allowing for a continuous stream of data. This means that the entire memory can be accessed with a single instruction as long as the clock continues. The instruction is completed by driving /CS high. The whole memory can be read with a single Read Data Bytes (READ) instruction. Any Read Data Bytes (READ) instruction, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

Figure 39. Read Data Bytes Sequence Diagram (SPI Mode/3-Byte Address Mode)

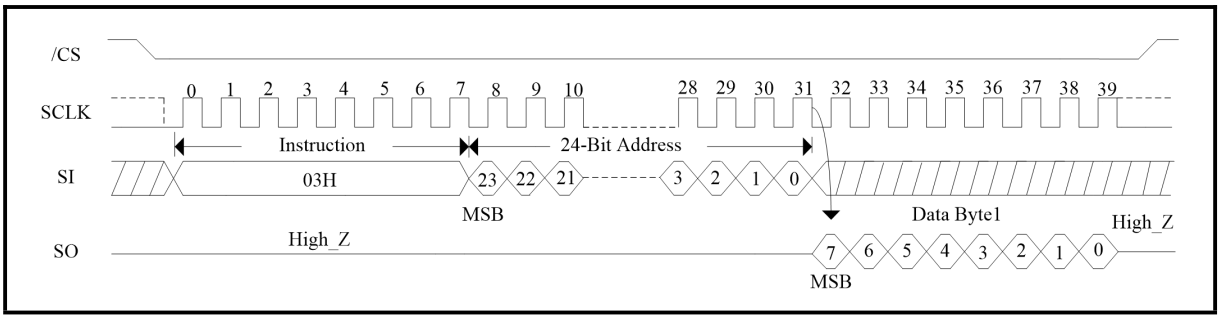
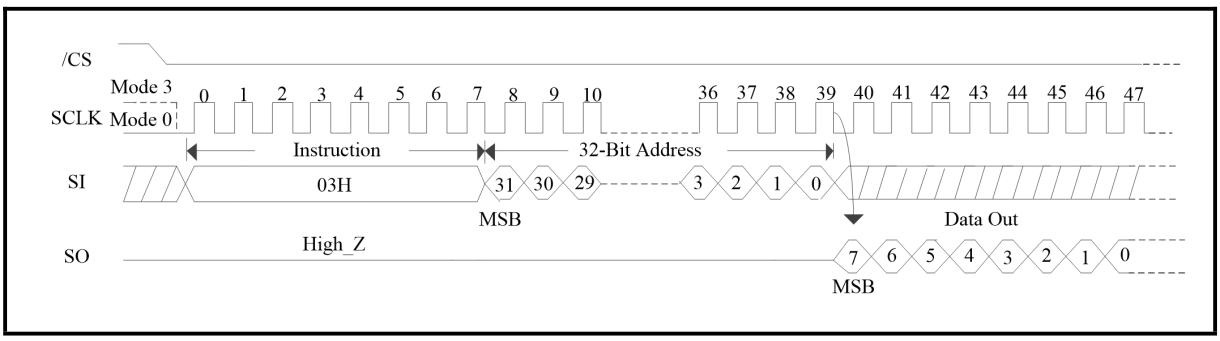


Figure 40. Read Data Bytes Sequence Diagram (SPI Mode/4-Byte Address Mode)



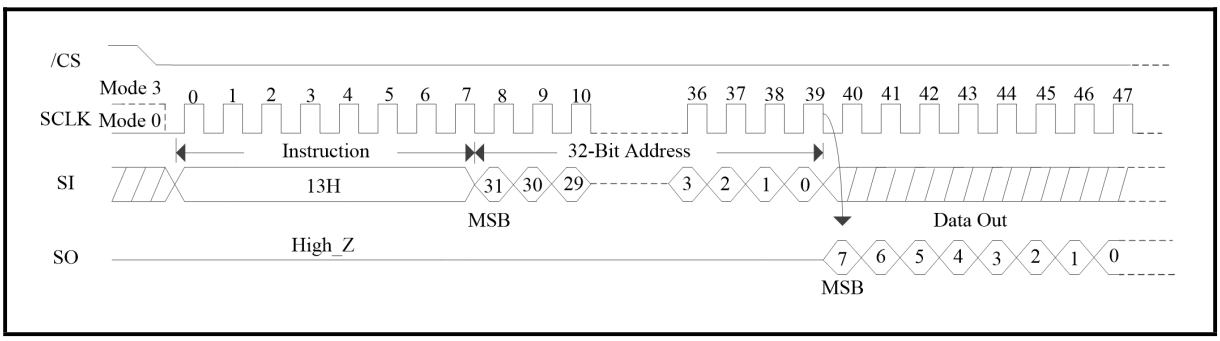
7.2.2 Read Data with 4-Byte Address (13H)

The Read Data with 4-Byte Address instruction is similar to the Read Data (03h) instruction. Instead of 24- bit address, 32-bit address is needed following the instruction code 13h. No matter the device is operating in 3-Byte Address Mode or 4-byte Address Mode, the Read Data with 4-Byte Address instruction will always require 32-bit address to access the entire 256Mb memory.

The Read Data with 4-Byte Address instruction sequence is shown in ***Figure 41***. If this instruction is issued while an Erase, Program or Write cycle is in process (WIP=1) the instruction is ignored and will not have any effects on the current cycle. The Read Data with 4-Byte Address instruction allows clock rates from D.C. to a maximum of fR (see AC Electrical Characteristics).

The Read Data with 4-Byte Address (13h) instruction is only supported in Standard SPI mode.

Figure 41. Read Data with 4-Byte Address Sequence Diagram (SPI Mode)



7.2.3 Fast Read (0BH)

See ***Figure 42-Figure 45***, the Read Data Bytes at Higher Speed (Fast Read) instruction is for quickly reading data out. It is followed by a 3-byte/4-byte address (A23/31-A0) and a dummy byte, each bit being latched-in during the rising edge of SCLK. Then the memory content, at that address, is shifted out on SO, each bit being shifted out, at a Max frequency fc, during the falling edge of SCLK. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out.

Figure 42. Fast Read Sequence Diagram (SPI Mode/3-Byte Address Mode)

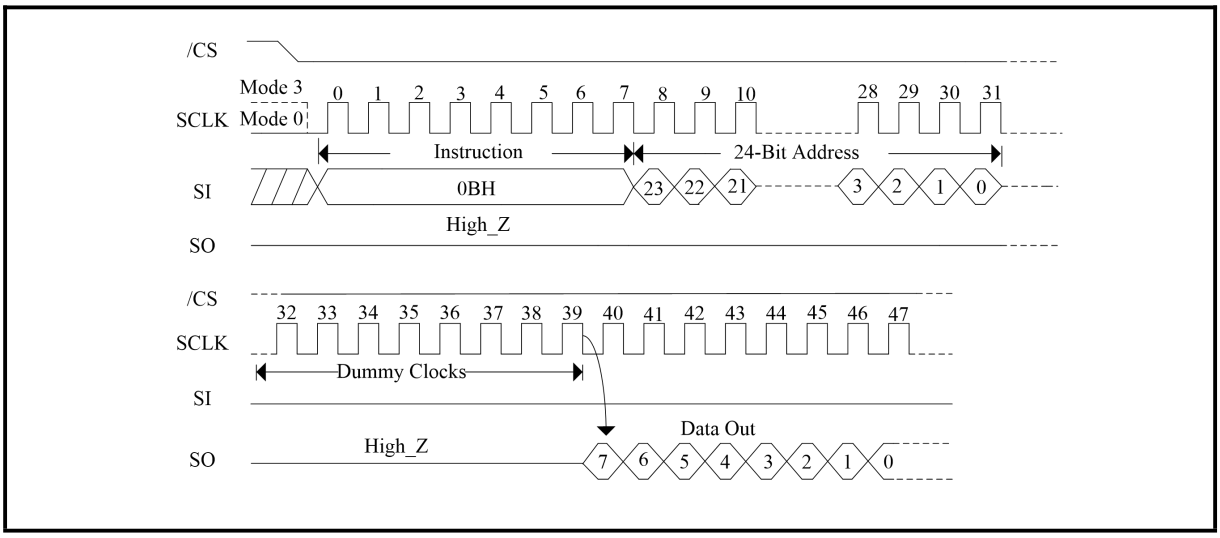
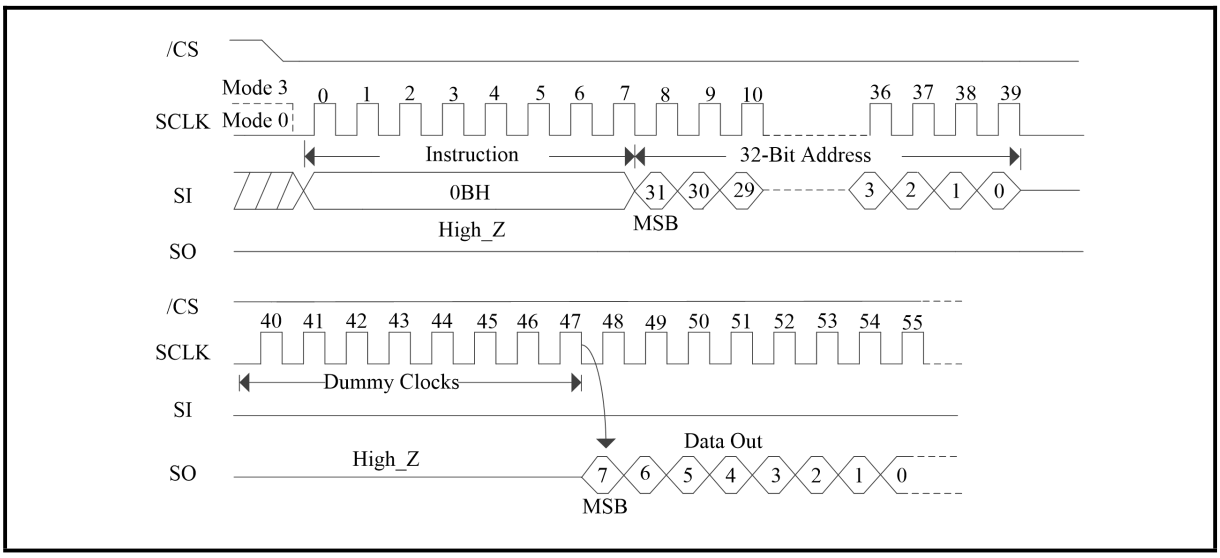


Figure 43. Fast Read Sequence Diagram (SPI Mode/4-Byte Address Mode)



Fast Read (0Bh) in QPI Mode

The Fast Read instruction is also supported in QPI mode. When QPI mode is enabled, the number of dummy clocks is configured by the “Set Read Parameters (C0h)” instruction to accommodate a wide range of applications with different needs for either maximum Fast Read frequency or minimum data access latency. Depending on the Read Parameter Bits P[5:4] setting, the number of dummy clocks can be configured as either 4, 4, 6 or 8. The default number of dummy clocks upon power up or after a Reset instruction is 4.

Figure 44. Fast Read Sequence Diagram (QPI Mode/3-Byte Address Mode)

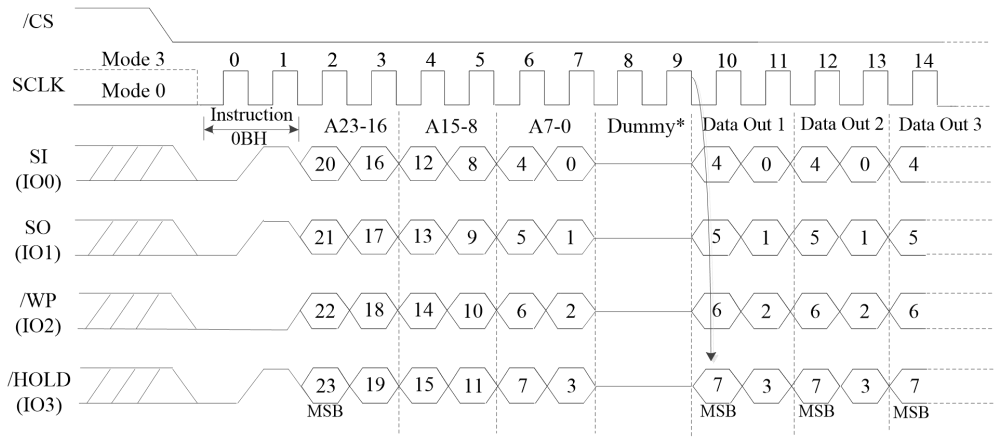
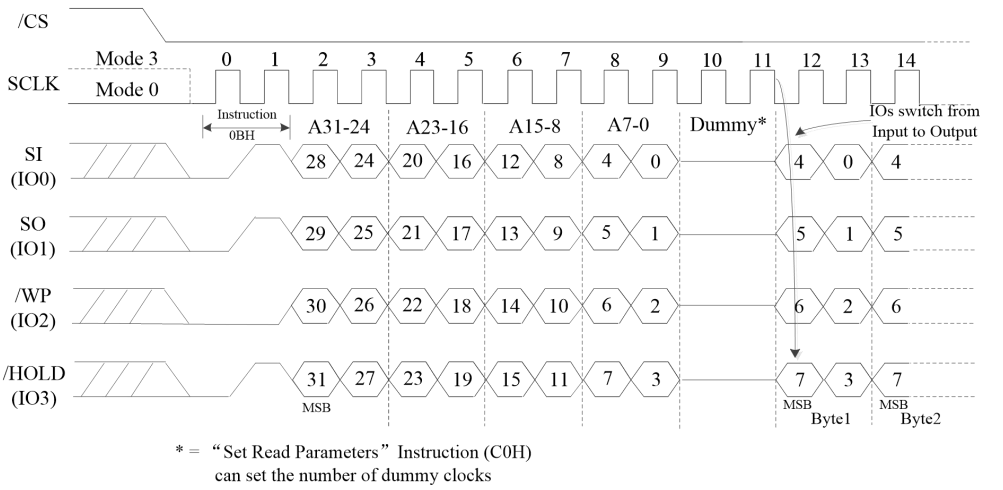


Figure 45. Fast Read Sequence Diagram (QPI Mode/4-Byte Address Mode)



7.2.4 DTR Fast Read (0DH)

The DTR Fast Read instruction is similar to the Fast Read instruction except that the 24/32-bit address input and the data output requires DTR (Double Transfer Rate) operation. This is accomplished by adding six “dummy” clocks after the 24/32-bit address as shown in ***Figure 46-Figure 47***. The dummy clocks allow the devices internal circuits additional time for setting up the initial address. During the dummy clocks the data value on the SO pin is a “don’t care”.

Figure 46. DTR Fast Read (SPI Mode/3-Byte Address Mode)

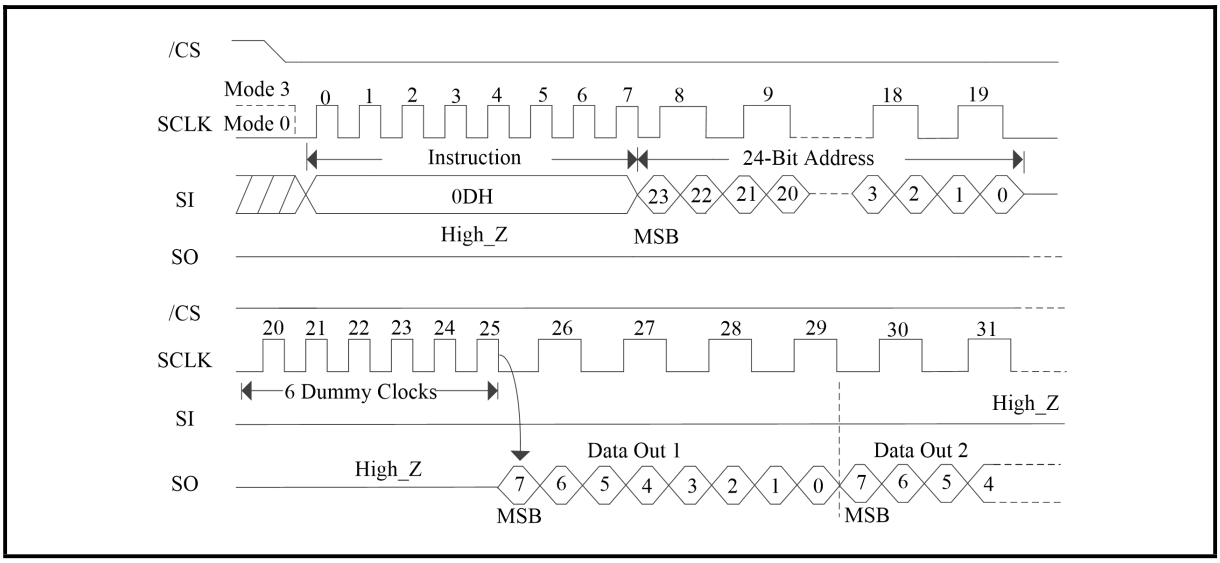
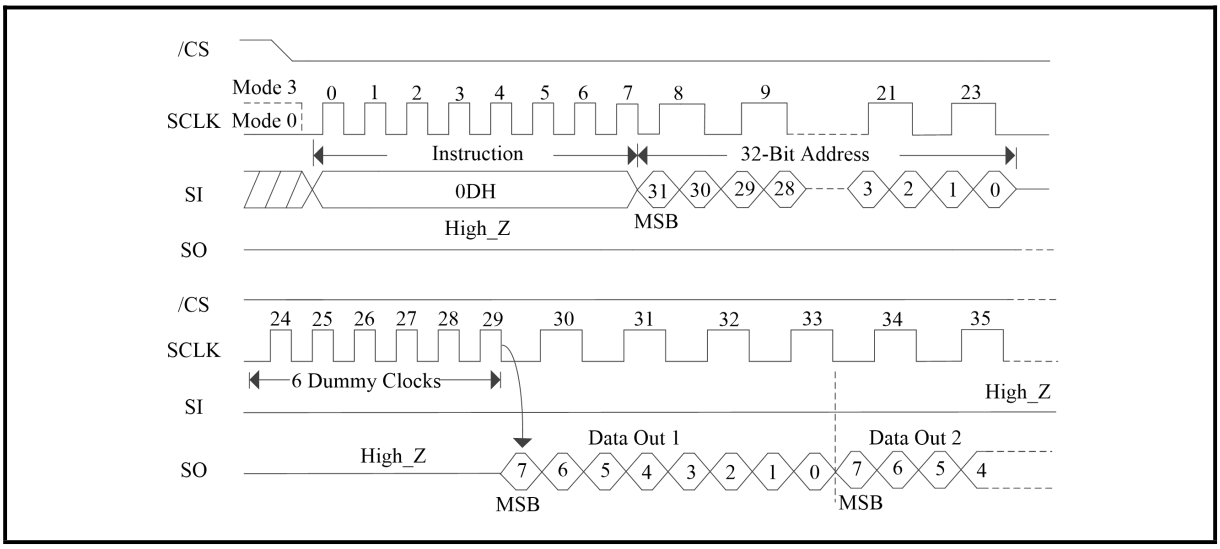


Figure 47. DTR Fast Read (SPI Mode/4-Byte Address Mode)



DTR Fast Read (0Dh) in QPI Mode

The DTR Fast Read instruction is also supported in QPI mode.

Figure 48. DTR Fast Read (QPI Mode/3-Byte Address Mode)

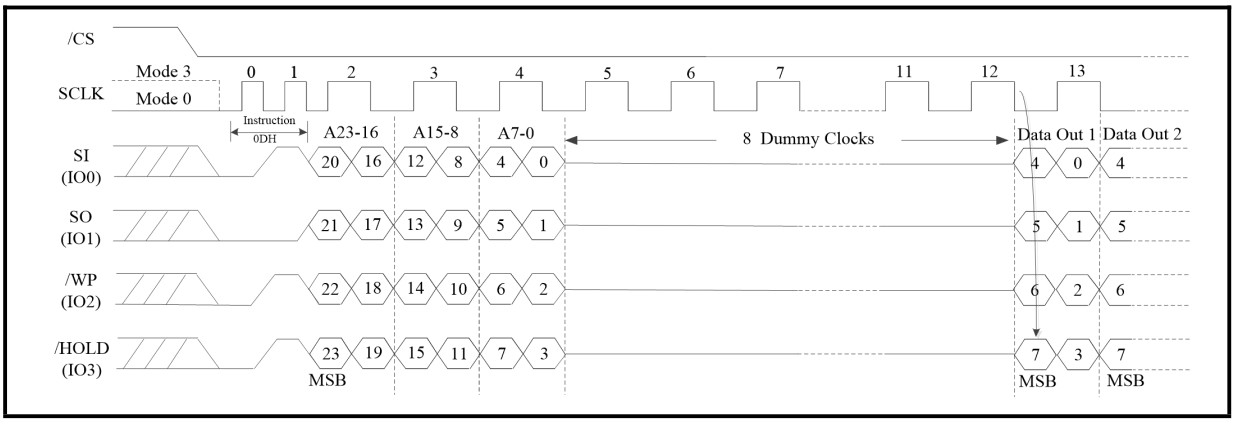
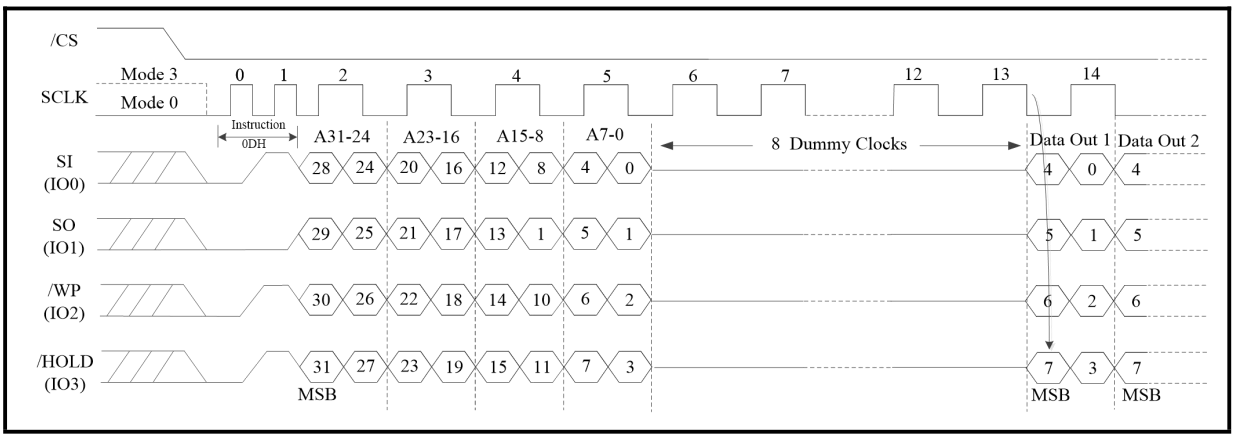


Figure 49. DTR Fast Read (QPI Mode/4-Byte Address Mode)

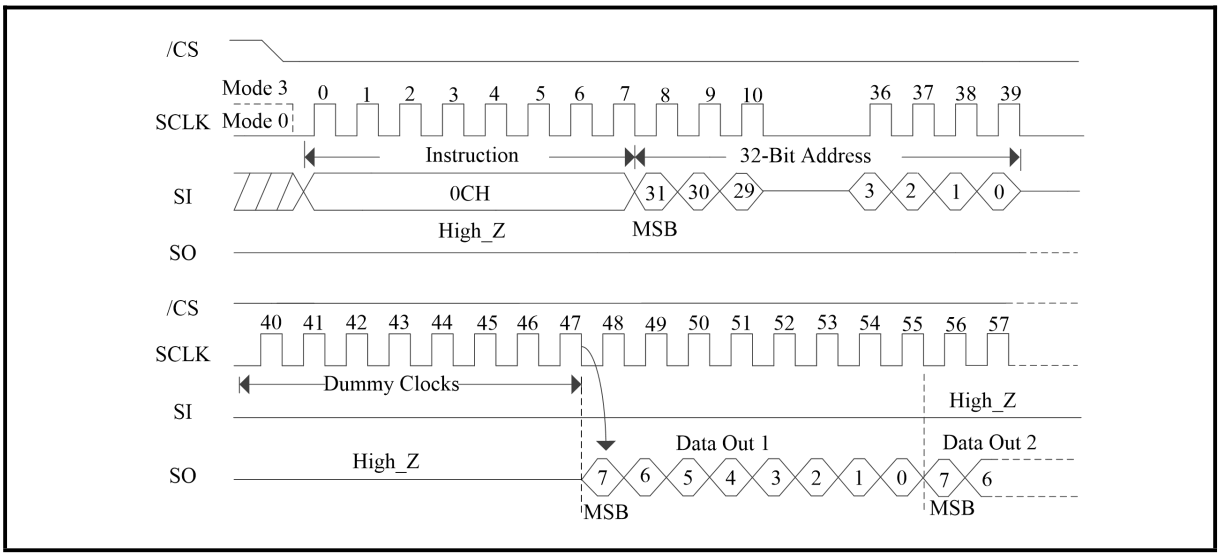


7.2.5 Fast Read with 4-Byte Address (0CH)

The Fast Read with 4-Byte Address (0Ch) instruction is similar to the Fast Read instruction except that it requires 32-bit address instead of 24-bit address. No matter the device is operating in 3-Byte Address Mode or 4-byte Address Mode, the Read Data with 4-Byte Address instruction will always require 32-bit address to access the entire 256Mb memory.

The Fast Read with 4-Byte Address instruction is only supported in Standard SPI mode. In QPI mode, the instruction code 0Ch is used for the “Burst Read with Wrap” instruction.

Figure 50. Fast Read with 4-Byte Address



7.2.6 Dual Output Fast Read (3BH)

See ***Figure 51-Figure 52***, the Dual Output Fast Read instruction is followed by 3/4-byte address (A23/31-A0) and a dummy byte, each bit being latched in during the rising edge of SCLK, then the memory contents are shifted out 2-bit per clock cycle from SI and SO. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out.

Figure 51. Dual Output Fast Read Sequence Diagram (SPI Mode/3-Byte Address Mode)

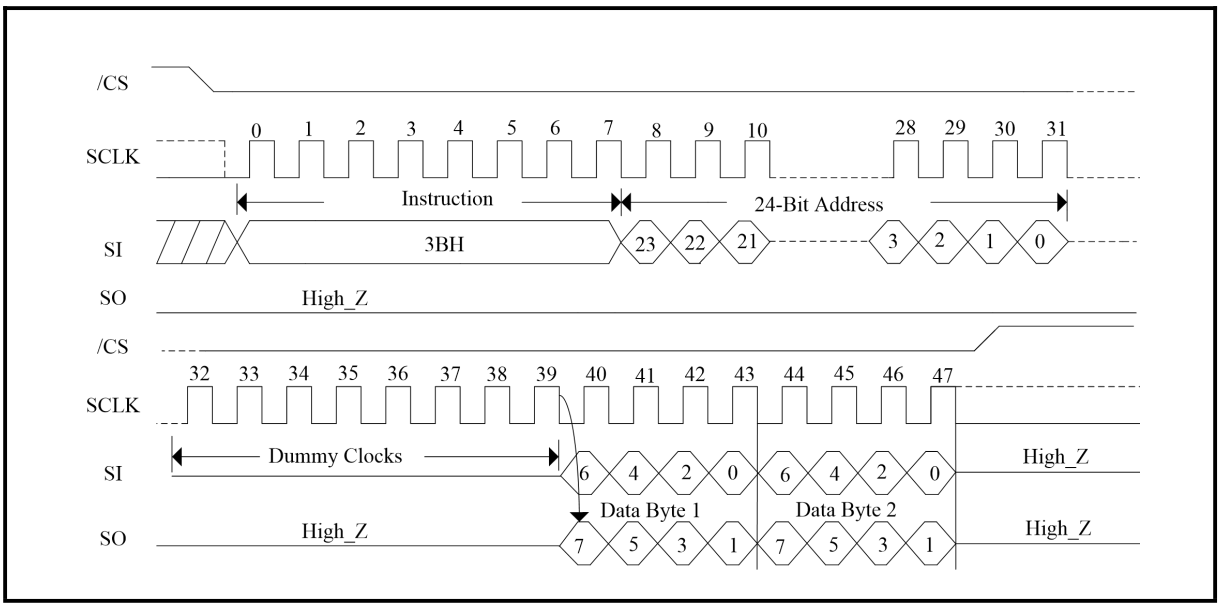
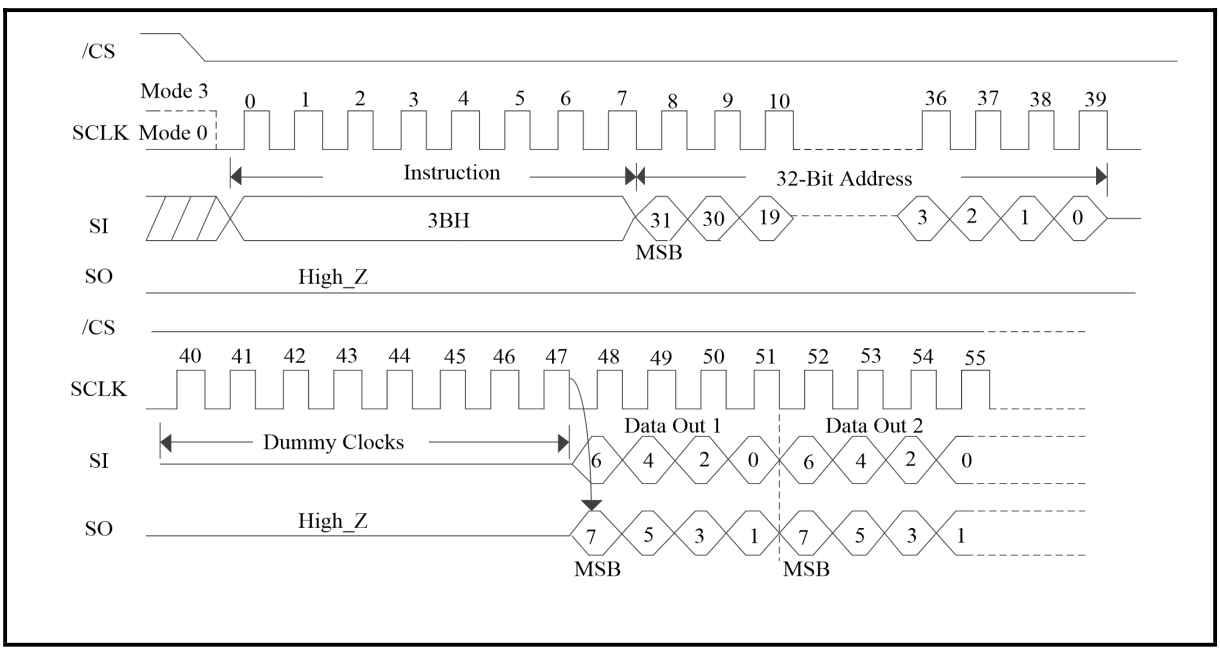


Figure 52. Dual Output Fast Read Sequence Diagram (SPI Mode/4-Byte Address Mode)

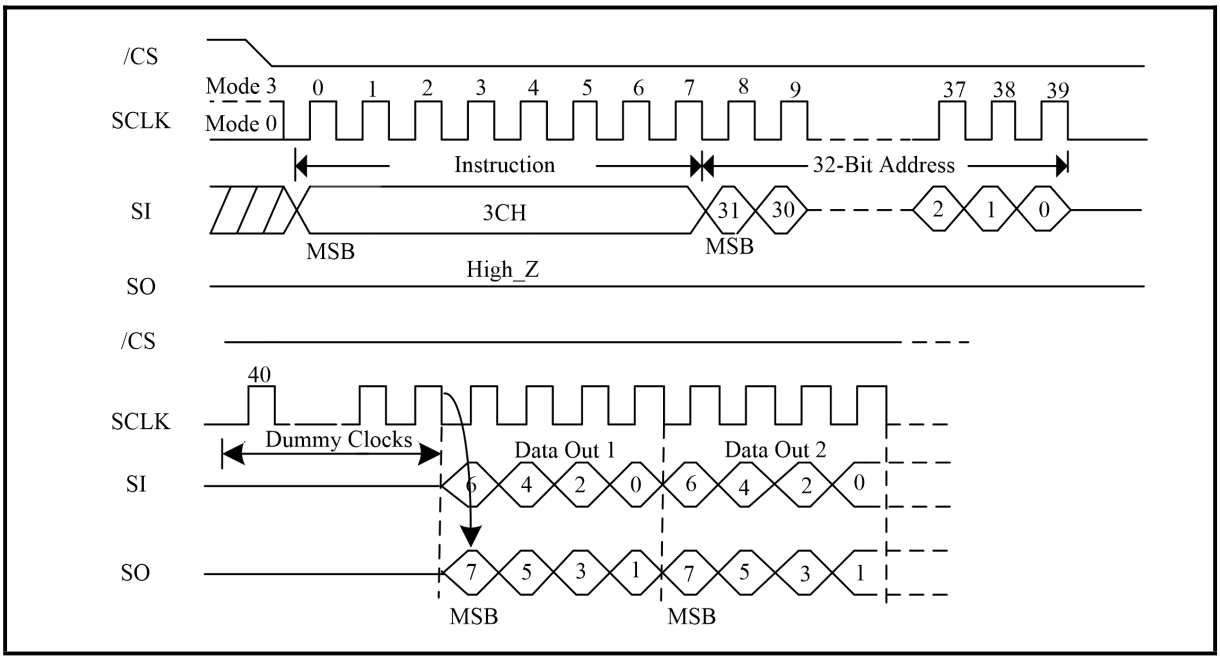


7.2.7 Fast Read Dual Output with 4-Byte Address (3CH)

The Fast Read Dual Output with 4-Byte Address instruction is similar to the Fast Read Dual Output instruction except that it requires 32-bit address instead of 24-bit address. No matter the device is operating in 3-Byte Address Mode or 4-byte Address Mode, the Fast Read Dual Output with 4-Byte Address instruction will always require 32-bit address to access the entire 256Mb memory.

The Fast Read Dual Output with 4-Byte Address (3Ch) instruction is only supported in Standard SPI mode.

Figure 53. Fast Read Dual Output with 4-Byte Address



7.2.8 Quad Output Fast Read (6BH)

See ***Figure 54-Figure 55***, the Quad Output Fast Read instruction is followed by 3/4-byte address (A23/31-A0) and a dummy byte, each bit being latched in during the rising edge of SCLK, then the memory contents are shifted out 4-bit per clock cycle from IO3, IO2, IO1 and IO0. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The Quad Enable bit (QE) of Status Register must be set to enable.

Figure 54. Quad Output Fast Read Sequence Diagram (SPI Mode/3-Byte Address Mode)

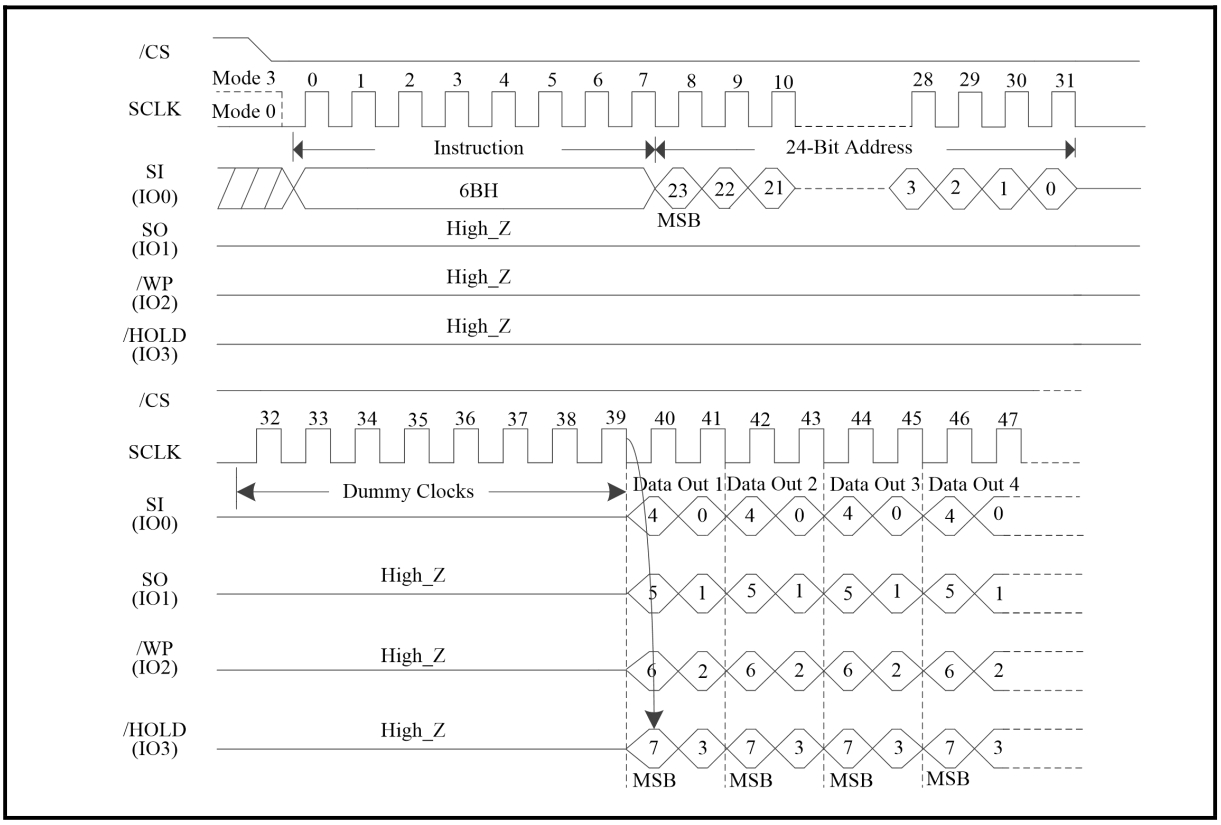
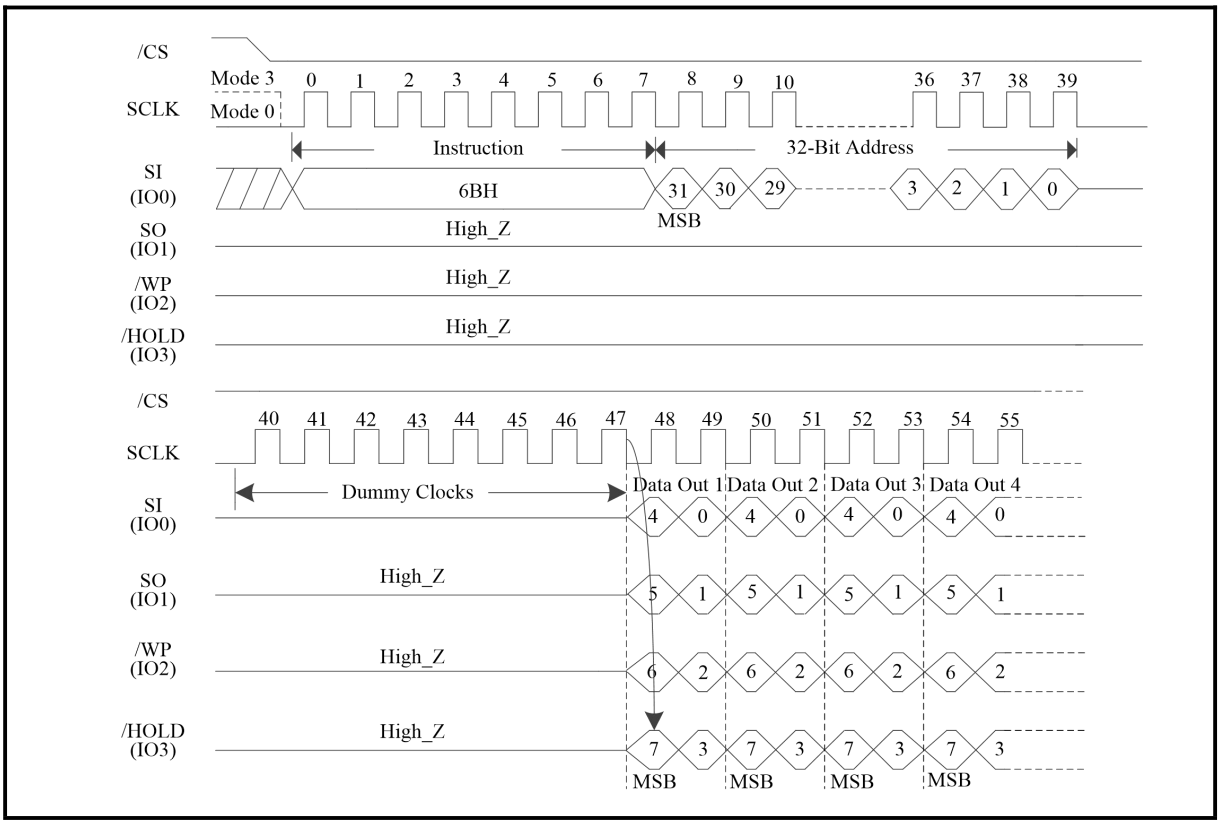


Figure 55. Quad Output Fast Read Sequence Diagram (SPI Mode/4-Byte Address Mode)

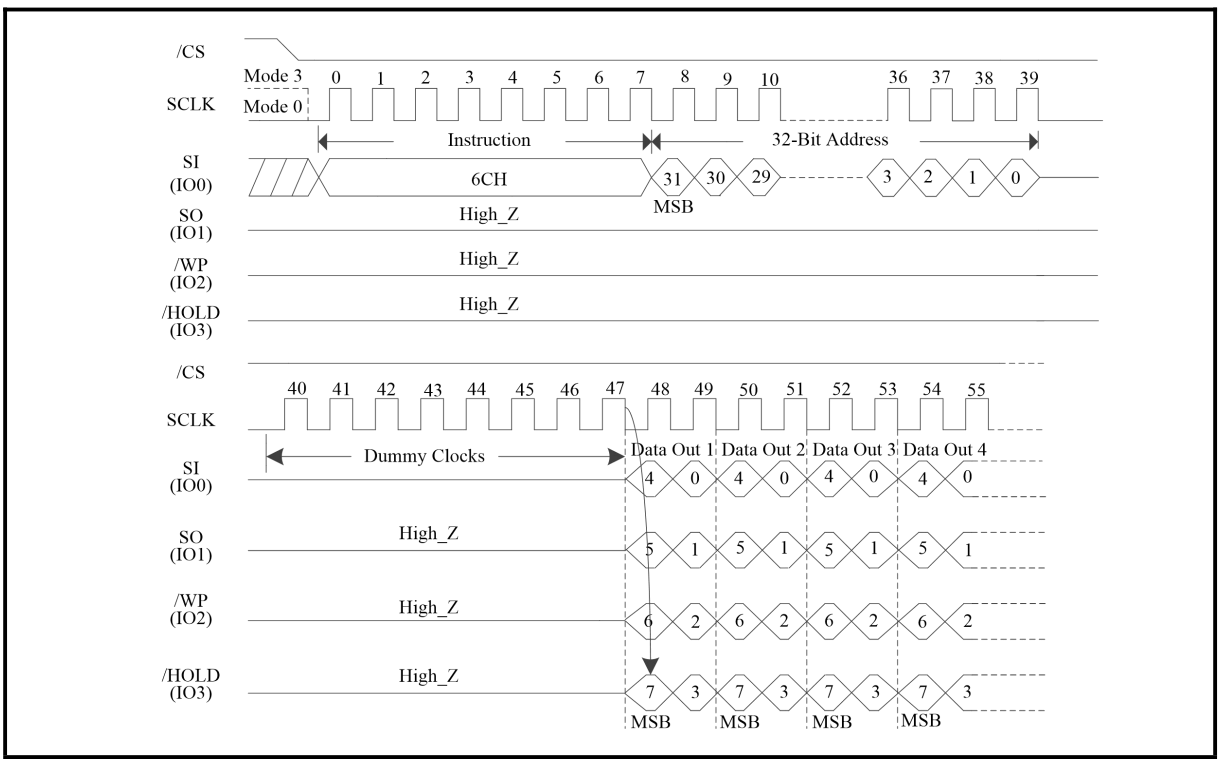


7.2.9 Fast Read Quad Output with 4-Byte Address (6CH)

The Fast Read Quad Output with 4-Byte Address instruction is similar to the Fast Read Quad Output instruction except that it requires 32-bit address instead of 24-bit address. No matter the device is operating in 3-Byte Address Mode or 4-byte Address Mode, the Fast Read Quad Output with 4-Byte Address instruction will always require 32-bit address to access the entire 256Mb memory. The Quad Enable bit (QE) of Status Register must be set to enable.

The Fast Read Quad Output with 4-Byte Address (6Ch) instruction is only supported in Standard SPI mode.

Figure 56. Fast Read Quad Output with 4-Byte Address



7.2.10 Dual I/O Fast Read (BBH)

See ***Figure 57-Figure 60***, the Dual I/O Fast Read instruction is similar to the Dual Output Fast Read instruction but with the capability to input the 3/4-byte address (A23/31-0) and a “Continuous Read Mode” byte 2-bit per clock by SI and SO, each bit being latched in during the rising edge of SCLK, then the memory contents are shifted out 2-bit per clock cycle from SI and SO. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out.

Dual I/O Fast Read with “continuous Read Mode”

The Dual I/O Fast Read instruction can further reduce instruction overhead through setting the “continuous Read Mode” bits (M7-4) after the inputs 3-byte address A23-A0).If the “continuous Read Mode” bits(M5-4)=(1,0),then the next Dual I/O fast Read instruction (after CS/ is raised and then lowered) does not require the BBH instruction code. The instruction sequence is shown in the following ***Figure 57-Figure 60***.If the “continuous Read Mode” bits (M5-4) does not equal (1,0), the next instruction requires the first BBH instruction code, thus returning to normal operation. A “continuous Read Mode” Reset instruction can be used to reset (M5-4) before issuing normal instruction.

Figure 57. Dual I/O Fast Read Sequence Diagram (SPI Mode/3-Byte Address Mode; Initial instruction or previous (M5-4)≠(1,0))

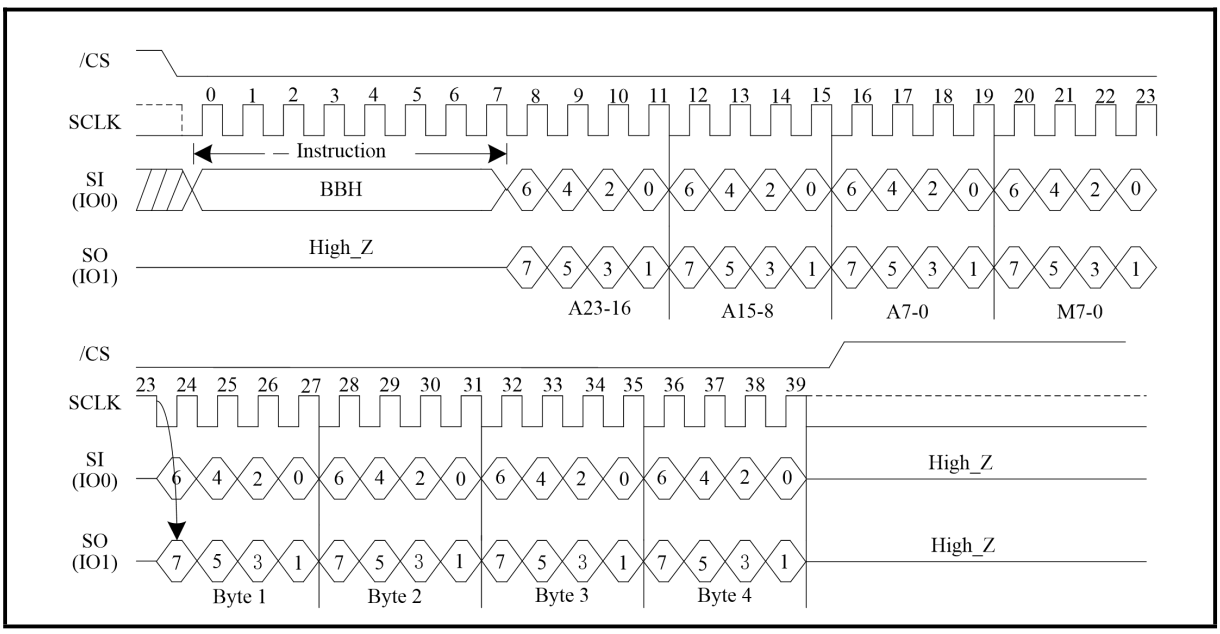


Figure 58. Dual I/O Fast Read Sequence Diagram (SPI Mode/4-Byte Address Mode; Initial instruction or previous (M5-4)≠(1,0))

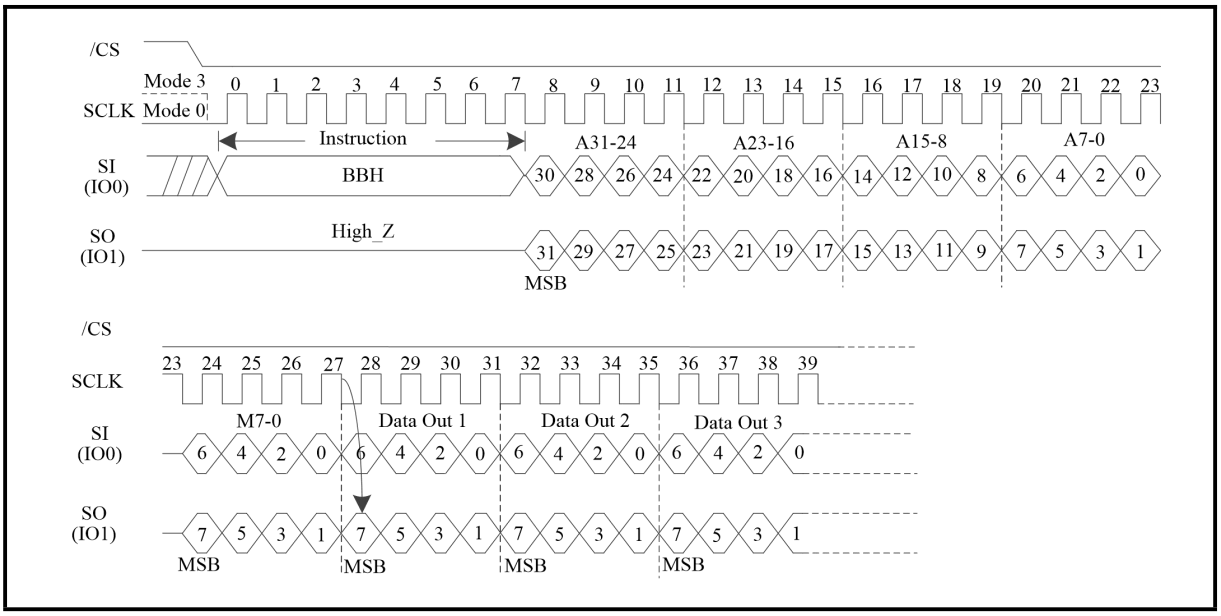


Figure 59. Dual I/O Fast Read Sequence Diagram (SPI Mode/3-Byte Address Mode; Previous instruction set (M5-4) =(1,0))

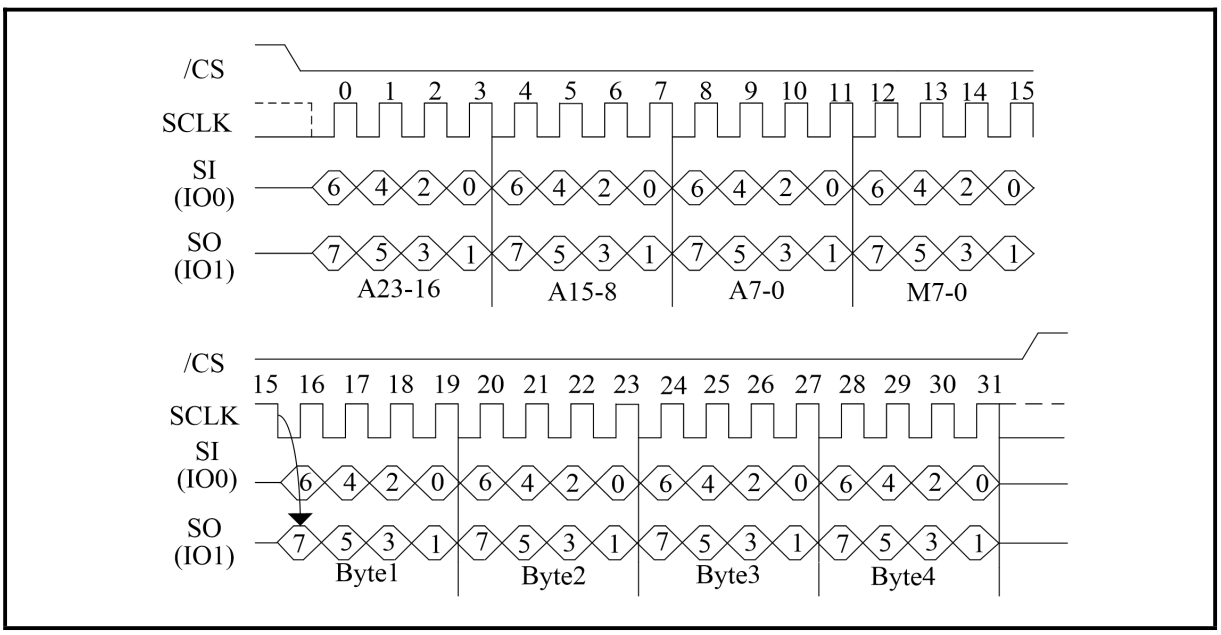
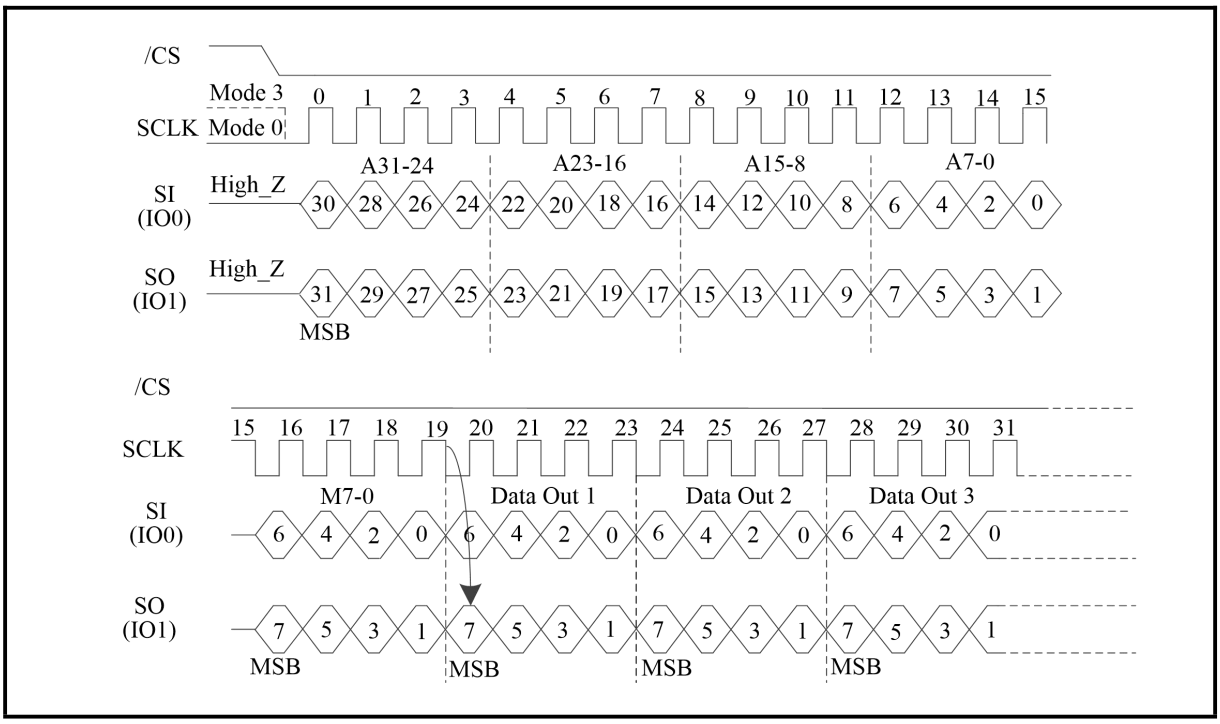


Figure 60. Dual I/O Fast Read Sequence Diagram (SPI Mode/4-Byte Address Mode; Previous instruction set (M5-4) =(1,0))



7.2.11 DTR Fast Read Dual I/O (BDH)

The DTR Fast Read Dual I/O (BDh) instruction allows for improved random access while maintaining two IO pins, IO0 and IO1. It is similar to the Fast Read Dual Output (3Bh) instruction but with the capability to input the Address bits (A23/A31-0) two bits per clock.

DTR Fast Read Dual I/O with "Continuous Read Mode"

The DTR Fast Read Dual I/O instruction can further reduce instruction overhead through setting the "Continuous Read Mode" bits (M7-0) after the input Address bits (A23/31-0), as shown in ***Figure 61-Figure 64***. The upper nibble of the (M7-4) controls the length of the next Fast Read Dual I/O instruction through the inclusion or exclusion of the first byte instruction code. The lower nibble bits of the (M3-0) are don't care ("x"). However, the IO pins should be high-impedance prior to the falling edge of the first data out clock.

If the "Continuous Read Mode" bits M5-4 = (1,0), then the next Fast Read Dual I/O instruction (after /CS is raised and then lowered) does not require the BDh instruction code, as shown in ***Figure 63-Figure 64***. This reduces the instruction sequence by eight clocks and allows the Read address to be immediately entered after /CS is asserted low. If the "Continuous Read Mode" bits M5-4 do not equal to (1,0), the next instruction (after /CS is raised and then lowered) requires the first byte instruction code, thus returning to normal operation.

Figure 61. DTR Fast Read Dual I/O (SPI Mode only/3-Byte Address Mode; Initial instruction or previous M5-4≠10)

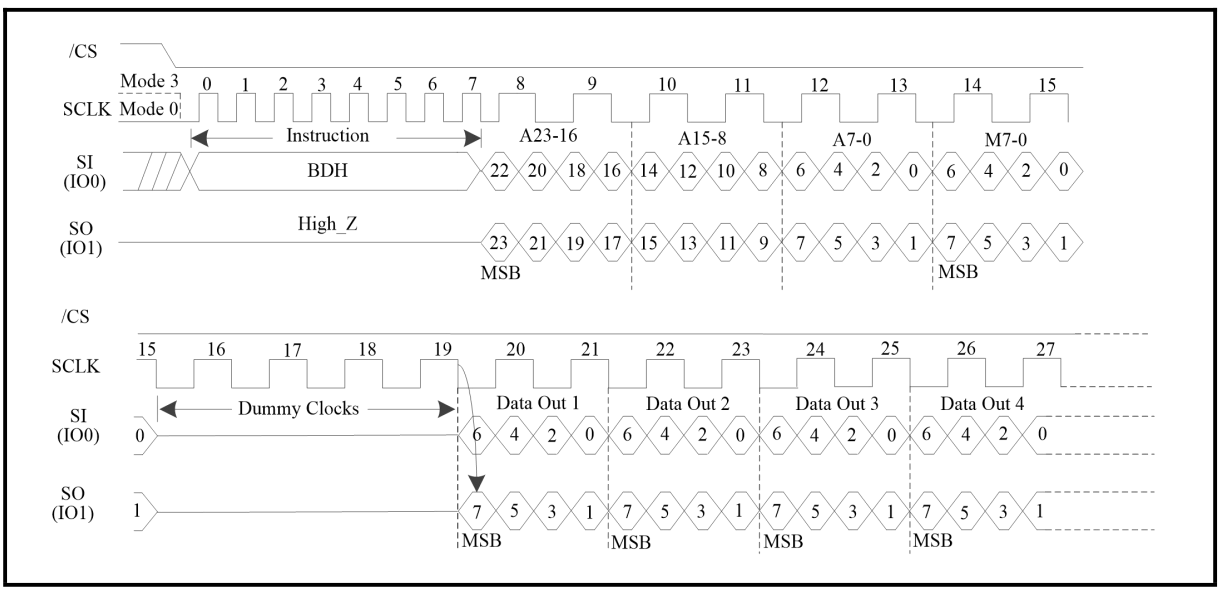


Figure 62. DTR Fast Read Dual I/O (SPI Mode only/4-Byte Address Mode; Initial instruction or previous M5-4≠10)

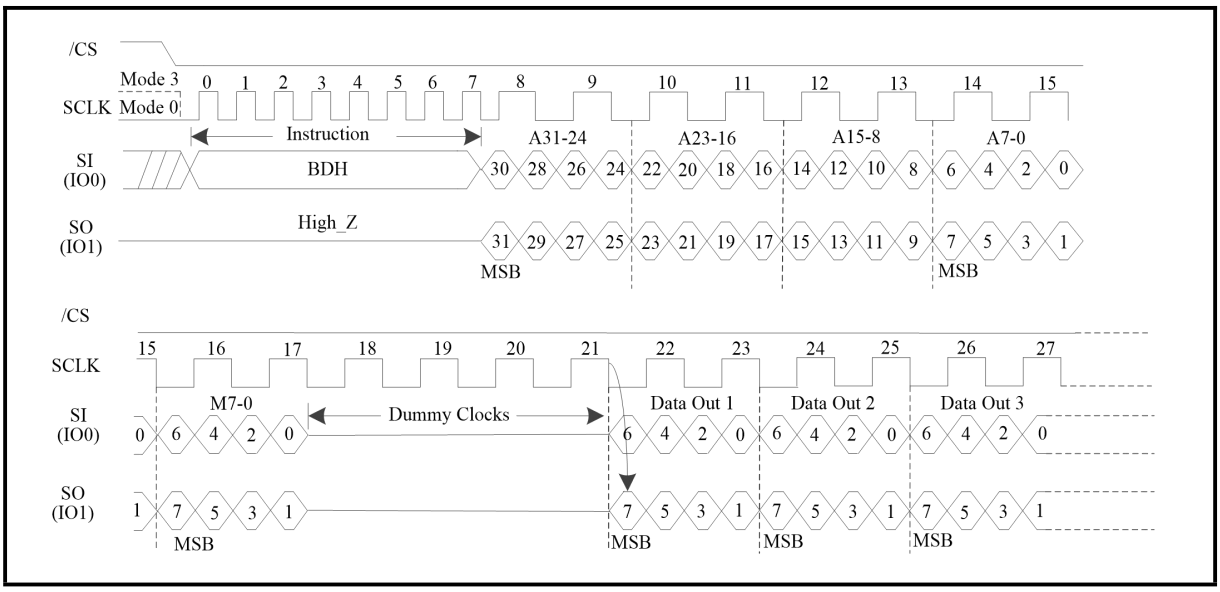


Figure 63. DTR Fast Read Dual I/O (SPI Mode only/3-Byte Address Mode; Previous instruction set M5-4=10)

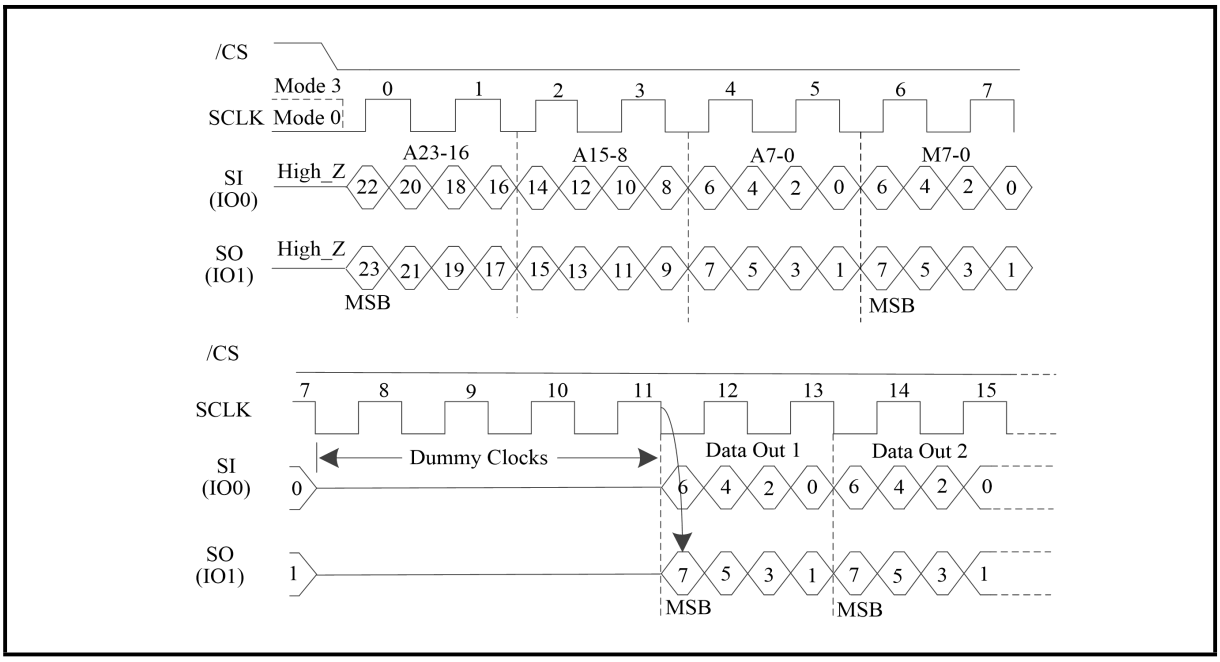
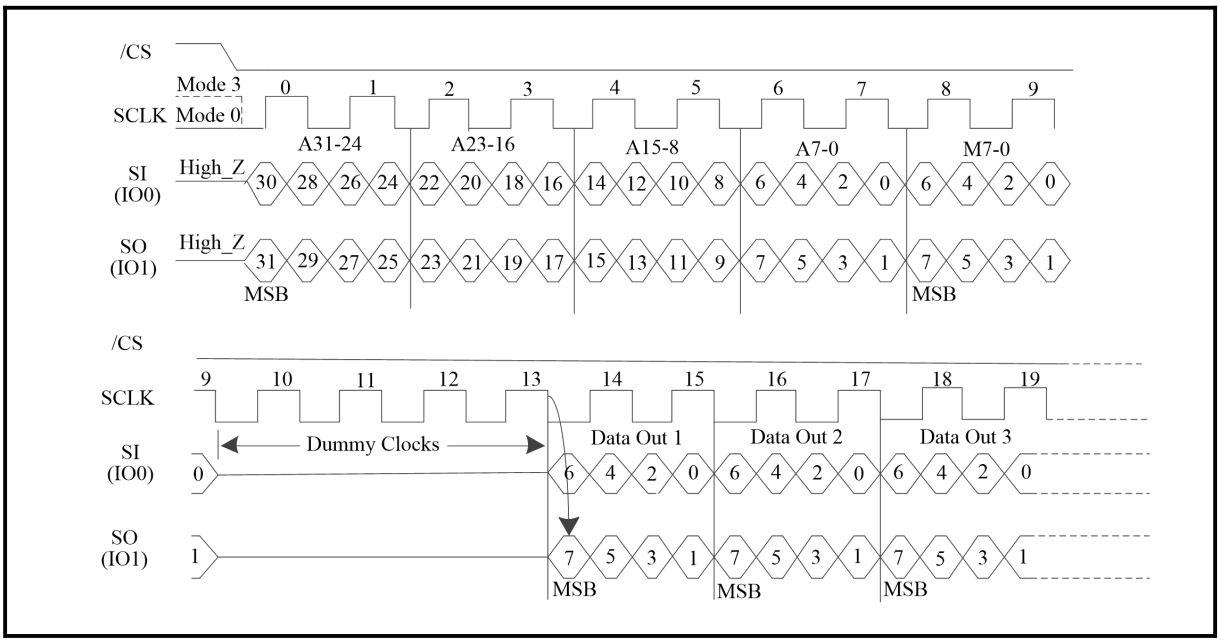


Figure 64. DTR Fast Read Dual I/O (SPI Mode only/4-Byte Address Mode; Previous instruction set M5-4=10)



7.2.12 Fast Read Dual I/O with 4-Byte Address (BCH)

The Fast Read Dual I/O with 4-Byte Address instruction is similar to the Fast Read Dual I/O instruction except that it requires 32-bit address instead of 24-bit address. No matter the device is operating in 3-Byte Address Mode or 4-byte Address Mode, the Fast Read Dual I/O with 4-Byte Address instruction will always require 32-bit address to access the entire 256Mb memory.

The Fast Read Dual I/O with 4-Byte Address (BCh) instruction is only supported in Standard SPI mode.

Figure 65. Fast Read Dual I/O with 4-Byte Address(SPI Mode only; Initial instruction or previous M5-4≠10)

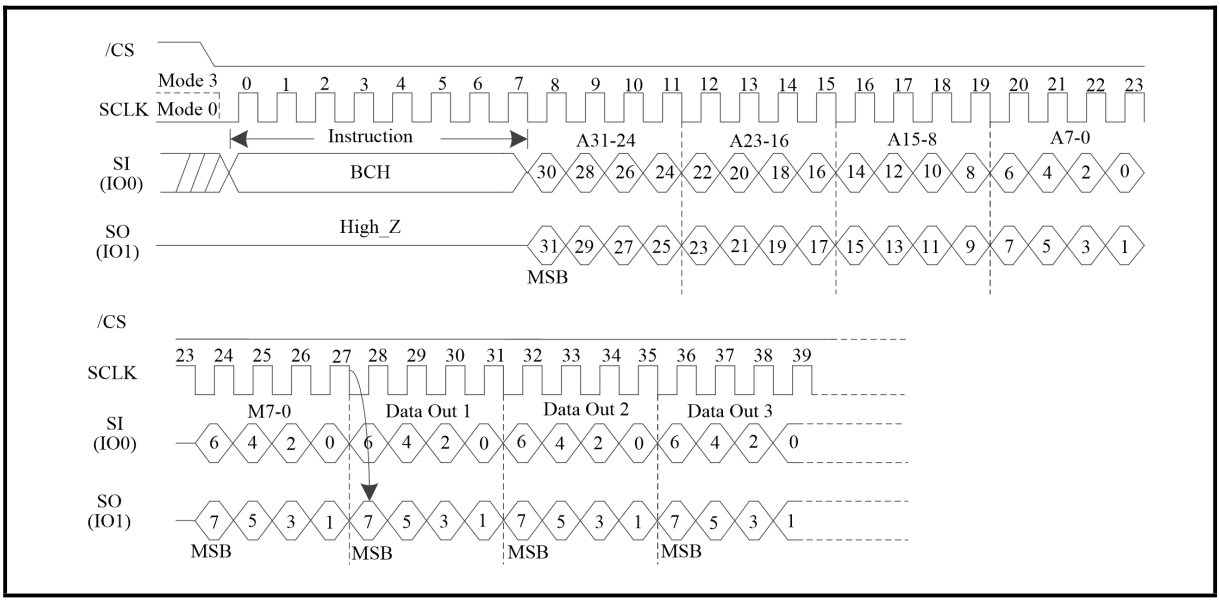
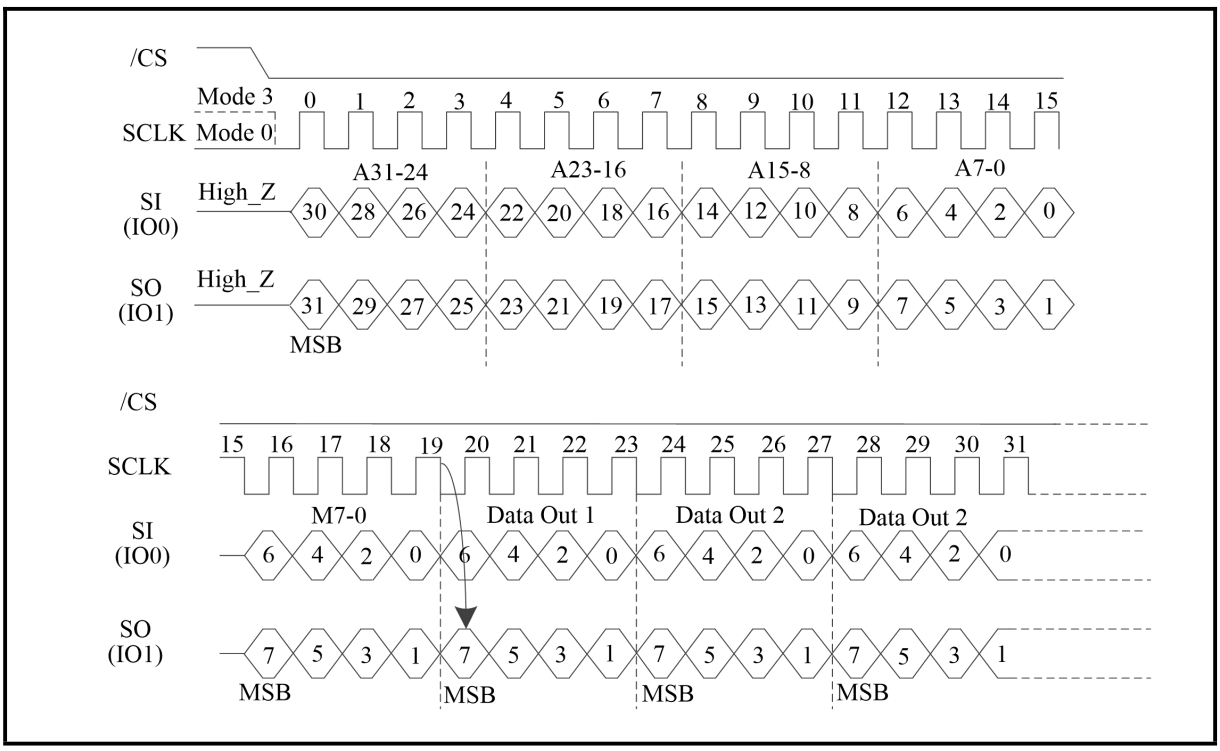


Figure 66. Fast Read Dual I/O with 4-Byte Address(SPI Mode only; Initial instruction or previous M5-4=10)



7.2.13 Quad I/O Fast Read (EBH)

See ***Figure 67-Figure 70***, the Quad I/O Fast Read instruction is similar to the Dual I/O Fast Read instruction but with the capability to input the 3/4-byte address (A23/31-0) and a "Continuous Read Mode" byte and 4-dummy clock 4-bit per clock by IO0, IO1, IO3, IO4, each bit being latched in during the rising edge of SCLK, then the memory contents are shifted out 4-bit per clock cycle from IO0, IO1, IO2, IO3. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The Quad Enable bit (QE) of Status Register must be set to enable for the Quad I/O Fast read instruction, as shown in ***Figure 67-Figure 74.***

Quad I/O Fast Read with "Continuous Read Mode"

The Quad I/O Fast Read instruction can further reduce instruction overhead through setting the "Continuous Read Mode" bits (M7-0) after the input Address bits (A23-0), If the "Continuous Read Mode" bits (M5-4)= (1,0), then the next Fast Read Quad I/O instruction(after /CS is raised and then lowered) does not require the EBH instruction code. If the "Continuous Read Mode" bits M5-4 do not equal to (1,0), the next instruction requires the first EBH instruction code, thus returning to normal operation. A "Continuous Read Mode" Reset instruction can also be used to reset (M5-4) before issuing normal instruction.

Figure 67. Quad I/O Fast Read Sequence Diagram (SPI Mode/3-Byte Address Mode; Initial instruction or previous (M5-4≠(1,0)))

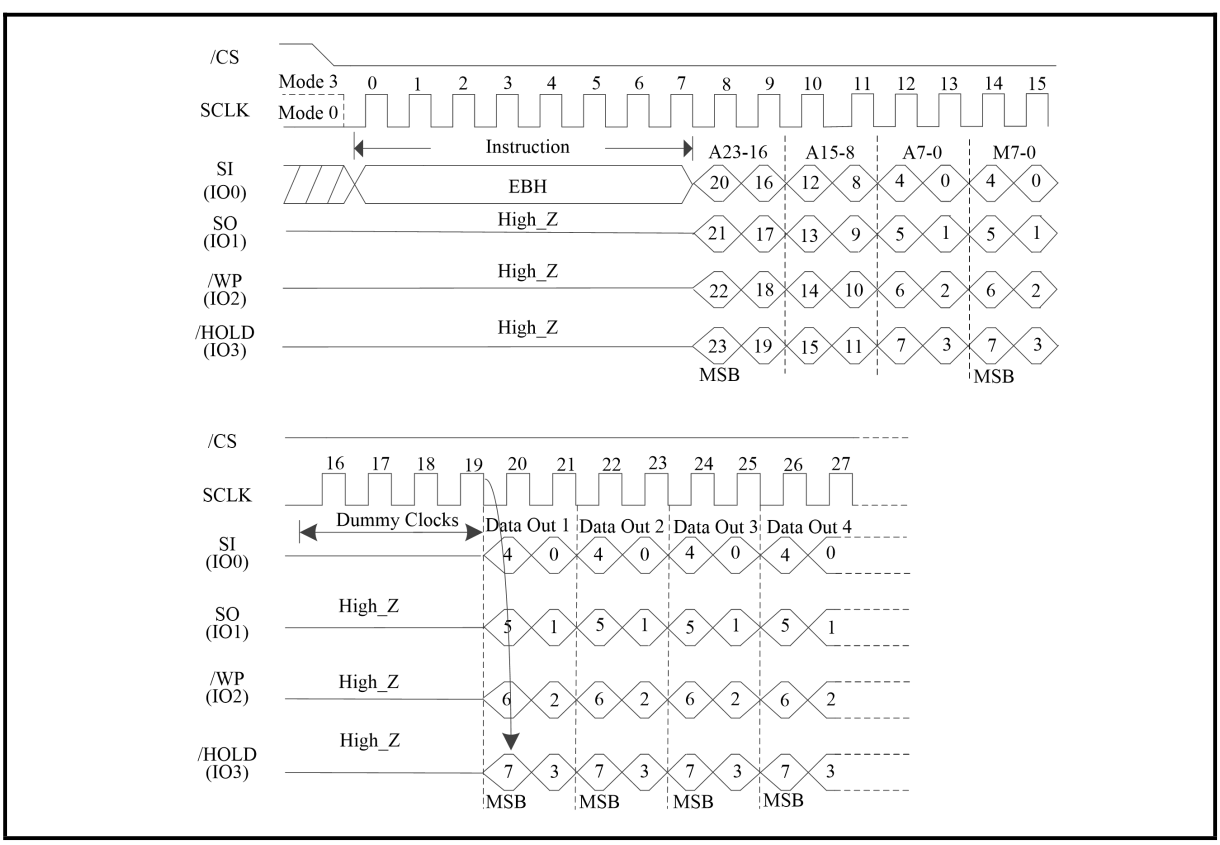


Figure 68. Quad I/O Fast Read Sequence Diagram (SPI Mode/4-Byte Address Mode; Initial instruction or previous (M5-4≠(1,0)))

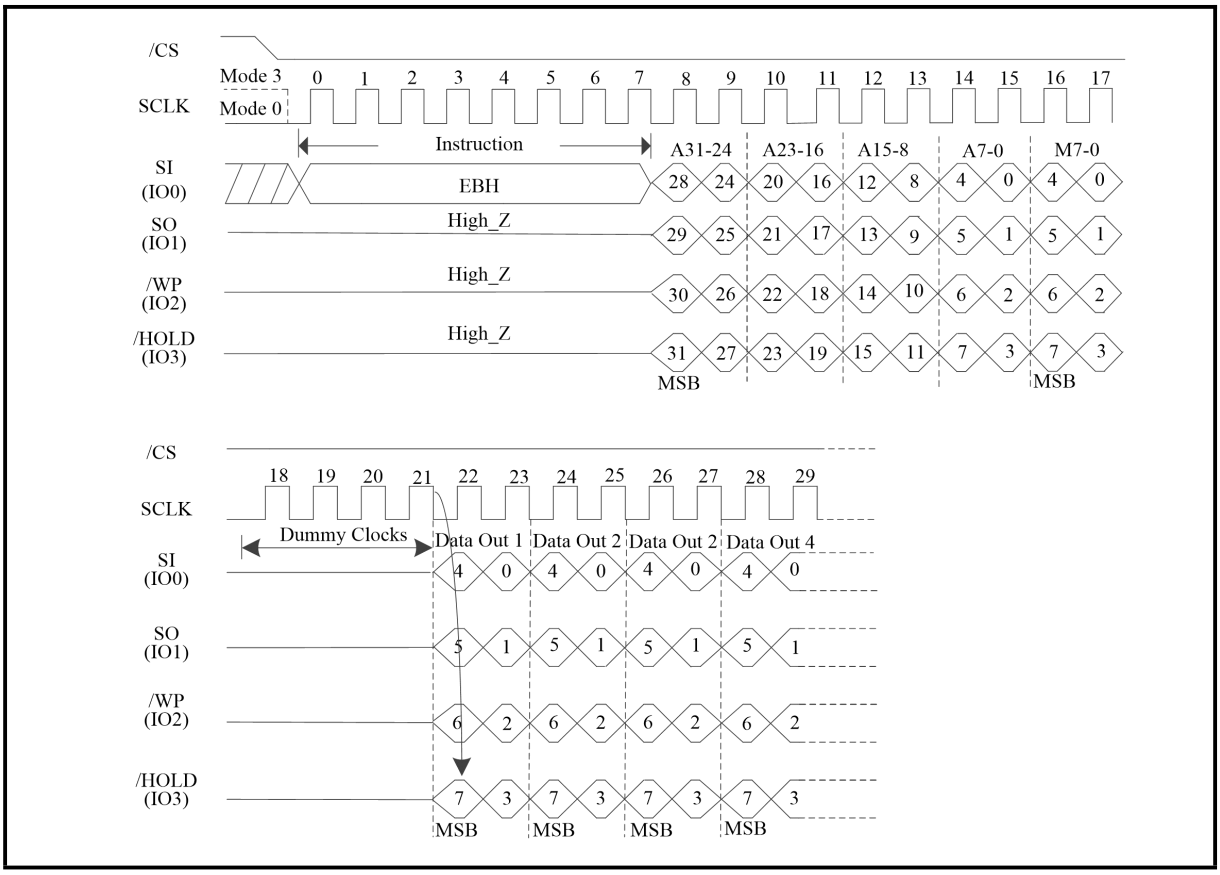


Figure 69. Quad I/O Fast Read Sequence Diagram (SPI Mode/3-Byte Address Mode; Initial instruction or previous (M5-4=(1,0)))

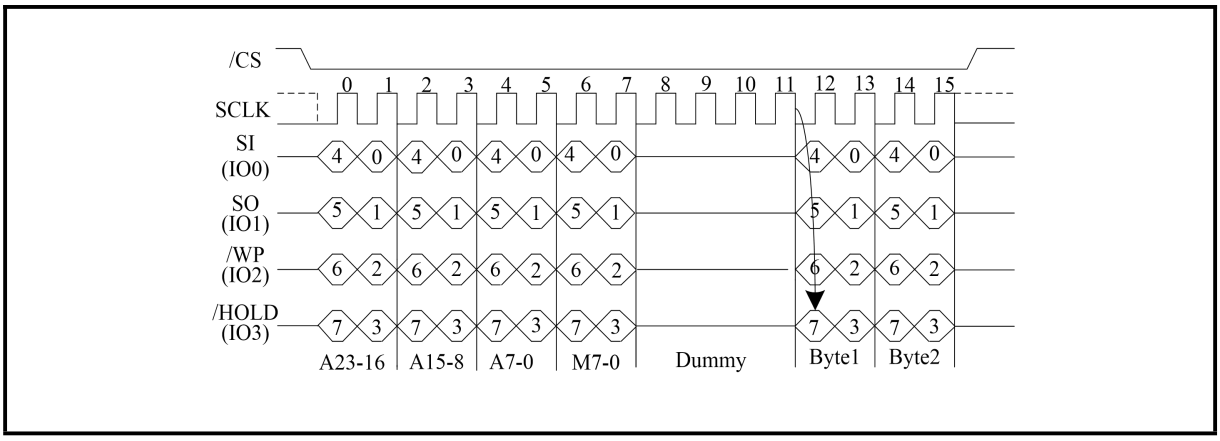
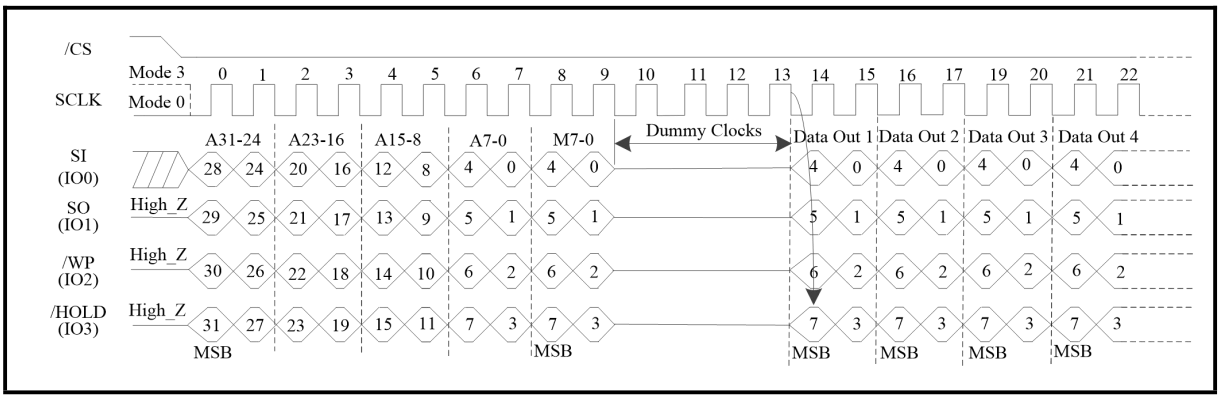


Figure 70. Quad I/O Fast Read Sequence Diagram (SPI Mode/4-Byte Address Mode; Initial instruction or previous (M5-4=(1,0)))



Quad I/O Fast Read with "8/16/32/64-Byte Wrap Around"

The Quad I/O Fast Read instruction can also be used to access a specific portion within a page by issuing a "Set Burst with Wrap" (77H) instruction prior to EBH. The "Set Burst with Wrap" (77H) instruction can either enable or disable the "Wrap Around" feature for the following EBH instructions. When "Wrap Around" is enabled, the data being accessed can be limited to either an 8, 16, 32 or 64-byte section of a 256-byte page. The output data starts at the initial address specified in the instruction, once it reaches the ending boundary of the 8/16/32/64-byte section, the output will wrap around to the beginning boundary automatically until /CS is pulled high to terminate the instruction.

The Burst with Wrap feature allows applications that use cache to quickly fetch a critical address and then fill the cache afterwards within a fixed length (8/16/32/64-byte) of data without issuing multiple read instructions.

The "Set Burst with Wrap" instruction allows three "Wrap Bits", W6-4 to be set. The W4 bit is used to enable or disable the "Wrap Around" operation while W6-5 are used to specify the length of the wrap around section within a page.

Fast Read Quad I/O (EBh) in QPI Mode

The Fast Read Quad I/O instruction is also supported in QPI mode, as shown in ***Figure 71-Figure 74.*** When QPI mode is enabled, the number of dummy clocks is configured by the "Set Read Parameters (C0h)" instruction to accommodate a wide range of applications with different needs for either maximum Fast Read frequency or minimum data access latency. Depending on the Read Parameter Bits P[5:4] setting, the number of dummy clocks can be configured as either 4, 4, 6 or 8. The default number of dummy clocks upon power up or after a Reset instruction is 4. In QPI mode, the "Continuous Read Mode" bits M7-0 are also considered as dummy clocks. In the default setting, the data output will follow the Continuous Read Mode bits immediately.

"Continuous Read Mode" feature is also available in QPI mode for Fast Read Quad I/O instruction. Please refer to the description on previous pages.

"Wrap Around" feature is not available in QPI mode for Fast Read Quad I/O instruction. To perform a read operation with fixed data length wrap around in QPI mode, a dedicated "Burst Read with Wrap" (0Ch) instruction must be used.

Figure 71. Quad I/O Fast Read Sequence Diagram (QPI Mode/3-Byte Address Mode; Initial instruction or previous (M5-4≠(1,0)))

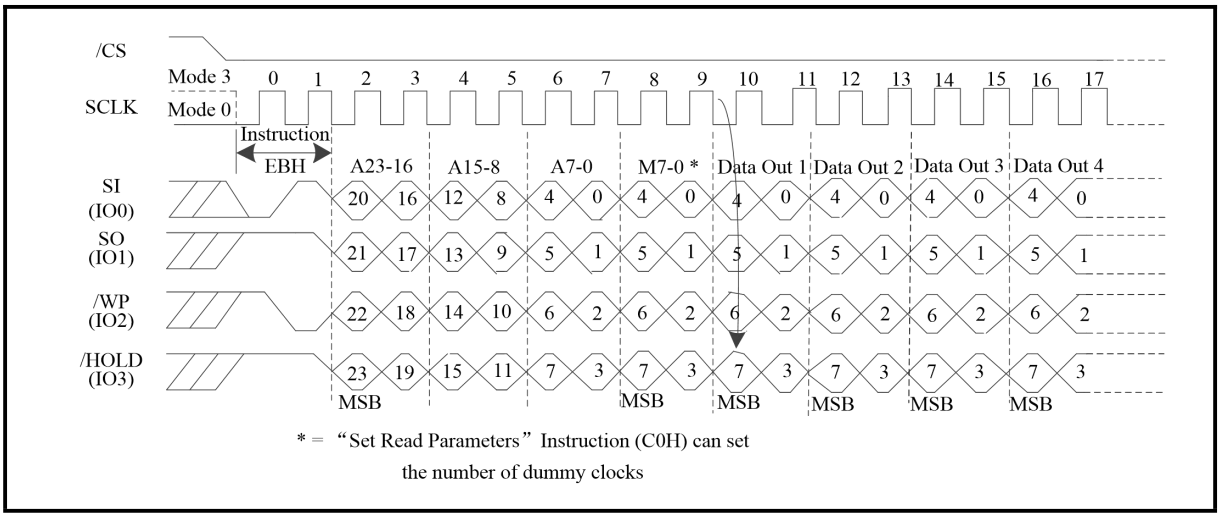


Figure 72. Quad I/O Fast Read Sequence Diagram (QPI Mode/4-Byte Address Mode; Initial instruction or previous (M5-4≠(1,0)))

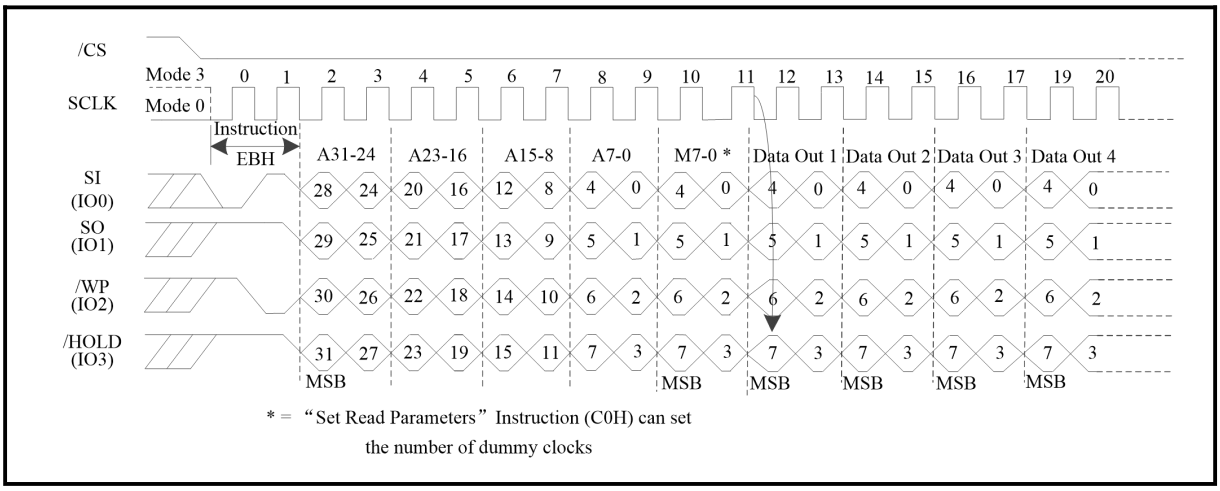


Figure 73. Quad I/O Fast Read Sequence Diagram (QPI Mode/3-Byte Address Mode; Initial instruction or previous (M5-4=(1,0)))

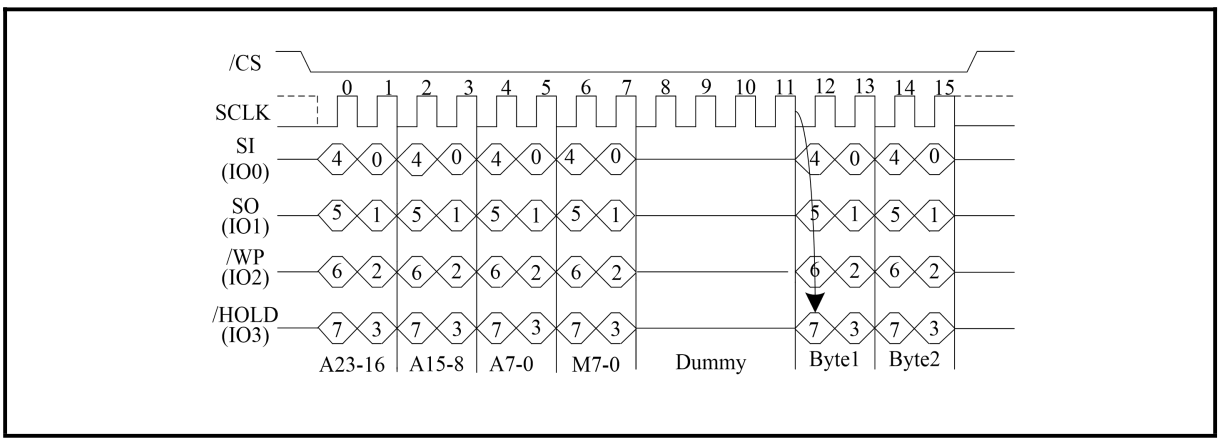
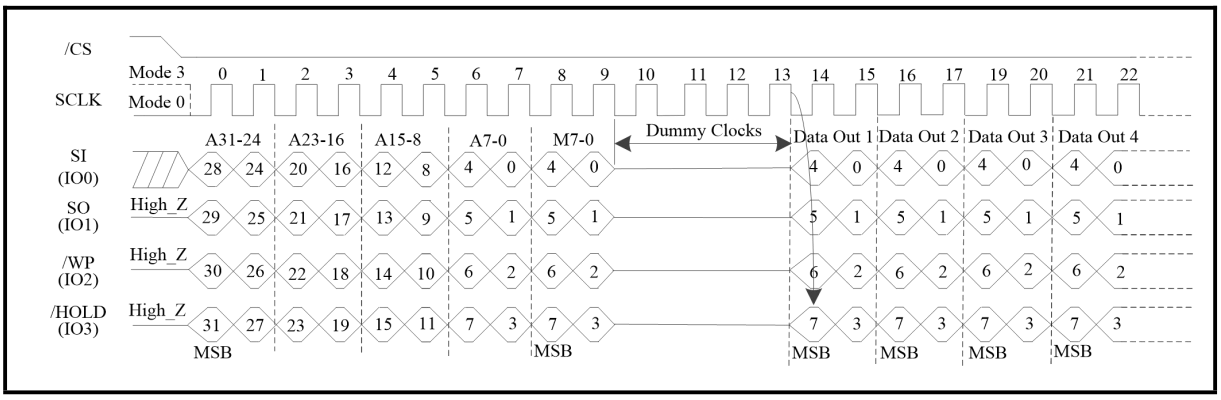


Figure 74. Quad I/O Fast Read Sequence Diagram (QPI Mode/4-Byte Address Mode; Initial instruction or previous (M5-4=(1,0)))



7.2.14 DTR Fast Read Quad I/O(EDH)

The DTR Fast Read Quad I/O (EDh) instruction is similar to the Fast Read Dual I/O (BBh) instruction except that address and data bits are input and output through four pins IO0, IO1, IO2 and IO3 and four Dummy clocks are required in SPI mode prior to the data output, as shown in ***Figure 75-Figure 82.*** The Quad Enable bit (QE) of Status Register must be set to enable.

DTR Fast Read Quad I/O with "Continuous Read Mode"

The Fast Read Quad I/O instruction can further reduce instruction overhead through setting the "Continuous Read Mode" bits (M7-0) after the input Address bits (A23/A31-0). The upper nibble of the (M7-4) controls the length of the next Fast Read Quad I/O instruction through the inclusion or exclusion of the first byte instruction code. The lower nibble bits of the (M3-0) are don't care ("x"). However, the IO pins should be high-impedance prior to the falling edge of the first data out clock.

If the "Continuous Read Mode" bits M5-4 = (1,0), then the next Fast Read Quad I/O instruction (after /CS is raised and then lowered) does not require the EDh instruction code. This reduces the instruction sequence by eight clocks and allows the Read address to be immediately entered after /CS is asserted low. If the "Continuous Read Mode" bits M5-4 do not equal to (1,0), the next instruction (after /CS is raised and then lowered) requires the first byte instruction code, thus returning to normal operation.

Figure 75. DTR Fast Read Quad I/O (SPI Mode/3-Byte Address Mode; Initial instruction or previous (M5-4≠(1,0)))

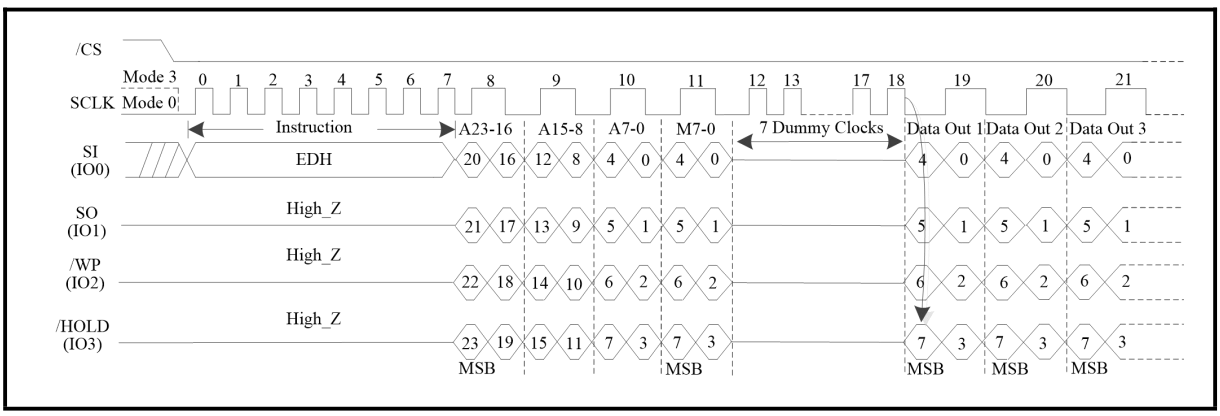


Figure 76. DTR Fast Read Quad I/O (SPI Mode/4-Byte Address Mode; Initial instruction or previous (M5-4≠(1,0)))

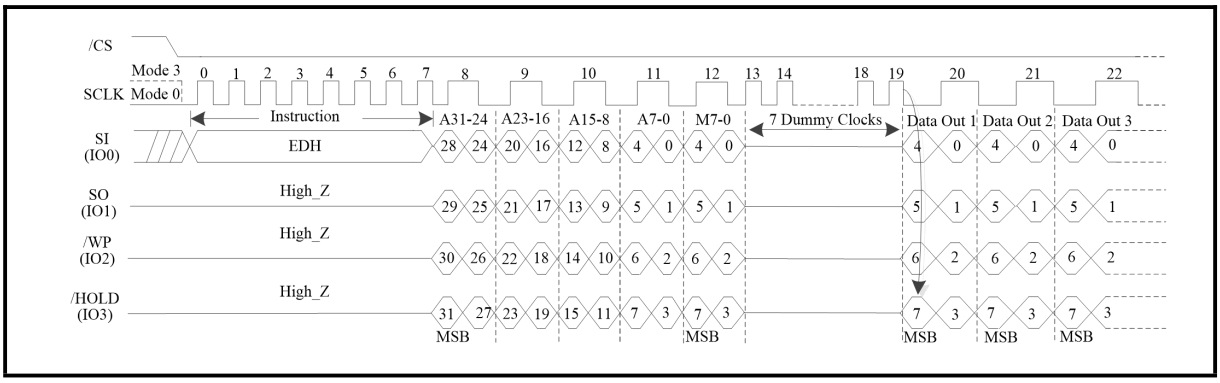


Figure 77. DTR Fast Read Quad I/O (SPI Mode/3-Byte Address Mode; Initial instruction or previous (M5-4=(1,0)))

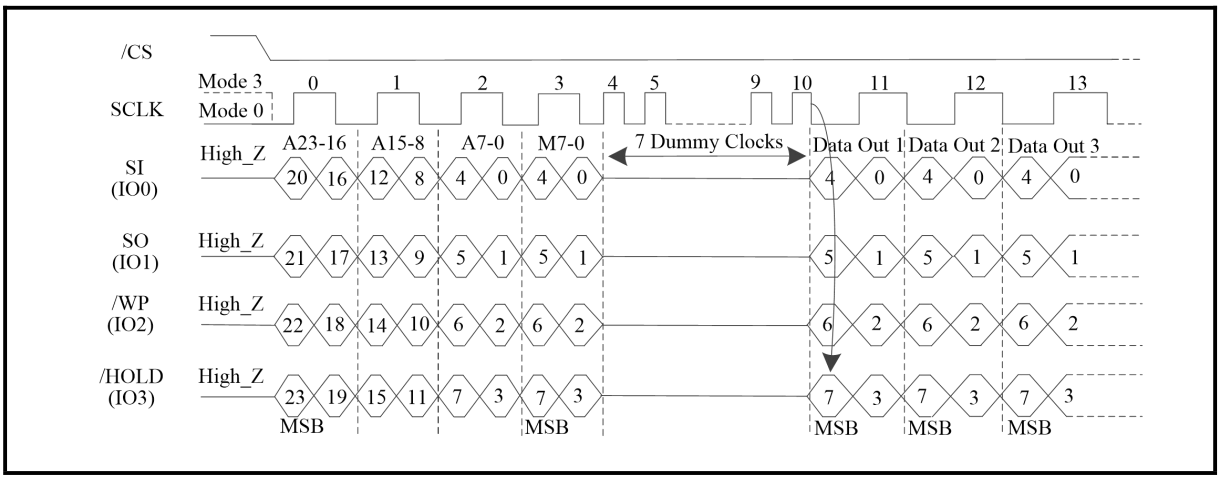
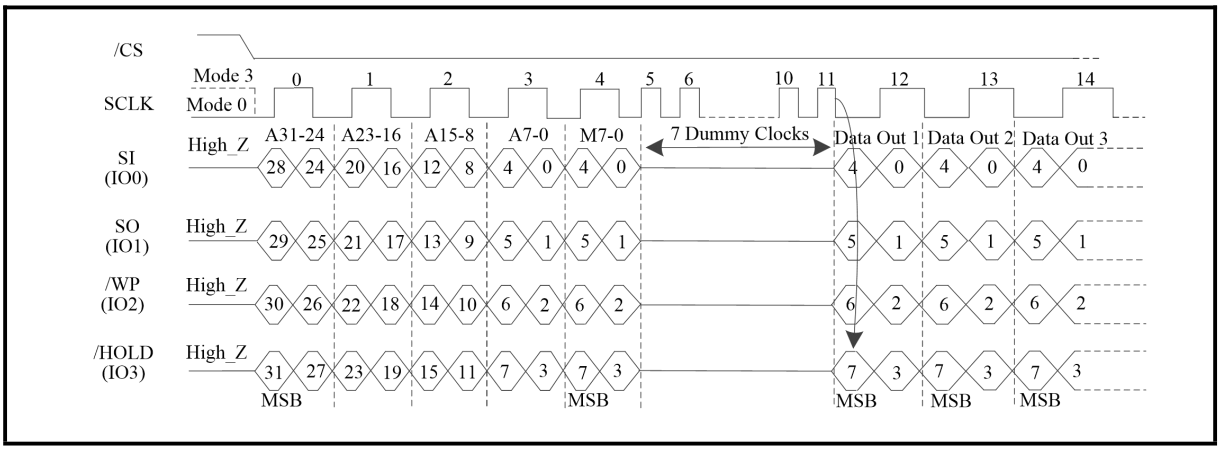


Figure 78. DTR Fast Read Quad I/O (SPI Mode/4-Byte Address Mode; Initial instruction or previous (M5-4=(1,0)))



DTR Fast Read Quad I/O with "8/16/32/64-Byte Wrap Around" in Standard SPI mode

The Fast Read Quad I/O instruction can also be used to access a specific portion within a page by issuing a "Set Burst with Wrap" (77h) instruction prior to EDh. The "Set Burst with Wrap" (77h) instruction can either enable or disable the "Wrap Around" feature for the following EDh instructions. When "Wrap Around" is enabled, the data being accessed can be limited to either an 8, 16, 32 or 64-byte section of a 256-byte page. The output data starts at the initial address specified in the instruction, once it reaches the ending boundary of the 8/16/32/64-byte section, the output will wrap around to the beginning boundary automatically until /CS is pulled high to terminate the instruction.

The Burst with Wrap feature allows applications that use cache to quickly fetch a critical address and then fill the cache afterwards within a fixed length (8/16/32/64-byte) of data without issuing multiple read instructions.

The "Set Burst with Wrap" instruction allows three "Wrap Bits", W6-4 to be set. The W4 bit is used to enable or disable the "Wrap Around" operation while W6-5 are used to specify the length of the wrap around section within a page.

DTR Fast Read Quad I/O (EDh) in QPI Mode

The DTR Fast Read Quad I/O instruction is also supported in QPI mode, as shown in ***Figure 79-Figure 82***. In QPI mode, the "Continuous Read Mode" can further reduce instruction overhead through setting the "Continuous Read Mode" bits (M7-0) after the input Address bits (A23/31-0). Please refer to the description on previous pages. If the "Continuous Read Mode" bits (M5-4)= (1,0), then the next Fast Read Quad I/O instruction(after /CS is raised and then lowered) does not require the EDH instruction code, The instruction sequence is shown in the followed Figure. If the "Continuous Read Mode" bits M5-4 do not equal to (1,0), the next instruction requires the first EDH instruction code, thus returning to normal operation. A "Continuous Read Mode" Reset instruction can also be used to reset (M5-4) before issuing normal instruction.

Figure 79. DTR Fast Read Quad I/O (QPI Mode/3-Byte Address Mode; Initial instruction or previous (M5-4≠(1,0)))

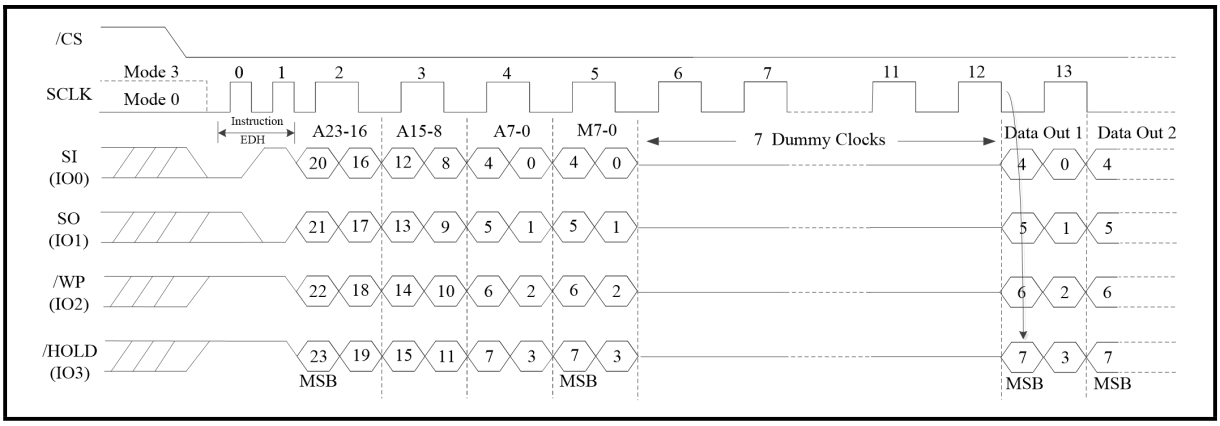


Figure 80. DTR Fast Read Quad I/O (QPI Mode/4-Byte Address Mode; Initial instruction or previous (M5-4≠(1,0)))

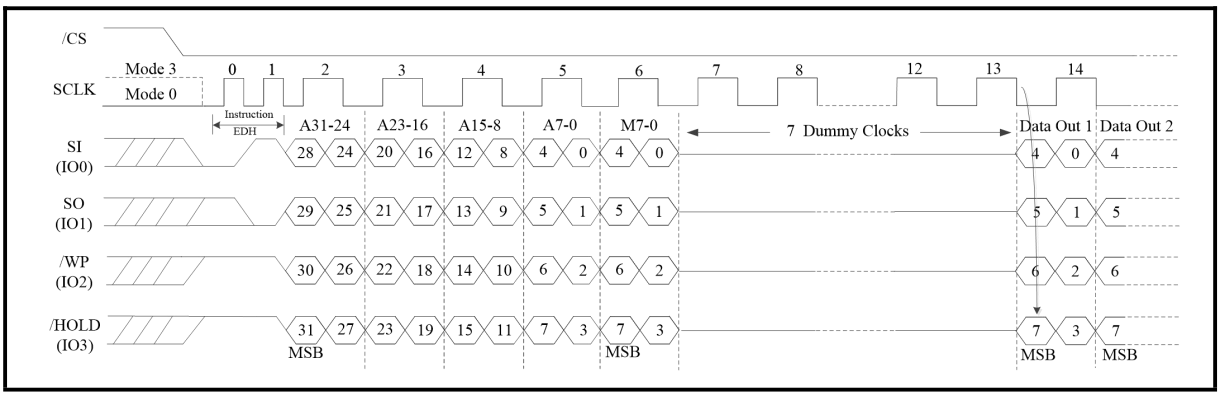


Figure 81. DTR Fast Read Quad I/O (QPI Mode/3-Byte Address Mode; Initial instruction or previous (M5-4=(1,0)))

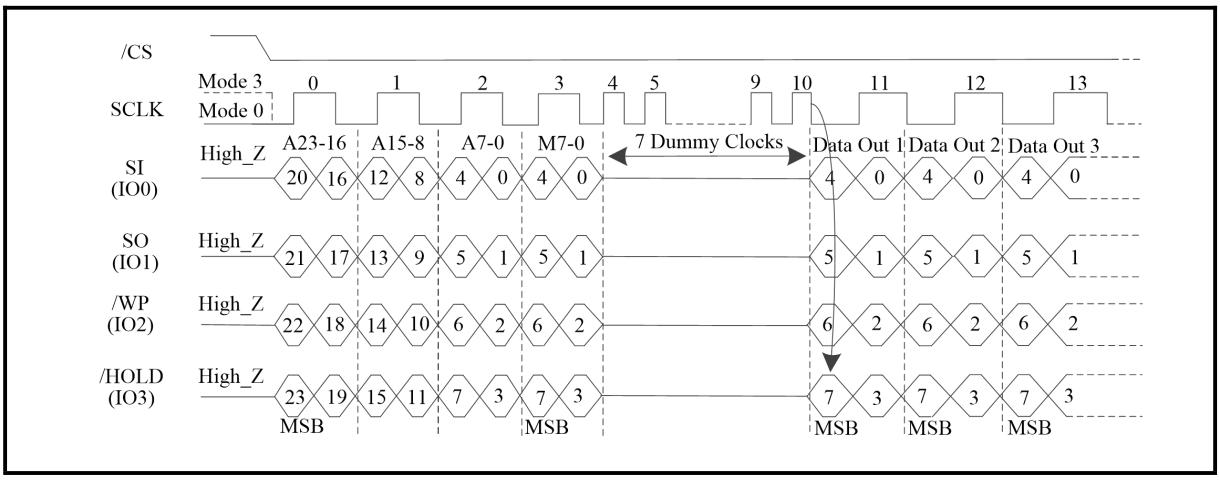
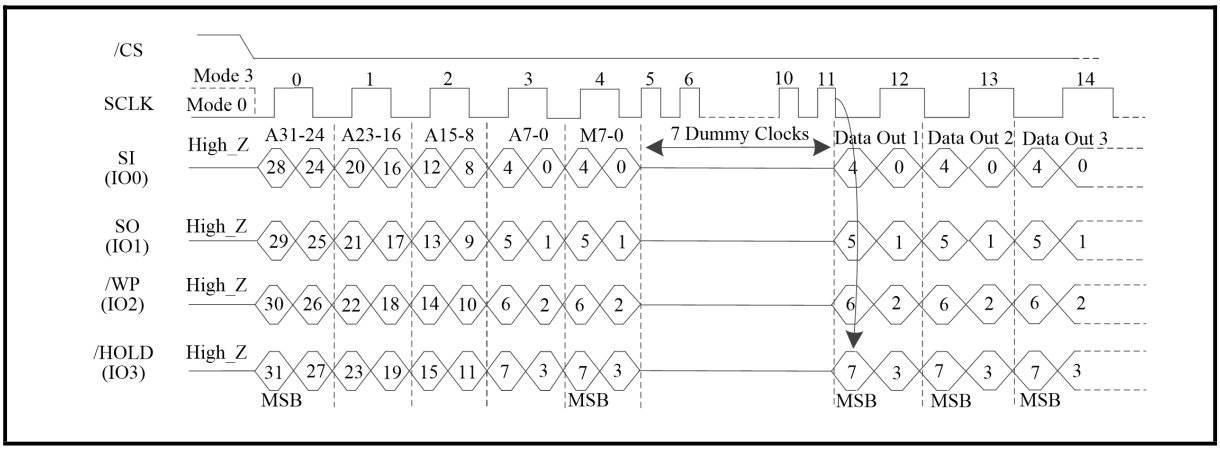


Figure 82. DTR Fast Read Quad I/O (QPI Mode/4-Byte Address Mode; Initial instruction or previous (M5-4=(1,0)))



7.2.15 Fast Read Quad I/O with 4-Byte Address (ECH)

The Fast Read Quad I/O with 4-Byte Address instruction is similar to the Quad I/O Fast Read instruction except that it requires 32-bit address instead of 24-bit address. No matter the device is operating in 3-Byte Address Mode or 4-byte Address Mode, the Fast Read Quad I/O with 4-Byte Address instruction will always require 32-bit address to access the entire 256Mb memory. The Quad Enable bit (QE) of Status Register must be set to enable.

Figure 83. Fast Read Quad I/O with 4-Byte Address (SPI Mode; Initial instruction or previous M5-4≠10)

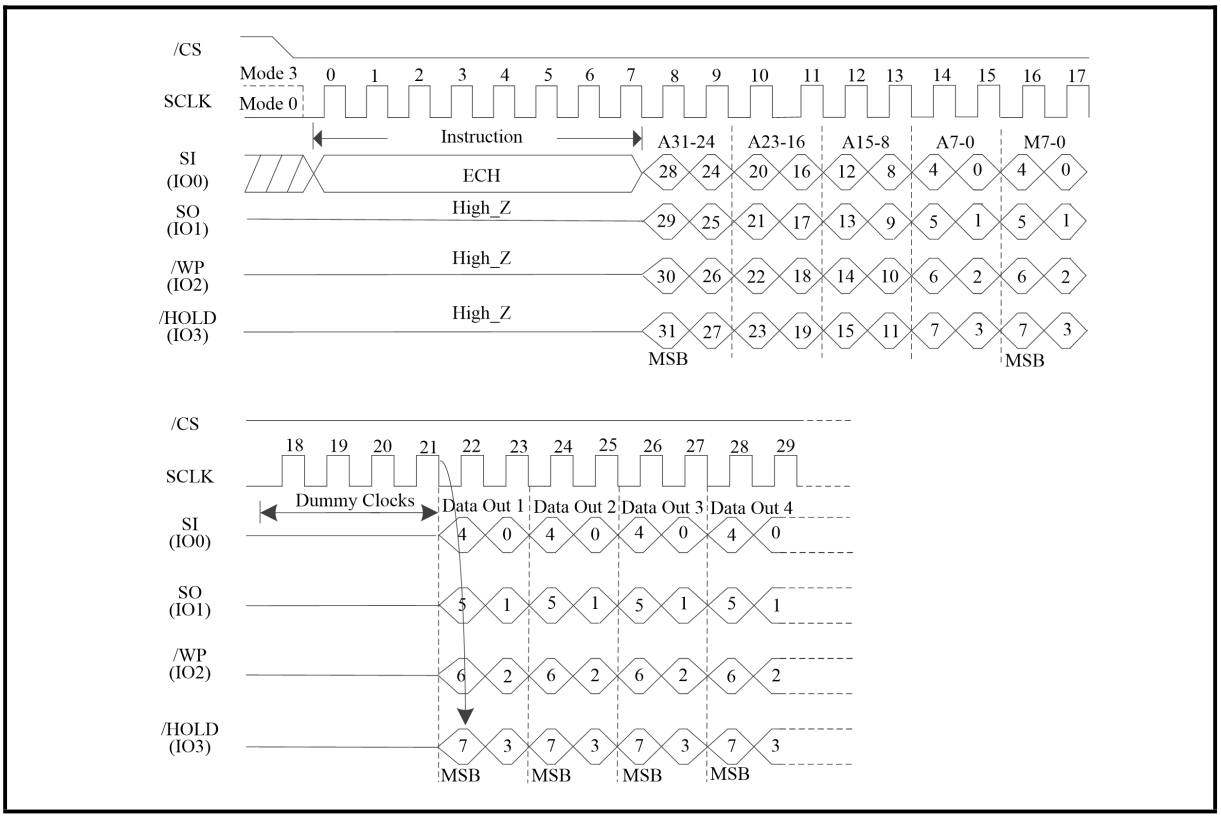
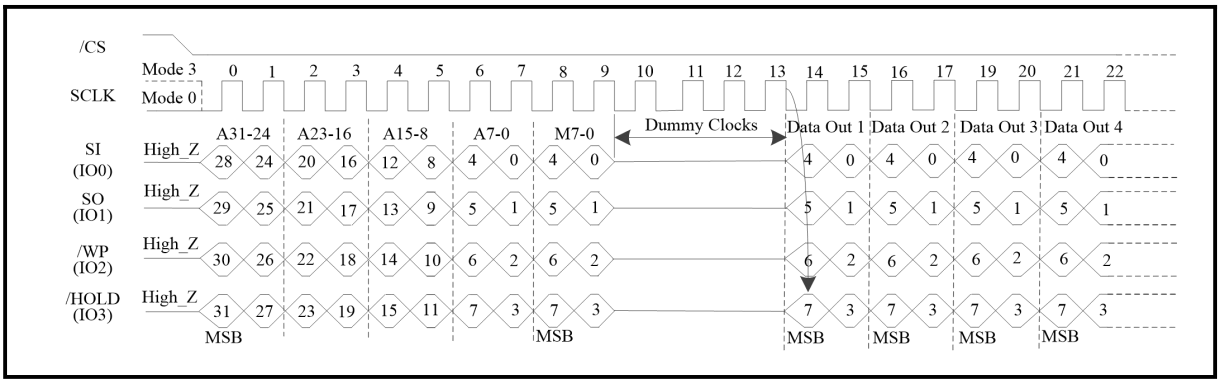


Figure 84. Fast Read Quad I/O with 4-Byte Address (SPI Mode; Initial instruction or previous M5-4=10)



Fast Read Quad I/O with 4-Byte Address with "8/16/32/64-Byte Wrap Around" in Standard SPI mode

The Fast Read Quad I/O with 4-Byte Address instruction can also be used to access a specific portion within a page by issuing a "Set Burst with Wrap" (77h) instruction prior to ECh. The "Set Burst with Wrap" (77h) instruction can either enable or disable the "Wrap Around" feature for the following ECh instructions. When "Wrap Around" is enabled, the data being accessed can be limited to either an 8, 16, 32 or 64-byte section of a 256-byte page. The output data starts at the initial address specified in the instruction, once it

reaches the ending boundary of the 8/16/32/64-byte section, the output will wrap around to the beginning boundary automatically until /CS is pulled high to terminate the instruction.

The Burst with Wrap feature allows applications that use cache to quickly fetch a critical address and then fill the cache afterwards within a fixed length (8/16/32/64-byte) of data without issuing multiple read instructions.

The “Set Burst with Wrap” instruction allows three “Wrap Bits”, W6-4 to be set. The W4 bit is used to enable or disable the “Wrap Around” operation while W6-5 are used to specify the length of the wrap around section within a page.

Fast Read Quad I/O with 4-Byte Address (ECh) in QPI Mode

The Fast Read Quad I/O with 4-Byte Address instruction is also supported in QPI mode, as shown in ***Figure 85-Figure 86***. When QPI mode is enabled, the number of dummy clocks is configured by the “Set Read Parameters (C0h)” instruction to accommodate a wide range of applications with different needs for either maximum Fast Read frequency or minimum data access latency. Depending on the Read Parameter Bits P[5:4] setting, the number of dummy clocks can be configured as either 4, 4, 6 or 8. The default number of dummy clocks upon power up or after a Reset instruction is 4. In QPI mode, the “Continuous Read Mode” bits M7-0 are also considered as dummy clocks. In the default setting, the data output will follow the Continuous Read Mode bits immediately.

“Continuous Read Mode” feature is also available in QPI mode for Fast Read Quad I/O with 4-Byte Address instruction. Please refer to the description on previous pages.

“Wrap Around” feature is not available in QPI mode for Fast Read Quad I/O with 4-Byte Address instruction. To perform a read operation with fixed data length wrap around in QPI mode, a dedicated “Burst Read with Wrap” (0Ch) instruction must be used.

Figure 85. Fast Read Quad I/O with 4-Byte Address (QPI Mode; Initial instruction or previous M5-4≠10)

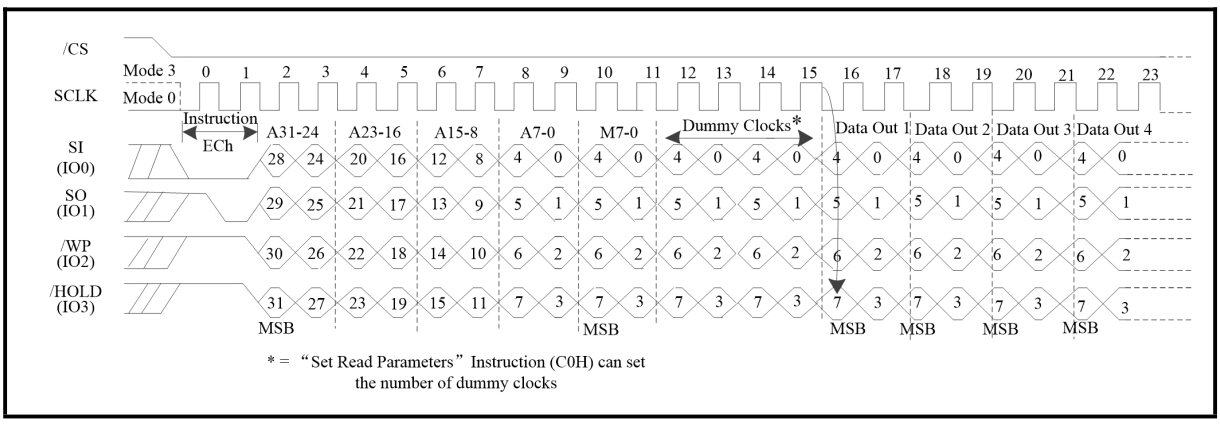
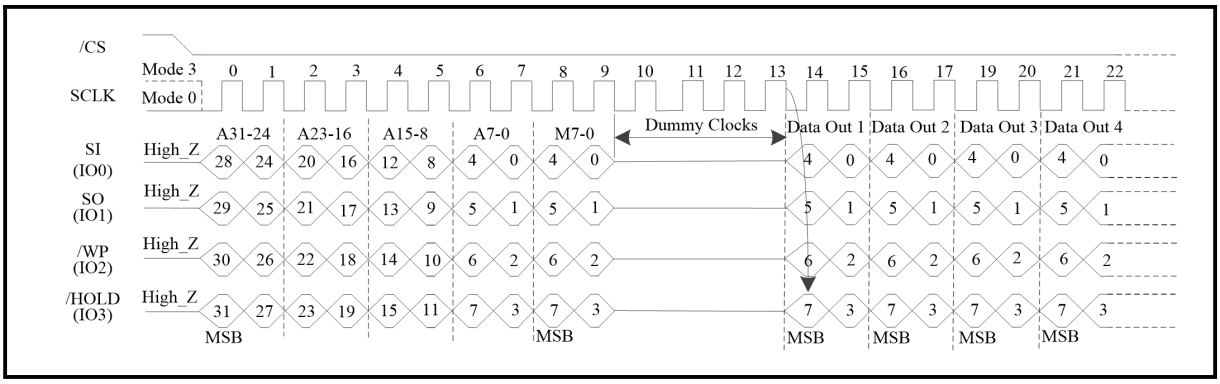


Figure 86. Fast Read Quad I/O with 4-Byte Address (QPI Mode; Initial instruction or previous M5-4=10)



7.2.16 DTR Quad I/O Fast Read with 4- Byte Address (EEH)

The DTR Quad I/O Fast Read with 4- Byte Address (EEh) instruction is similar to the Fast Read Dual I/O (BBh) instruction except that address and data bits are input and output through four pins IO0, IO1, IO2 and IO3 and four Dummy clocks are required in SPI mode prior to the data output, as shown in ***Figure 87-Figure 90***. The Quad Enable bit (QE) of Status Register must be set to enable.

DTR Fast Read Quad I/O with "Continuous Read Mode"

The DTR Quad I/O Fast Read with 4-Byte Address instruction can further reduce instruction overhead through setting the "Continuous Read Mode" bits (M7-0) after the input Address bits (A31-0) The upper nibble of the (M7-4) controls the length of the next Fast Read Quad I/O instruction through the inclusion or exclusion of the first byte instruction code. The lower nibble bits of the (M3-0) are don't care ("x"). However, the IO pins should be high-impedance prior to the falling edge of the first data out clock.

If the "Continuous Read Mode" bits M5-4 = (1,0), then the next DTR Quad I/O Fast Read with 4- Byte Address instruction (after /CS is raised and then lowered) does not require the EEh instruction code, as shown in ***Figure 88***. This reduces the instruction sequence by eight clocks and allows the Read address to be immediately entered after /CS is asserted low. If the "Continuous Read Mode" bits M5-4 do not equal to (1,0), the next instruction (after /CS is raised and then lowered) requires the first byte instruction code, thus returning to normal operation.

Figure 87. DTR Quad I/O Fast Read with 4- Byte Address (SPI Mode; Initial instruction or previous M5-4≠10)

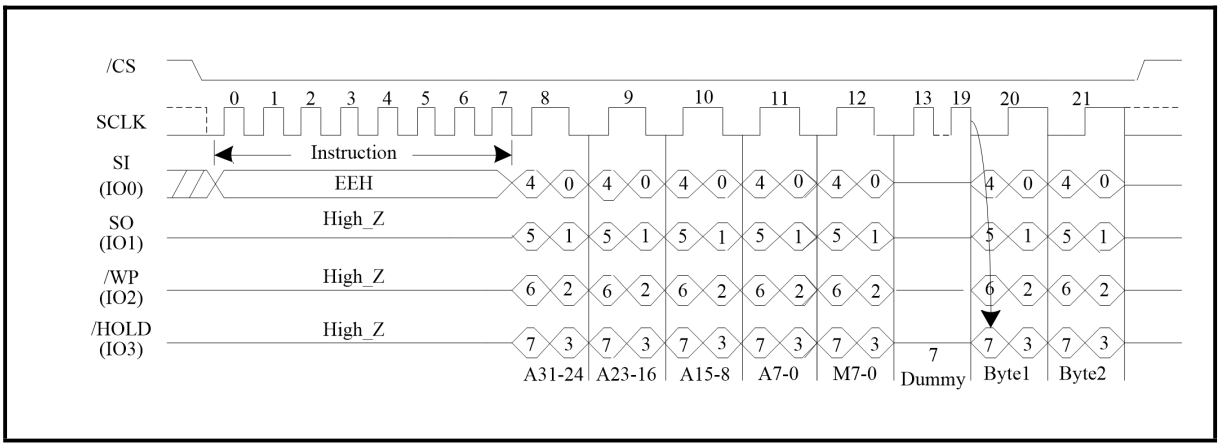
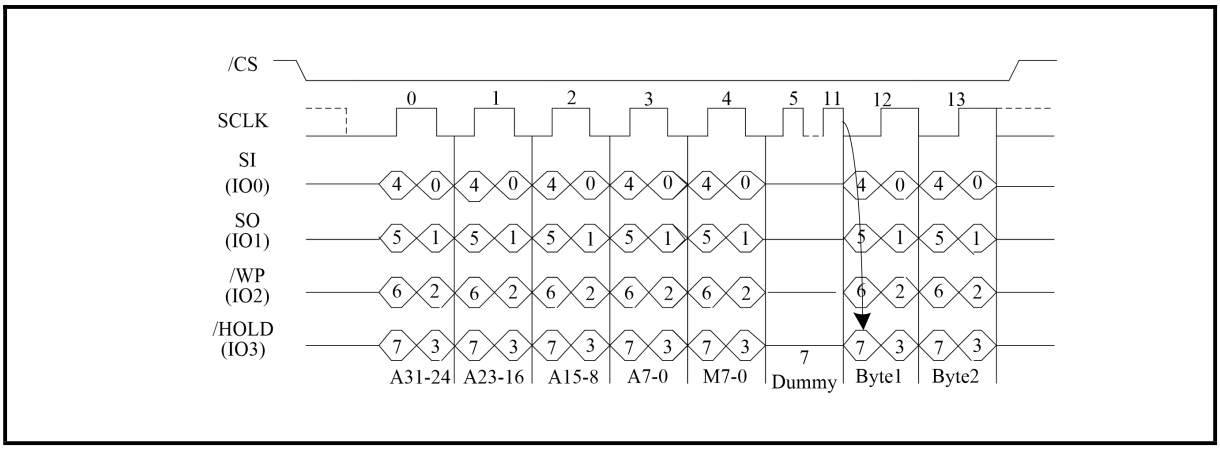


Figure 88. DTR Quad I/O Fast Read with 4- Byte Address (SPI Mode; Initial instruction or previous M5-4=10)



DTR Quad I/O Fast Read with 4- Byte Address with "8/16/32/64-Byte Wrap Around" in Standard SPI mode

The DTR Quad I/O Fast Read with 4- Byte Address instruction can also be used to access a specific portion within a page by issuing a “Set Burst with Wrap” (77h) instruction prior to EEh. The “Set Burst with Wrap” (77h) instruction can either enable or disable the “Wrap Around” feature for the following EEh instructions. When “Wrap Around” is enabled, the data being accessed can be limited to either an 8, 16, 32 or 64-byte section of a 256-byte page. The output data starts at the initial address specified in the instruction, once it reaches the ending boundary of the 8/16/32/64-byte section, the output will wrap around to the beginning boundary automatically until /CS is pulled high to terminate the instruction.

The Burst with Wrap feature allows applications that use cache to quickly fetch a critical address and then fill the cache afterwards within a fixed length (8/16/32/64-byte) of data without issuing multiple read instructions.

The “Set Burst with Wrap” instruction allows three “Wrap Bits”, W6-4 to be set. The W4 bit is used to enable or disable the “Wrap Around” operation while W6-5 are used to specify the length of the wrap around section within a page.

DTR Quad I/O Fast Read with 4- Byte Address (EEh) in QPI Mode

“Continuous Read Mode” feature is also available in QPI mode for DTR Quad I/O Fast Read with 4- Byte Address instruction.

“Wrap Around” feature is not available in QPI mode for Fast Read Quad I/O instruction. To perform a read operation with fixed data length wrap around in QPI mode, a dedicated “Burst Read with Wrap” (0Ch) instruction must be used.

Figure 89. DTR Quad I/O Fast Read with 4- Byte Address (QPI Mode; Initial instruction or previous M5-4≠10)

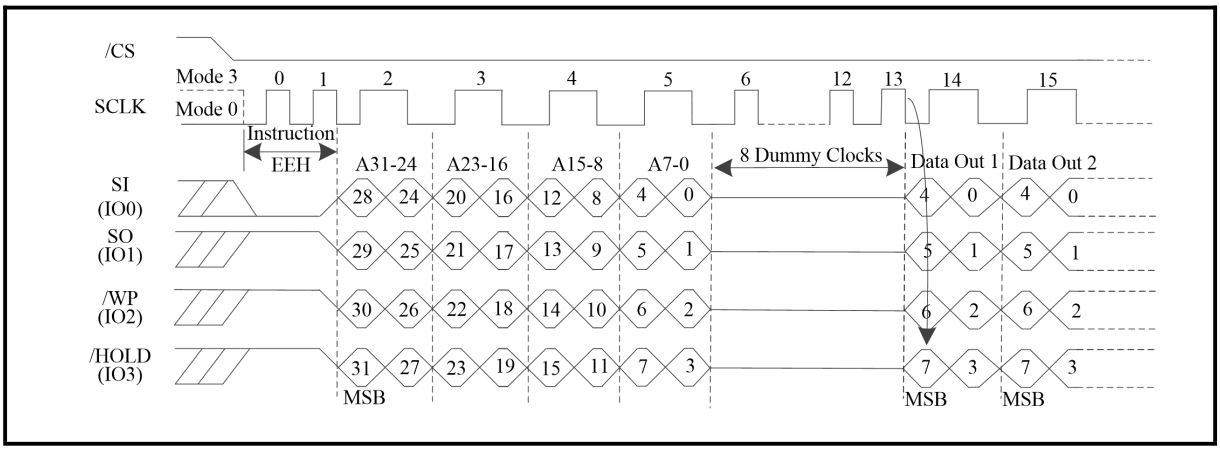
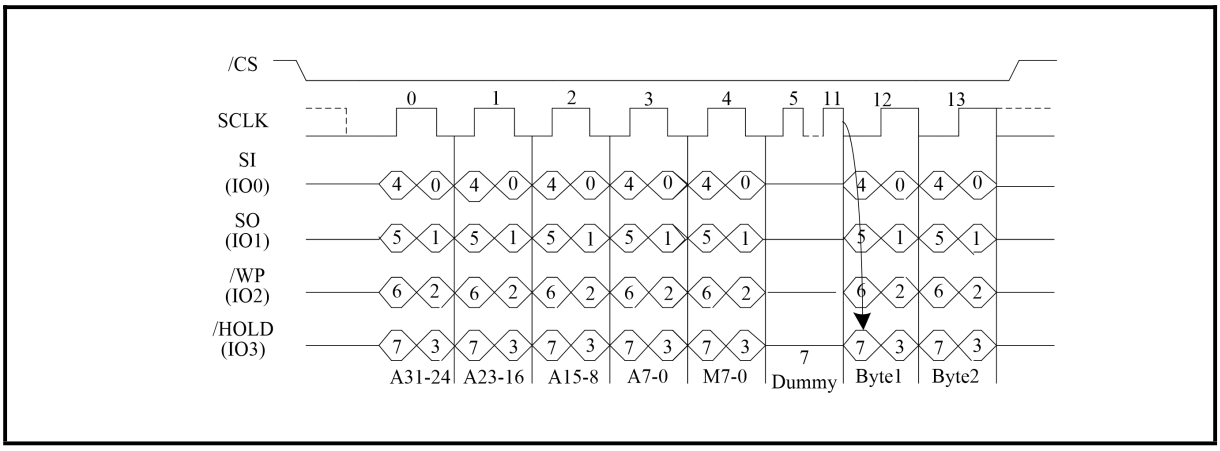


Figure 90. DTR Quad I/O Fast Read with 4- Byte Address (QPI Mode; Initial instruction or previous M5-4=10)



7.2.17 Quad I/O Word Fast Read (E7H)

The Quad I/O Word Fast Read instruction is similar to the Quad Fast Read instruction except that the lowest address bit (A0) must equal 0 and 2-dummy clock. The instruction sequence is shown in the followed ***Figure 91-Figure 94***, the first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The Quad Enable bit (QE) of Status Register (S9) must be set to enable for the Quad I/O Word Fast Read instruction. The Quad Enable bit (QE) of Status Register must be set to enable.

Quad I/O Word Fast Read with "Continuous Read Mode"

The Quad I/O Word Fast Read instruction can further reduce instruction overhead through setting the "Continuous Read Mode" bits (M7-0) after the input 3-byte Address bits (A23-0). If the "Continuous Read Mode" bits (M5-4) = (1, 0), then the next Quad I/O Fast Read instruction (after /CS is raised and then lowered) does not require the E7H instruction code, the instruction sequence is shown in the followed ***Figure 93-Figure 94***. If the "Continuous Read Mode" bits M5-4 do not equal to (1,0), the next instruction requires the first E7H instruction code, thus returning to normal operation. A "Continuous Read Mode" Reset instruction can also be used to reset (M5-4) before issuing normal instruction.

Figure 91. Quad I/O Word Fast Read Sequence Diagram (SPI Mode/3-Byte Address Mode; Initial instruction or previous (M5-4)≠(1,0))

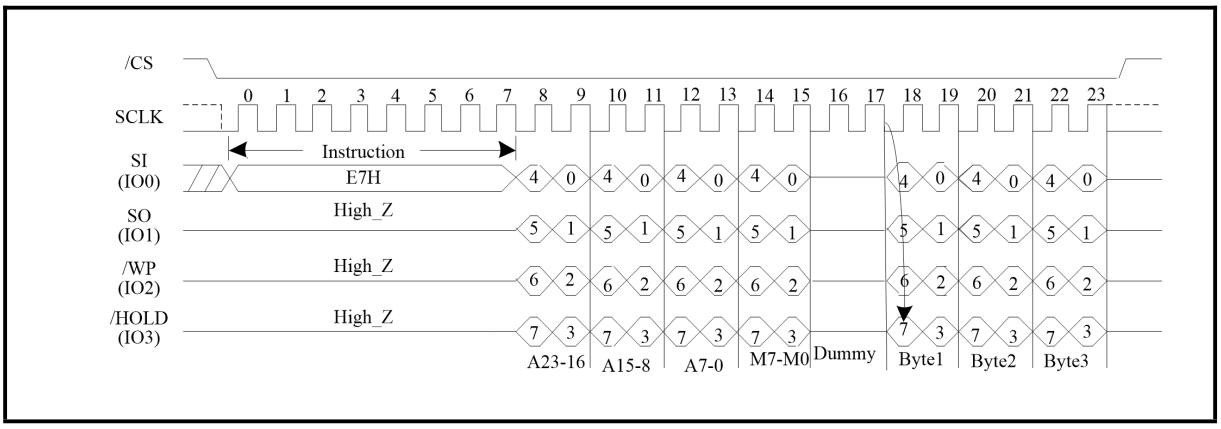


Figure 92. Quad I/O Word Fast Read Sequence Diagram (SPI Mode/4-Byte Address Mode; Initial instruction or previous (M5-4)≠(1,0))

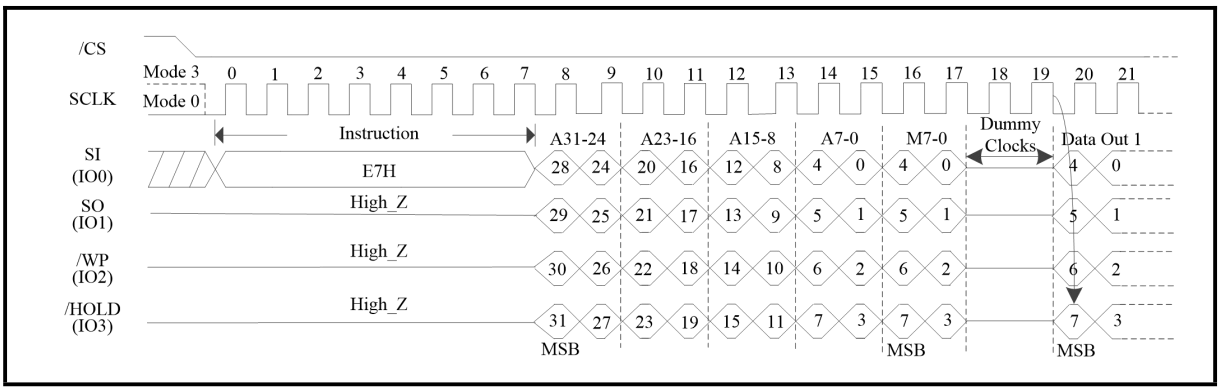


Figure 93. Quad I/O Word Fast Read Sequence Diagram (SPI Mode/3-Byte Address Mode; Initial instruction or previous (M5-4)=(1,0))

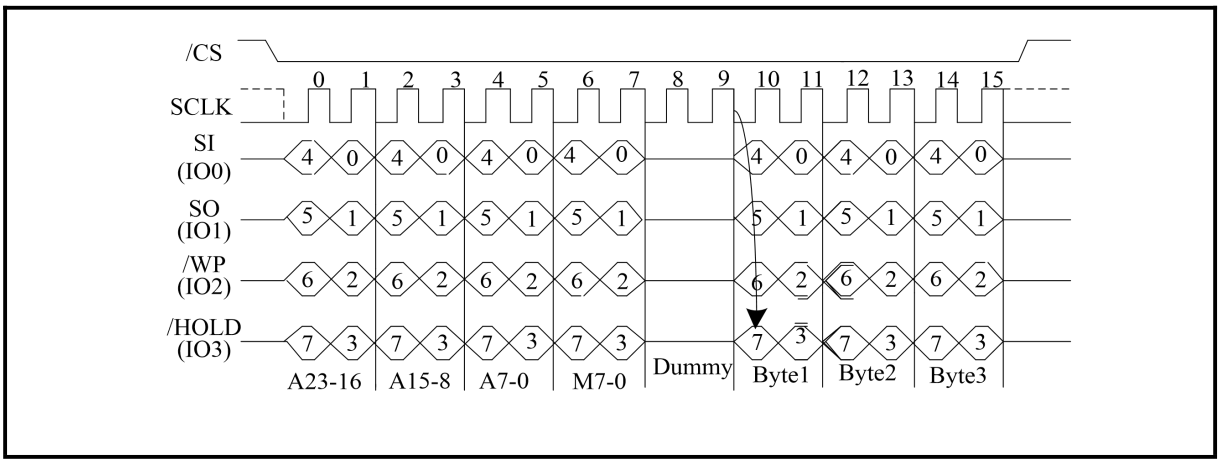
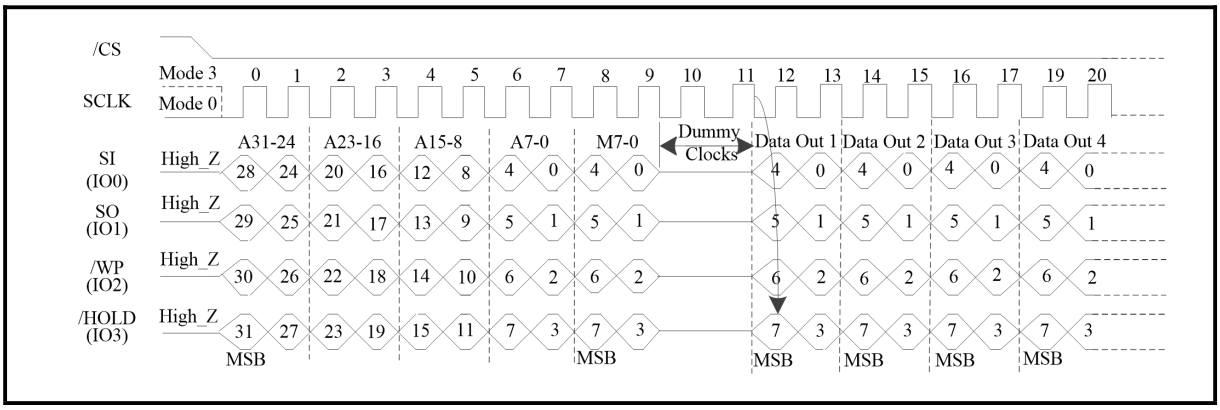


Figure 94. Quad I/O Word Fast Read Sequence Diagram (SPI Mode/4-Byte Address Mode; Initial instruction or previous (M5-4)=(1,0))



Quad I/O Word Fast Read with "8/16/32/64-Byte Wrap Around" in standard SPI mode

The Quad I/O Fast Read instruction can also be used to access a specific portion within a page by issuing a "Set Burst with Wrap" (77H) instruction prior to E7H. The "Set Burst with Wrap" (77H) instruction can either enable or disable the "Wrap Around" feature for the following E7H instructions. When "Wrap Around" is enabled, the data being accessed can be limited to either an 8, 16, 32 or 64-byte section of a 256-byte page. The output data starts at the initial address specified in the instruction, once it reaches the ending boundary of the 8/16/32/64-byte section, the output will wrap around to the beginning boundary automatically until /CS is pulled high to terminate the instruction.

The Burst with Wrap feature allows applications that use cache to quickly fetch a critical address and then fill the cache afterwards within a fixed length (8/16/32/64-byte) of data without issuing multiple read instructions.

The "Set Burst with Wrap" instruction allows three "Wrap Bits", W6-4 to be set. The W4 bit is used to enable or disable the "Wrap Around" operation while W6-5 are used to specify the length of the wrap around section within a page.

7.2.18 Set Burst with Wrap (77H)

See ***Figure 95-Figure 96,*** The Set Burst with Wrap instruction is used in conjunction with “EBH”, “EDH”, “ECH”, “EEH” and “E7H” instructions to access a fixed length of 8/16/32/64-byte section within a 256-byte page, in standard SPI mode.

The Set Burst with Wrap instruction sequence:/CS goes low ->Send Set Burst with Wrap instruction ->Send24 Dummy bits ->Send 8 bits” Wrap bits”->/CS goes high.

If W6-4 is set by a Set Burst with Wrap instruction, all the following “EBH”, “EDH”, “ECH”, “EEH” and “E7H” instructions will use the W6-4 setting to access the 8/16/32/64-byte section within any page. To exit the “Wrap Around” function and return to normal read operation, another Set Burst with Wrap instruction should be issued to set W4=1. The default value of W4 upon power on is 1.

W6 , W5	W4 = 0		W4 =1 (DEFAULT)	
	Wrap Around	Wrap Length	Wrap Around	Wrap Length
0 0	Yes	8-byte	No	N/A
0 1	Yes	16-byte	No	N/A
1 0	Yes	32-byte	No	N/A
1 1	Yes	64-byte	No	N/A

Figure 95. Set Burst with Wrap Sequence Diagram (SPI Mode only/3-Byte Address Mode)

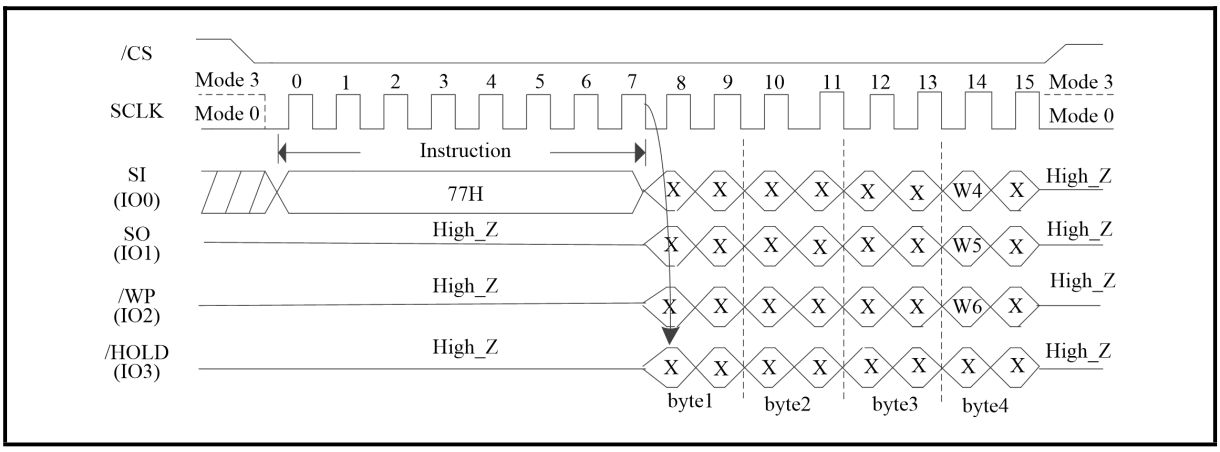
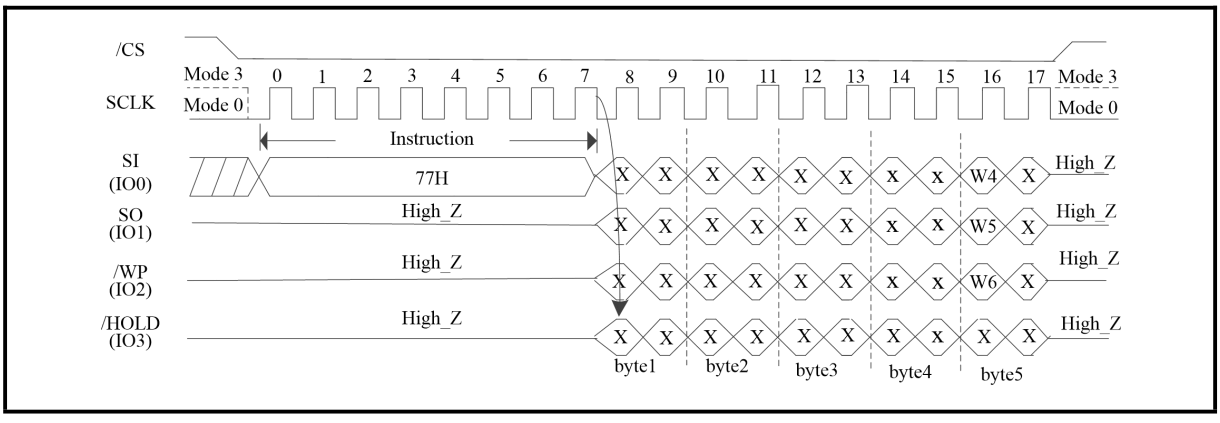


Figure 96. Set Burst with Wrap Sequence Diagram (SPI Mode only/4-Byte Address Mode)



7.2.19 Set Read Parameters (C0H)

In QPI mode, to accommodate a wide range of applications with different needs for either maximum read frequency or minimum data access latency, “Set Read Parameters (C0h)” instruction can be used to configure the number of dummy clocks for “0BH”, “EBH”, “ECH”, “0CH”,

“4BH”, “48H”, “5AH” and “E2H” instructions, as shown in ***Table 21***, and to configure the number of bytes of “Wrap Length” for the “0CH” and “0EH” instruction.

Table 21. Instructions that configurable dummy number

Mode	Instruction	
QPI	Fast Read	0Bh
	Fast Read Quad I/O	EBh
	Fast Read Quad I/O with 4-Byte Address	ECh
	Burst Read with Wrap	0Ch
	Read Unique ID Number	4Bh
	Read Security Registers	48h
	Read Serial Flash Discoverable Parameter	5Ah
	Read SPB Status	E2h

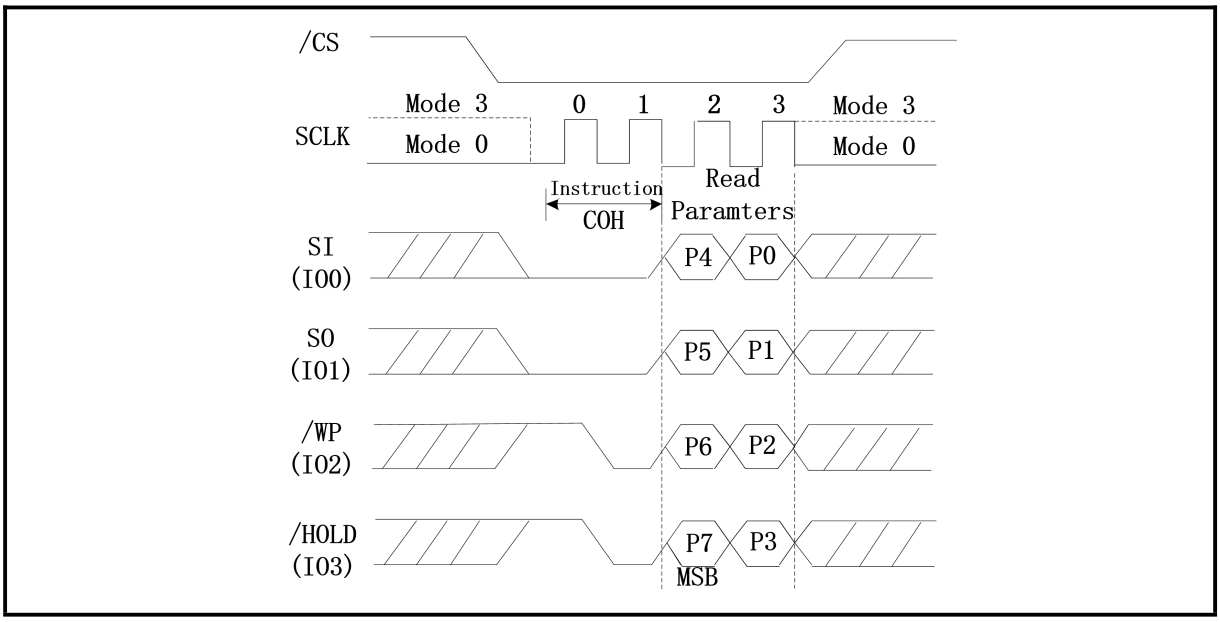
In Standard SPI mode, the “Set Read Parameters (C0h)” instruction is not accepted. The dummy clocks for various Fast Read instructions in Standard/Dual/Quad SPI mode are fixed, please refer to the Instruction ***Table 19*** for details. The “Wrap Length” is set by W5-4 bit in the “Set Burst with Wrap (77h)” instruction. This setting will remain unchanged when the device is switched from Standard SPI mode to QPI mode.

The default “Wrap Length” after a power up or a Reset instruction is 8 bytes, the default number of dummy clocks is 4. The number of dummy clocks is only programmable for “0BH”, “EBH”, “ECH”, “0CH”, “4BH”, “48H”, “5AH” and “E2H”instructions in the QPI mode. Whenever the device is switched from SPI mode to QPI mode, the number of dummy clocks should be set again, prior to any “0BH”, “EBH”, “ECH”, “0CH”, “4BH”, “48H”, “5AH” and “E2H” instructions.

P5 – P4	DUMMY CLOCKS	MAXIMUM READ FREQ.	MAXIMUM READ FREQ. (A[1:0]=0,0 VCC=2.7V~2.9V)	MAXIMUM READ FREQ. (A[1:0]=0,0 VCC=3.0V~3.6V)
0 0	4	55MHz	80MHz	80MHz
0 1	4	55MHz	80MHz	80MHz
1 0	6	80MHz	80MHz	100MHz
1 1	8	80MHz	80MHz	100MHz

P1 – P0	WRAP LENGTH
0 0	8-byte
0 1	16-byte
1 0	32-byte
1 1	64-byte

Figure 97. Burst Read with Wrap (QPI Mode only)



7.2.20 Burst Read with Wrap (0CH)

The “Burst Read with Wrap (0Ch)” instruction provides an alternative way to perform the read operation with “Wrap Around” in QPI mode. The instruction is similar to the “Fast Read (0Bh)” instruction in QPI mode, except the addressing of the read operation will “Wrap Around” to the beginning boundary of the “Wrap Length” once the ending boundary is reached.

The “Wrap Length” and the number of dummy clocks can be configured by the “Set Read Parameters (C0h)” instruction

Figure 98. Burst Read with Wrap (QPI Mode only/3-Byte Address Mode)

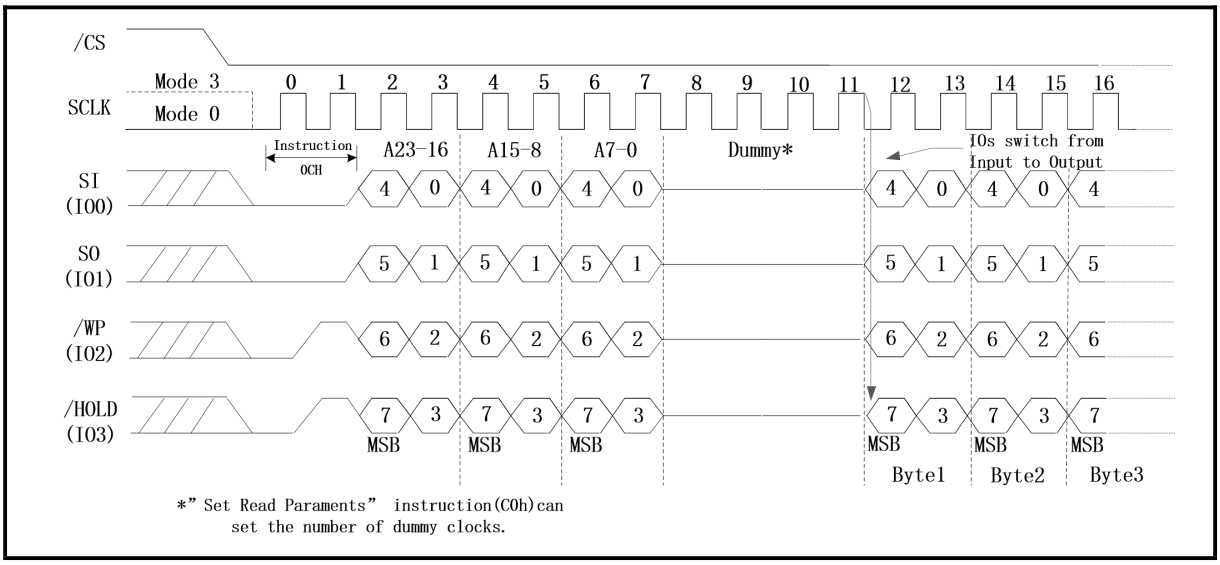
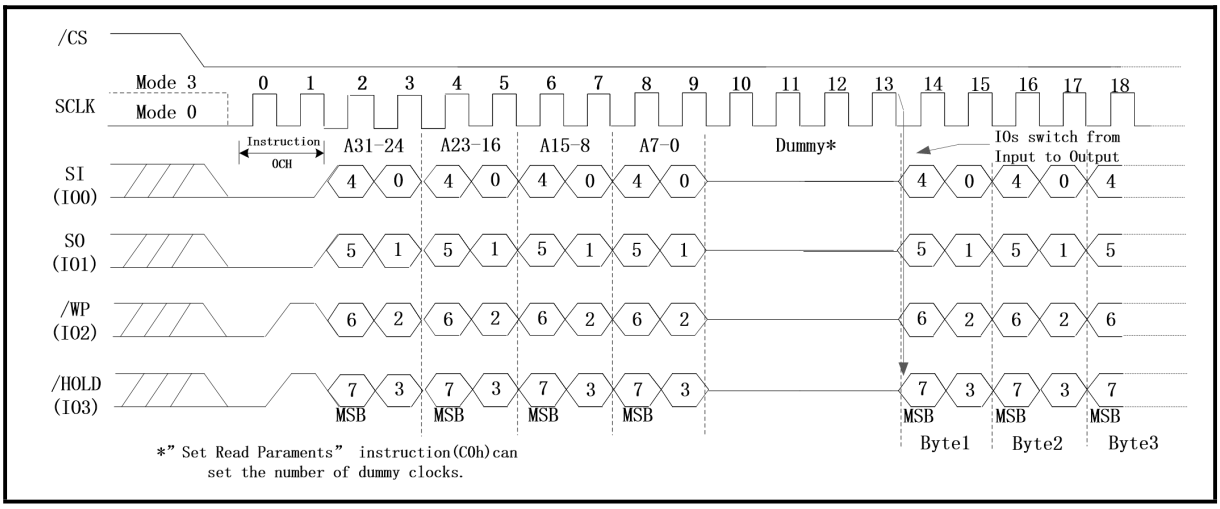


Figure 99. Burst Read with Wrap (QPI Mode only/4-Byte Address Mode)



7.2.21 DTR Burst Read with Wrap (0EH)

The “DTR Burst Read with Wrap (0Eh)” instruction provides an alternative way to perform the read operation with “Wrap Around” in QPI mode. The instruction is similar to the “Fast Read (0Bh)” instruction in QPI mode, except the addressing of the read operation will “Wrap Around” to the beginning boundary of the “Wrap Length” once the ending boundary is reached.

The “Wrap Length” can be configured by the “Set Read Parameters (C0h)” instruction.

Figure 100. DTR Burst Read with Wrap (QPI Mode only/3-Byte Address Mode)

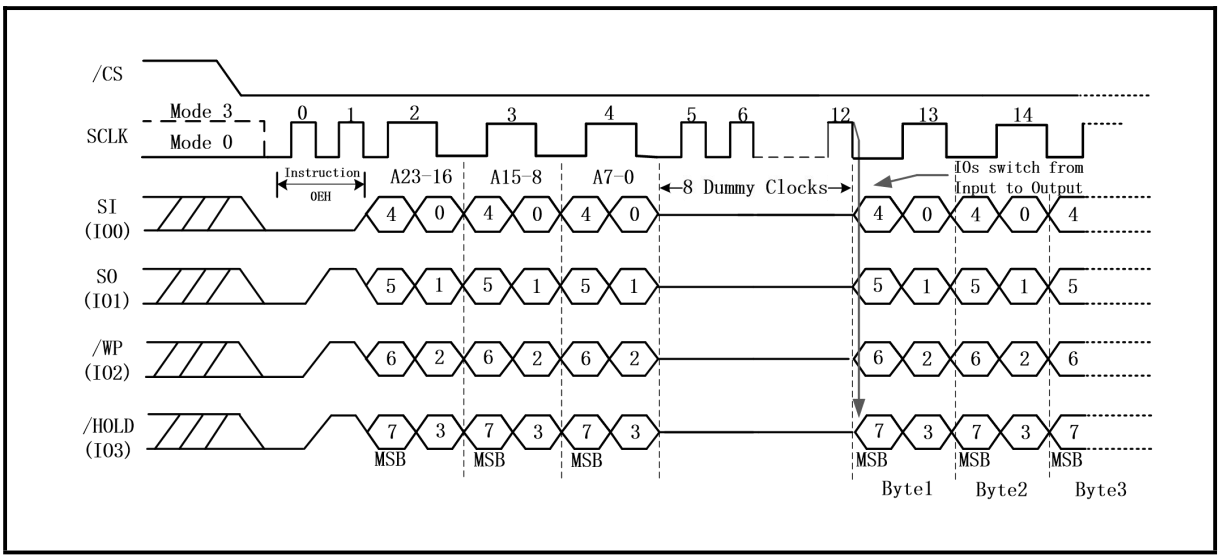
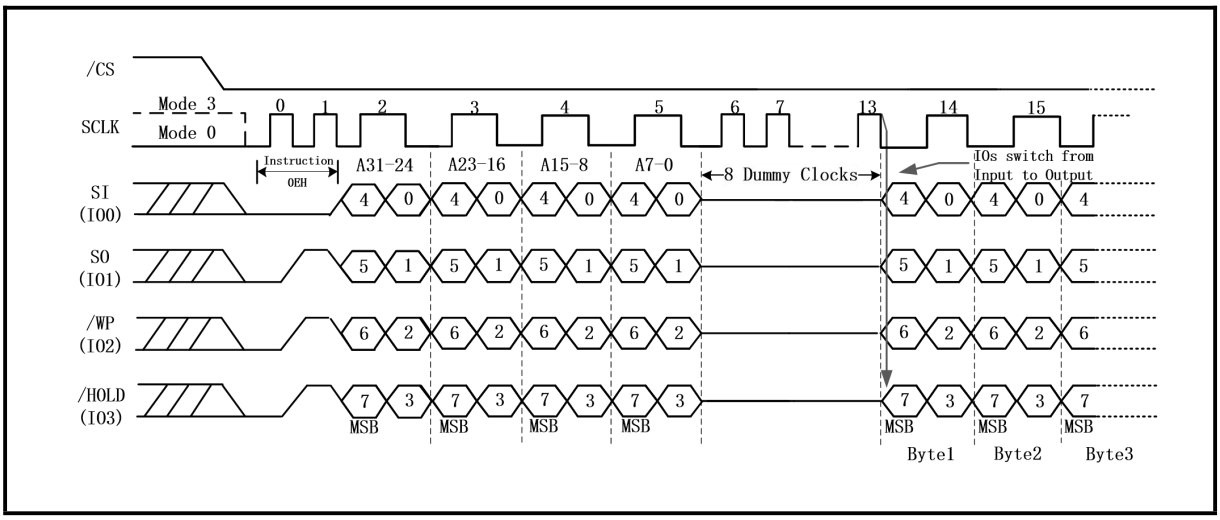


Figure 101. DTR Burst Read with Wrap (QPI Mode only/4-Byte Address Mode)



7.3 ID and Security Instructions

7.3.1 Read Manufacture ID/ Device ID (90H)

See ***Figure 102-Figure 103***, The Read Manufacturer/Device ID instruction is an alternative to the Release from Power-Down/Device ID instruction that provides both the JEDEC assigned Manufacturer ID and the specific Device ID.

The instruction is initiated by driving the /CS pin low and shifting the instruction code “90H” followed by a 24-bit address (A23-A0) of 000000H, regardless of the 3-byte or 4-byte Address Mode. If the 24-bit address is initially set to 000001H, the Device ID will be read first.

Figure 102. Read Manufacture ID/ Device ID Sequence Diagram (SPI Mode)

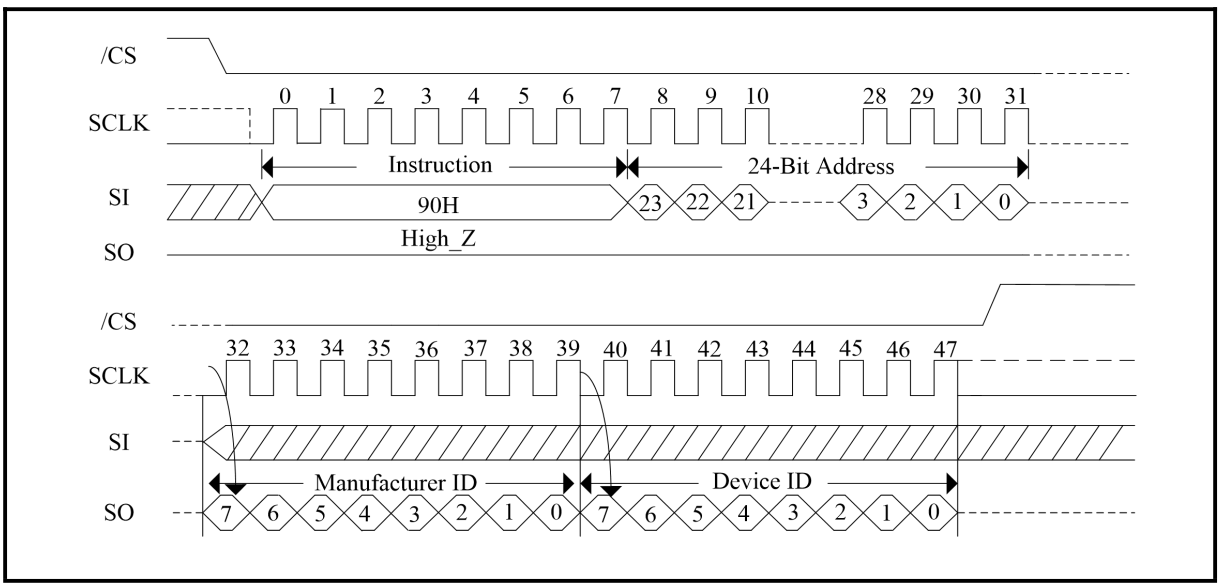
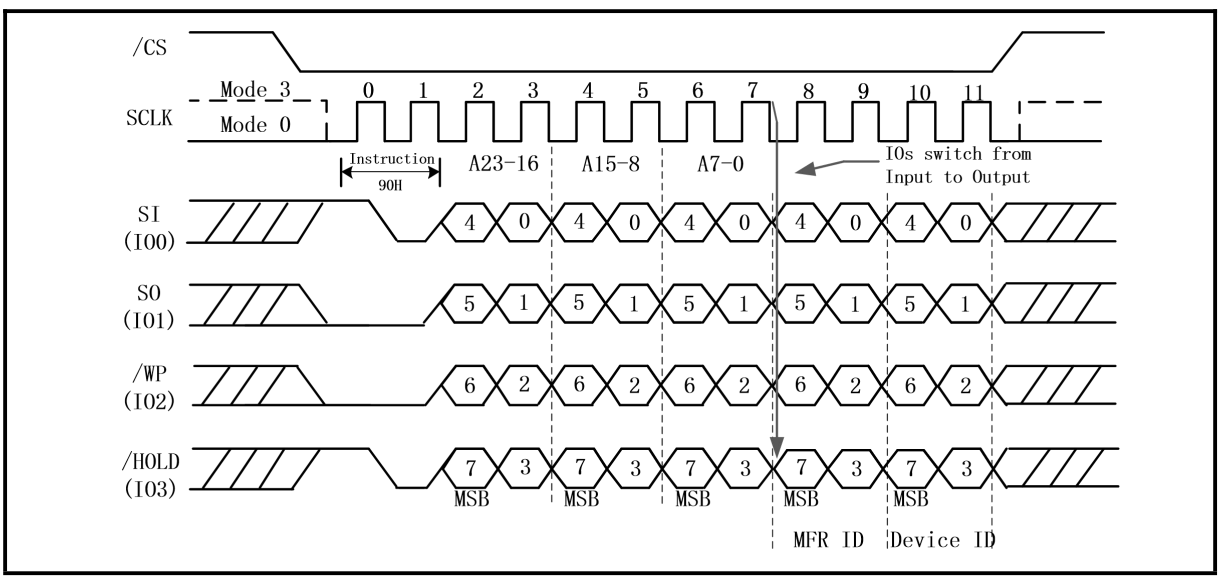


Figure 103. Read Manufacture ID/ Device ID Sequence Diagram (QPI Mode)



7.3.2 Dual I/O Read Manufacture ID/ Device ID (92H)

See ***Figure 104-Figure 105***, the Dual I/O Read Manufacturer/Device ID instruction is an alternative to the Release from Power-Down/Device ID instruction that provides both the JEDEC assigned Manufacturer ID and the specific Device ID by Dual I/O.

The instruction is initiated by driving the /CS pin low and shifting the instruction code “92H” followed by a 24/32-bit address (A23/31-A0) of 000000/00000000H. If the 24/32-bit address is initially set to 000001/00000001H, the Device ID will be read first.

Figure 104. Dual I/O Read Manufacture ID/ Device ID Sequence Diagram (SPI Mode/3-Byte Address Mode)

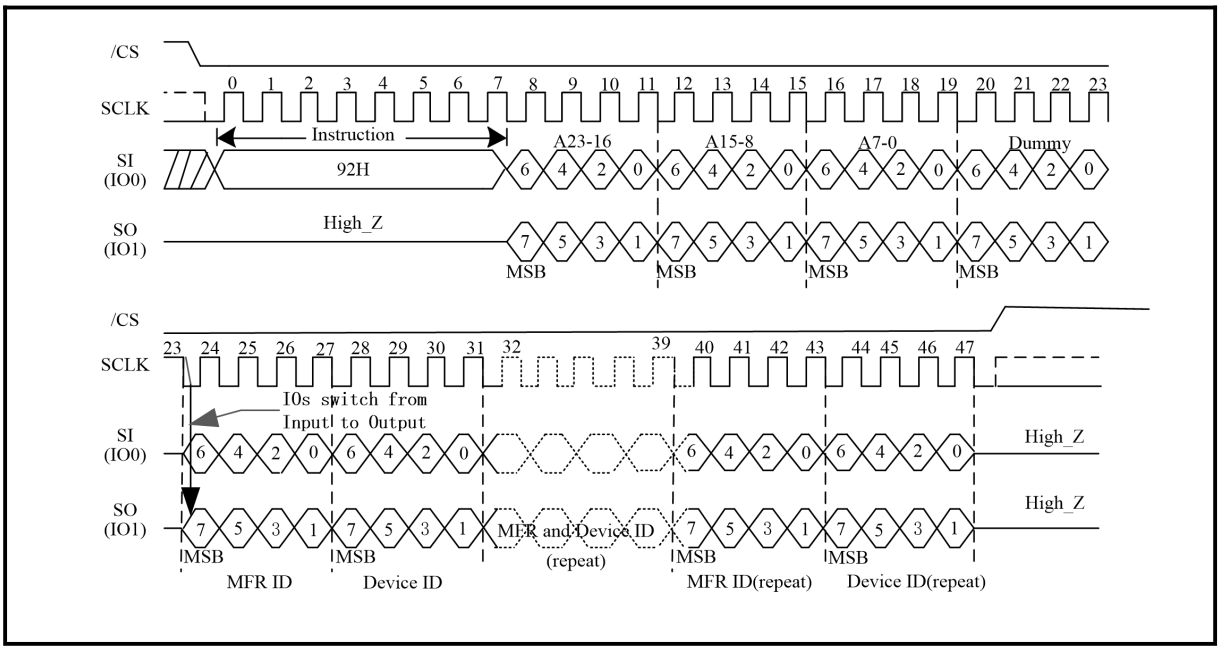
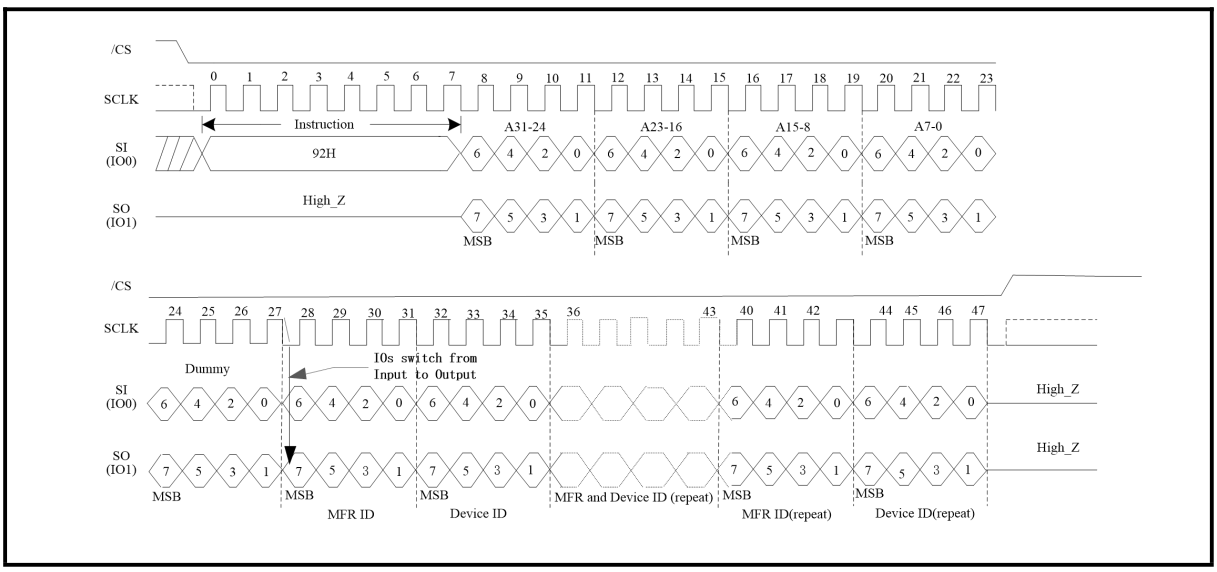


Figure 105. Dual I/O Read Manufacture ID/ Device ID Sequence Diagram (SPI Mode/4-Byte Address Mode)



7.3.3 Quad I/O Read Manufacture ID/ Device ID (94H)

See ***Figure 106-Figure 107***, the Quad I/O Read Manufacturer/Device ID instruction is an alternative to the Release from Power-Down/Device ID instruction that provides both the JEDEC assigned Manufacturer ID and the specific Device ID by quad I/O. The Quad Enable bit (QE) of Status Register must be set to enable.

The instruction is initiated by driving the /CS pin low and shifting the instruction code “94H” followed by a 24/32-bit address (A23/31-A0) of 000000H and 6 dummy clocks. If the 24/32-bit address is initially set to 000001/00000001H, the Device ID will be read first.

Figure 106. Quad I/O Read Manufacture ID/ Device ID Sequence Diagram (SPI Mode/3-Byte Address Mode)

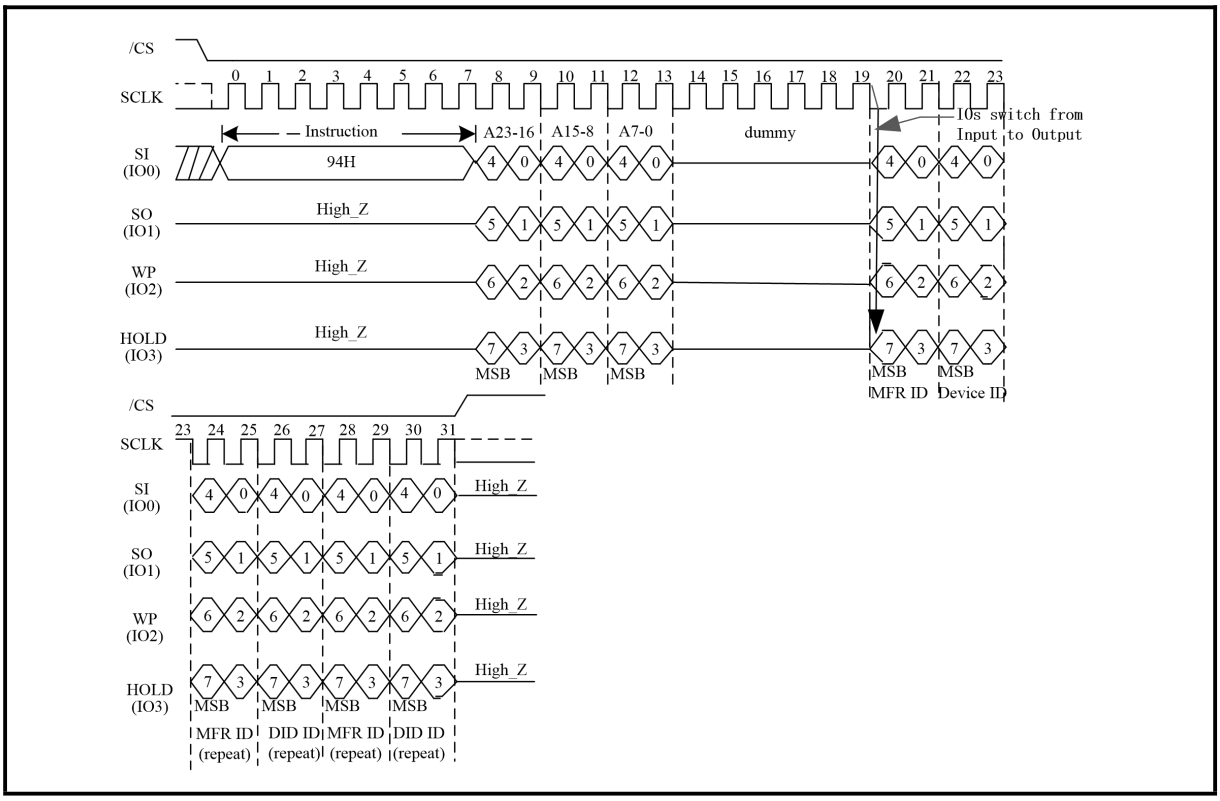
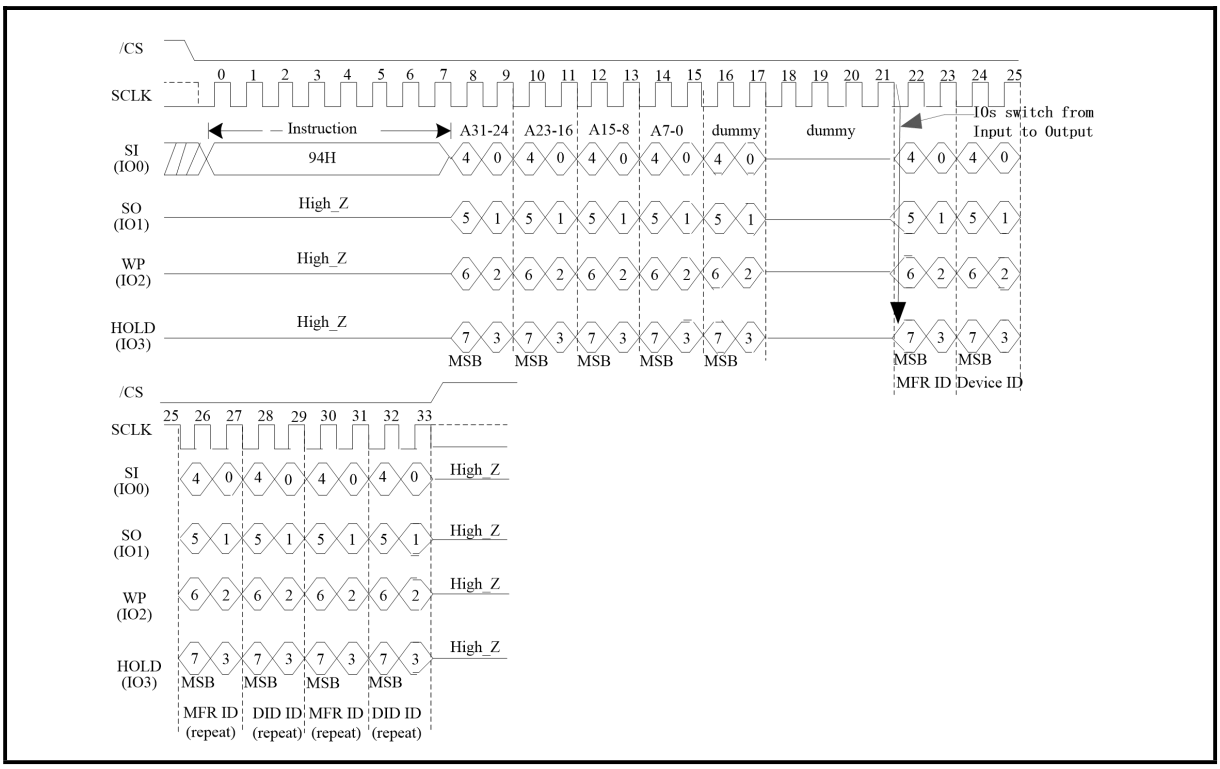


Figure 107. Quad I/O Read Manufacture ID/ Device ID Sequence Diagram (SPI Mode/3-Byte Address Mode)



7.3.4 Read JEDEC ID (9FH)

The JEDEC ID instruction allows the 8-bit manufacturer identification to be read, followed by two bytes of device identification. The device identification indicates the memory type in the first byte, and the memory capacity of the device in the second byte. JEDEC ID instruction while an Erase or Program cycle is in progress, is not decoded, and has no effect on the cycle that is in progress. The JEDEC ID instruction should not be issued while the device is in Deep Power-Down Mode.

See ***Figure 108-Figure 109***, the device is first selected by driving /CS to low. Then, the 8-bit instruction code for the instruction is shifted in. This is followed by the 24-bit device identification, stored in the memory, being shifted out on Serial Data Output, each bit being shifted out during the falling edge of Serial Clock. The JEDEC ID instruction is terminated by driving /CS to high at any time during data output. When /CS is driven high, the device is put in the Standby Mode. Once in the Standby Mode, the device waits to be selected, so that it can receive, decode and execute instructions.

Figure 108. JEDEC ID Sequence Diagram (SPI Mode)

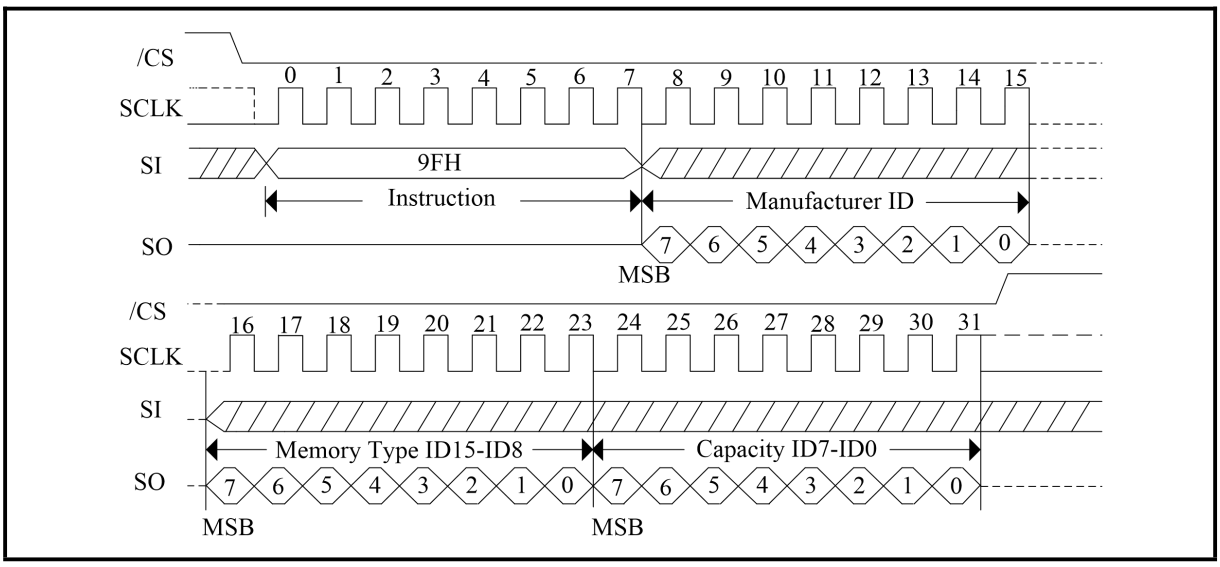
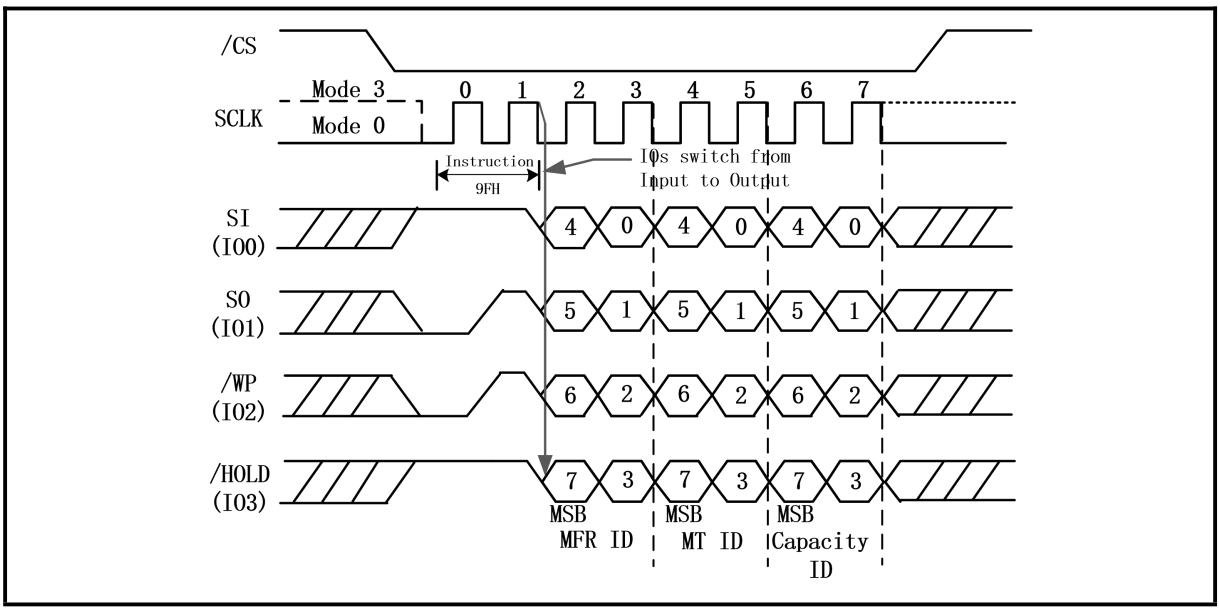


Figure 109. JEDEC ID Sequence Diagram (QPI Mode)



7.3.5 Read Unique ID Number (4Bh)

The Read Unique ID Number instruction accesses a factory-set read-only 128-bit number that is unique to each BY25Q256FS device. The ID number can be used in conjunction with user software methods to help prevent copying or cloning of a system. The Read Unique ID instruction is initiated by driving the /CS pin low and shifting the instruction code “4Bh” followed by four or five bytes of dummy clocks in SPI mode. In QPI mode, it contains 3/4 bytes dummy and some dummy that can be configured by the “Set Read Parameters (C0h)” instruction. After which, the 128-bit ID is shifted out on the falling edge of SCLK as

Figure 110. Read Unique ID Sequence Diagram (SPI Mode/3-Byte Address Mode)

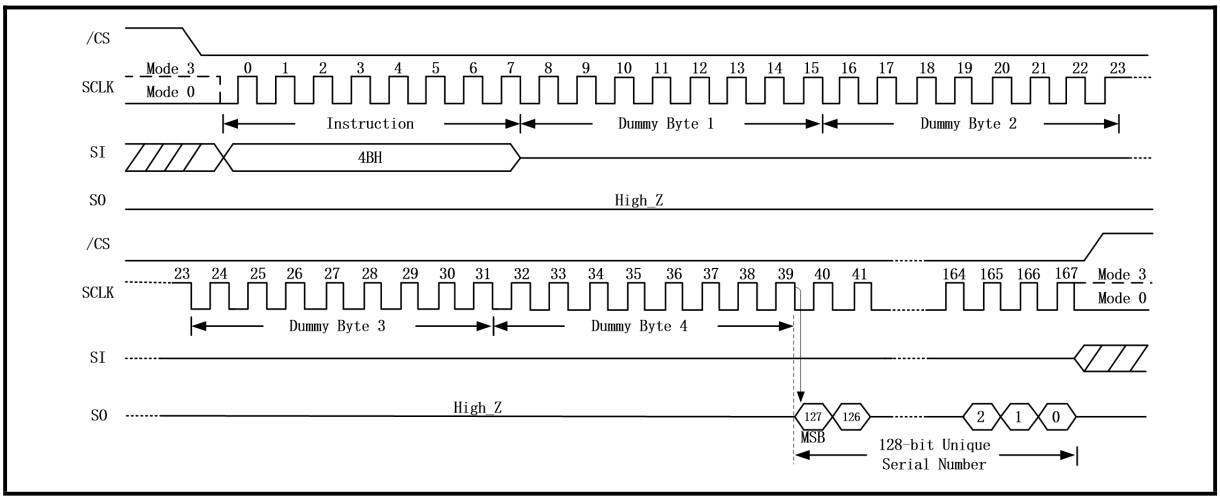


Figure 111. Read Unique ID Sequence Diagram (SPI Mode/4-Byte Address Mode)

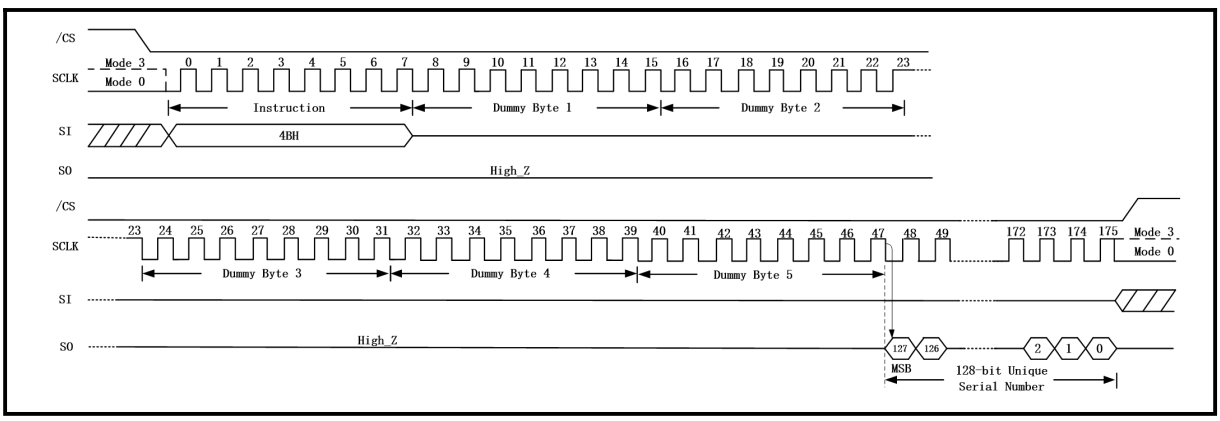


Figure 112. Read Unique ID Sequence Diagram (QPI Mode/3-Byte Address Mode)

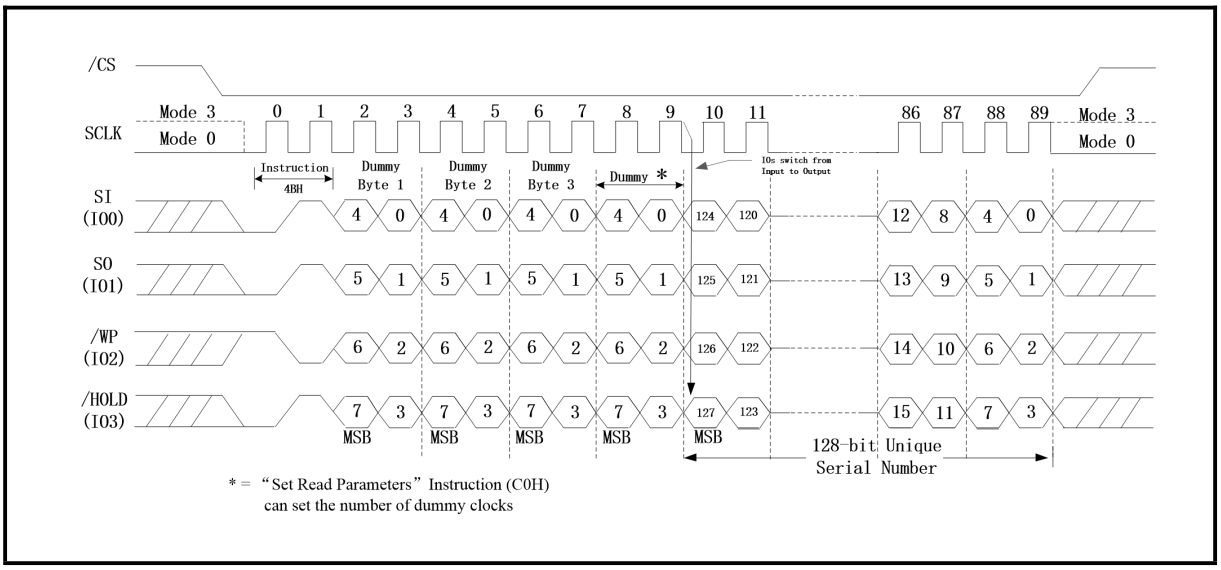
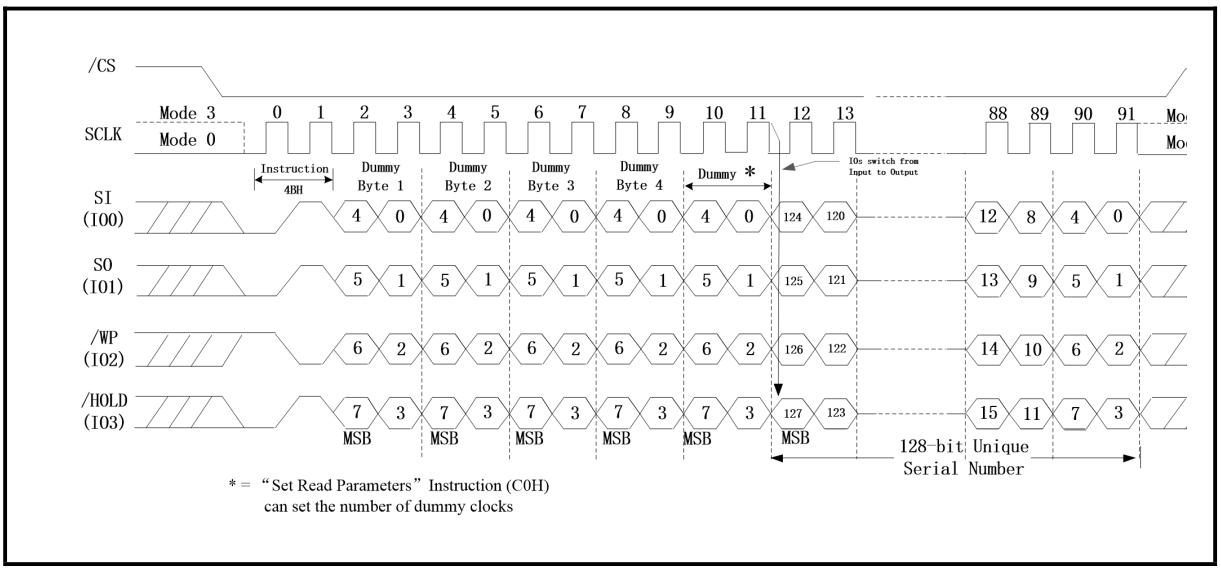


Figure 113. Read Unique ID Sequence Diagram (QPI Mode/4-Byte Address Mode)



7.3.6 Deep Power-Down (B9H)

Although the standby current during normal operation is relatively low, standby current can be further reduced with the Deep Power-down instruction. The lower power consumption makes the Deep Power-down (DPD) instruction especially useful for battery powered applications (*see ICC1 and ICC2*). The instruction is initiated by driving the /CS pin low and shifting the instruction code "B9h" as shown in ***Figure 114-Figure 115***

The /CS pin must be driven high after the eighth bit has been latched. If this is not done the Deep Power down instruction will not be executed. After /CS is driven high, the power-down state will entered within the time duration of tDP. While in the power-down state only the Release from Deep Power-down/Device ID instruction, software reset sequence or hardware reset sequence, which restores the device to normal operation, will be recognized. All other Instructions are ignored. This includes the Read Status Register instruction, which is always available during normal operation. Ignoring all but one instruction also makes the Power Down state a useful condition for securing maximum write protection. The device always powers-up in the normal operation with the standby current of ICC1.

Figure 114. Deep Power-Down Sequence Diagram (SPI Mode)

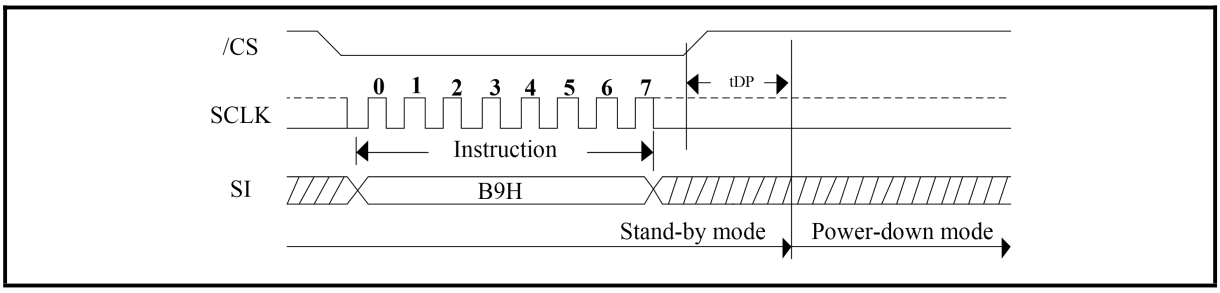
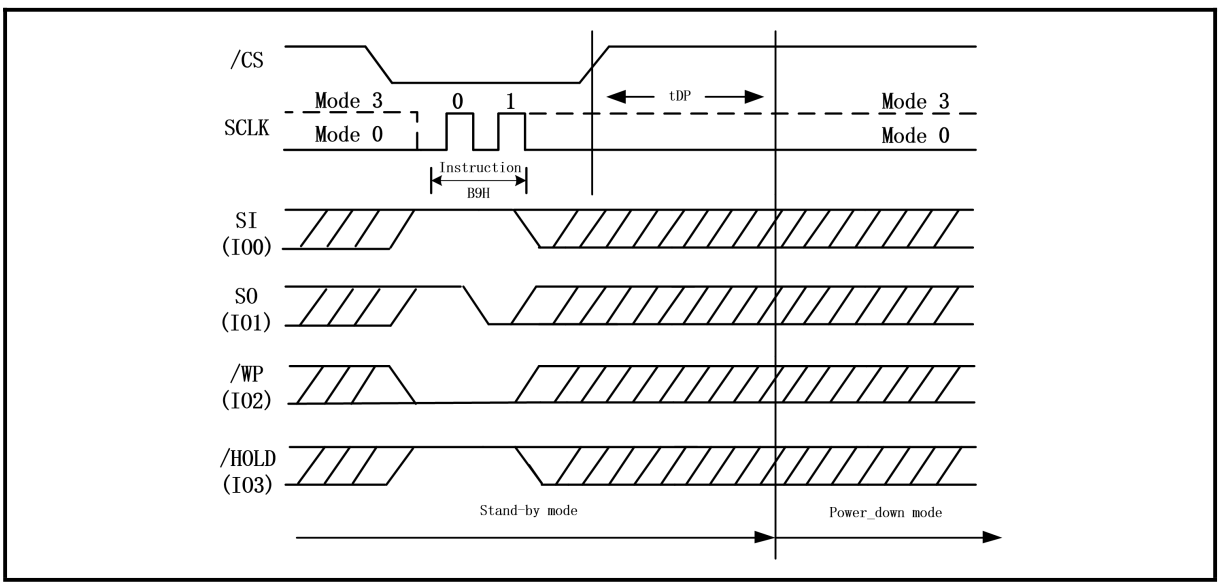


Figure 115. Deep Power-Down Sequence Diagram (QPI Mode)



7.3.7 Release from Deep Power-Down/Read Device ID (ABH)

The Release from Power-Down or Device ID instruction is a multi-purpose instruction. It can be used to release the device from the Power-Down state or obtain the devices electronic identification (ID) number.

See ***Figure 116-Figure 117***, to release the device from the Power-Down state, the instruction is issued by driving the /CS pin low, shifting the instruction code "ABH" and driving /CS high Release from Power-Down will take the time duration of tRES1 (See *AC Characteristics*) before the device will resume normal operation and other instruction are accepted. The /CS pin must remain high during the tRES1 time duration.

When used only to obtain the Device ID while not in the Power-Down state, the instruction is initiated by driving the /CS pin low and shifting the instruction code "ABH" followed by 3-dummy byte. The Device ID bits are then shifted out on the falling edge of SCLK with most significant bit (MSB) first as shown in ***Figure 118-Figure 119***. The Device ID value for the BY25QM1GFS is listed in Manufacturer and Device Identification table. The Device ID can be read continuously. The instruction is completed by driving /CS high.

When used to release the device from the Power-Down state and obtain the Device ID, the instruction is the same as previously described, and shown in ***Figure 118-Figure 119***, except that after /CS is driven high it must remain high for a time duration of tRES2 (See *AC Characteristics*). After this time duration the device will resume normal operation and other instruction will be accepted. If the Release from Power-Down/Device ID instruction is issued while an Erase, Program or Write cycle is in process (when WIP equal 1) the instruction is ignored and will not have any effects on the current cycle.

Figure 116. Release Power-Down Sequence Diagram (SPI Mode)

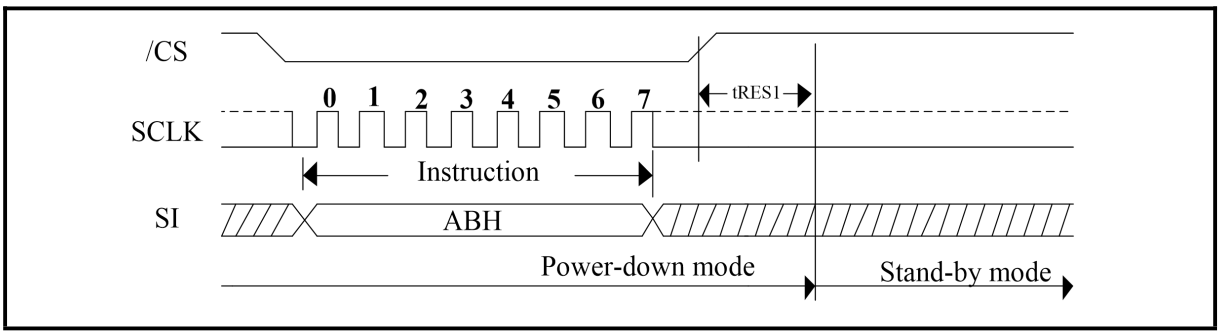


Figure 117. Release Power-Down Sequence Diagram (QPI Mode)

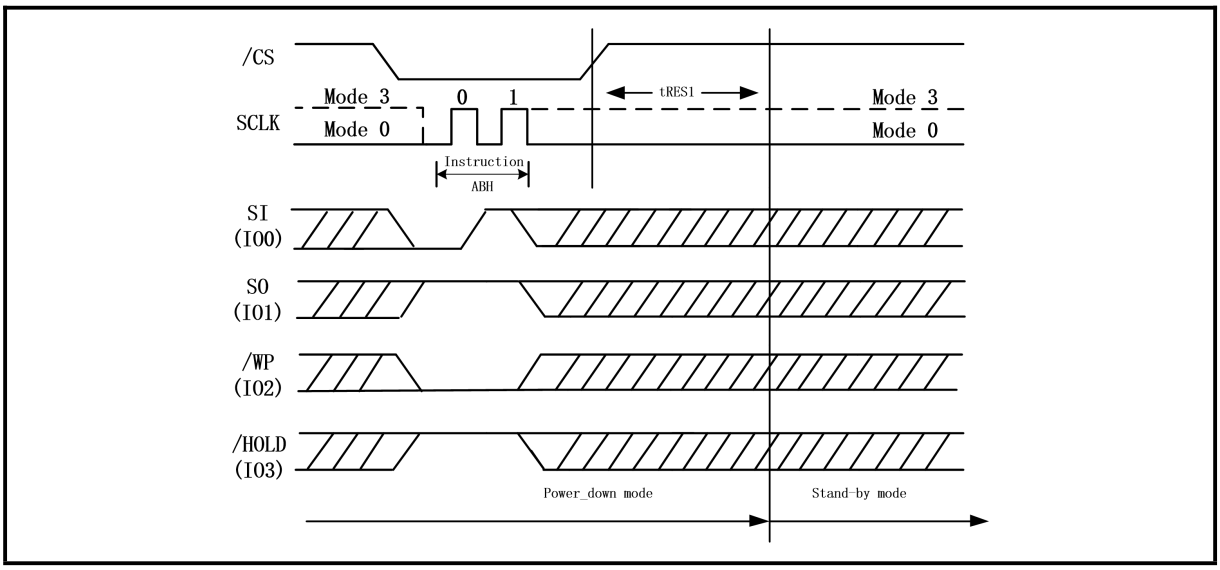


Figure 118. Release Power-Down/Read Device ID Sequence Diagram (SPI Mode)

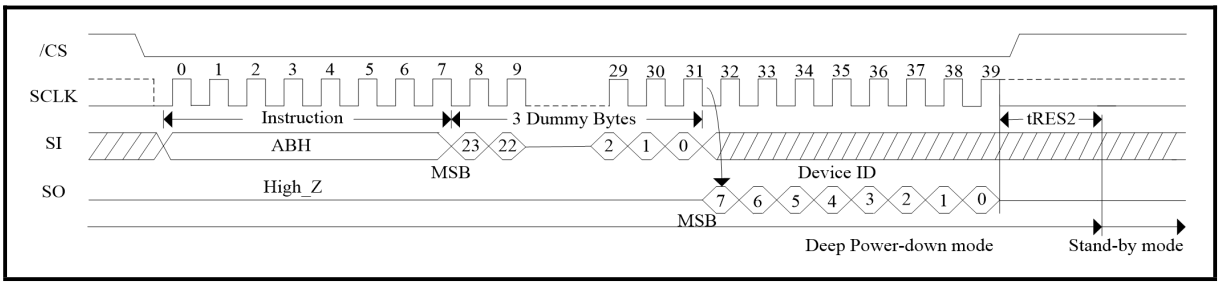
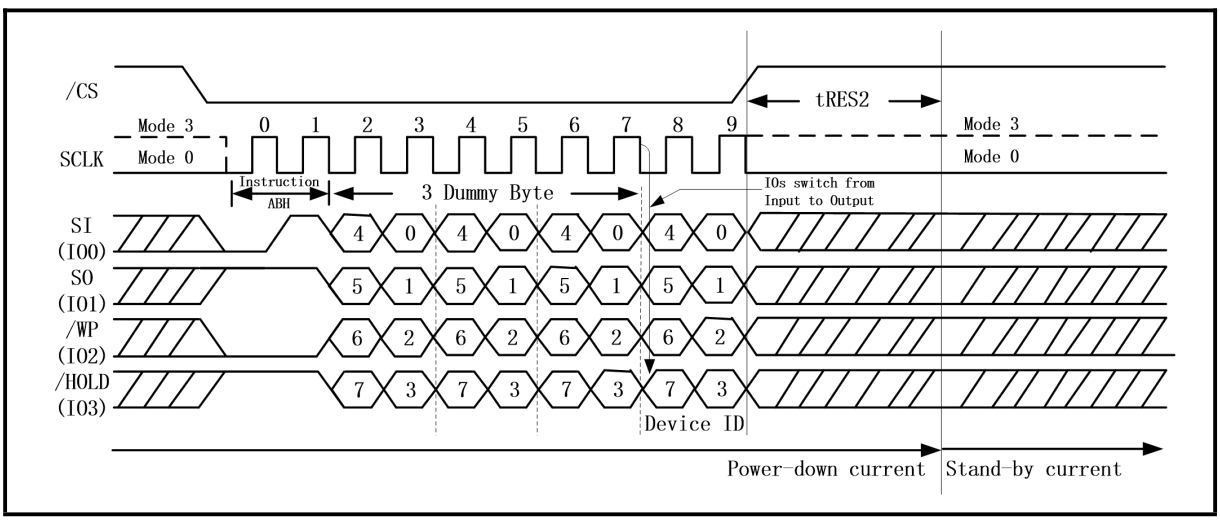


Figure 119. Release Power-Down/Read Device ID Sequence Diagram (QPI Mode)



7.3.8 Read Security Registers (48H)

See ***Figure 120-Figure 123***, the instruction is followed by a 3/4-byte address (A23/31-A0) and the dummy byte. In QPI mode, the number of dummy can be configured by the “C0h” instruction. Each bit being latched-in during the rising edge of SCLK. Then the memory content, at that address, is shifted out on SO, each bit being shifted out, at a Max frequency fC, during the falling edge of SCLK. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. Once the A8-A0 address reaches the last byte of the register (Byte FFH), it will reset to 000H, the instruction is completed by driving /CS high.

ADDRESS	A23/31-A16	A15-12	A11-9	A8-0
Security Register #1	00H/0000H	0 0 0 1	0 0 0	Byte Address
Security Register #2	00H/0000H	0 0 1 0	0 0 0	Byte Address
Security Register #3	00H/0000H	0 0 1 1	0 0 0	Byte Address

Figure 120. Read Security Registers instruction Sequence Diagram (SPI Mode/3-Byte Address Mode)

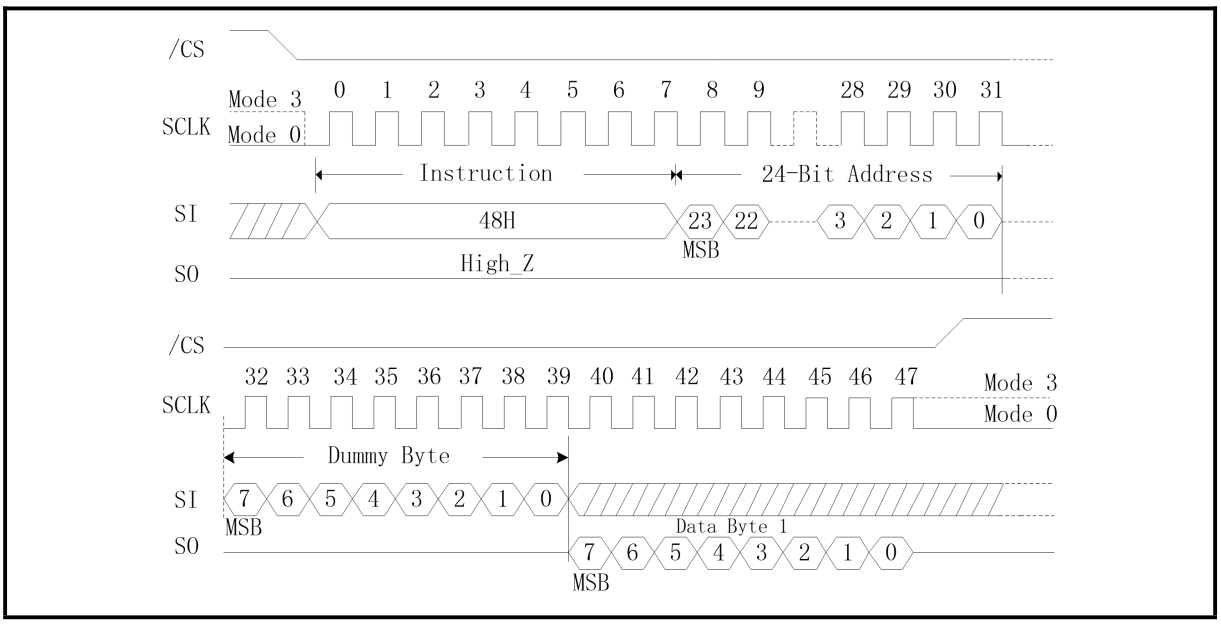


Figure 121. Read Security Registers instruction Sequence Diagram (SPI Mode/4-Byte Address Mode)

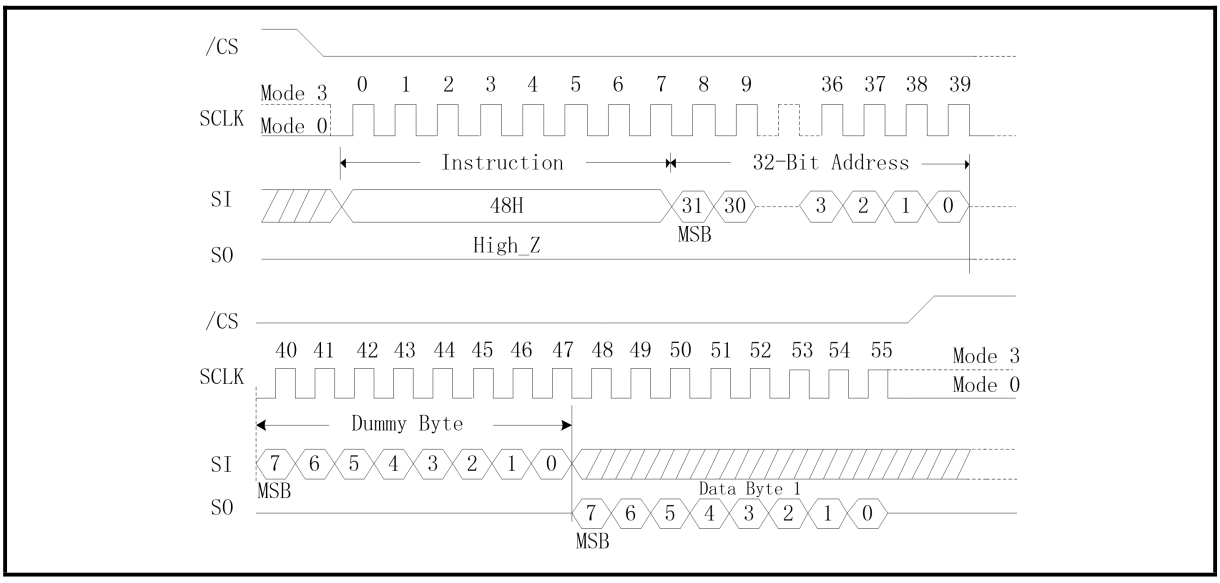


Figure 122. Read Security Registers instruction Sequence Diagram (QPI Mode/3-Byte Address Mode)

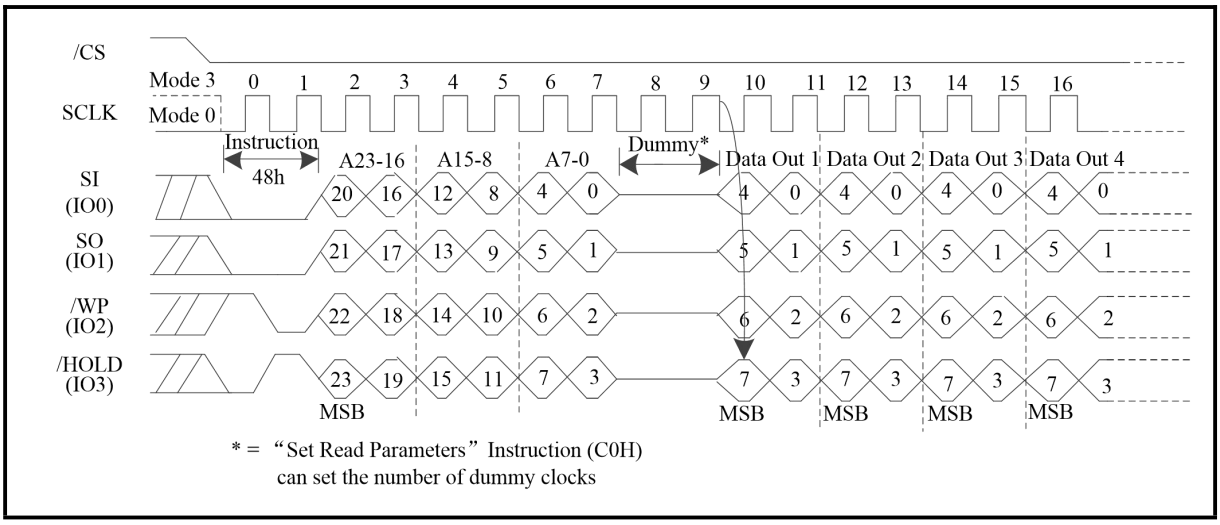
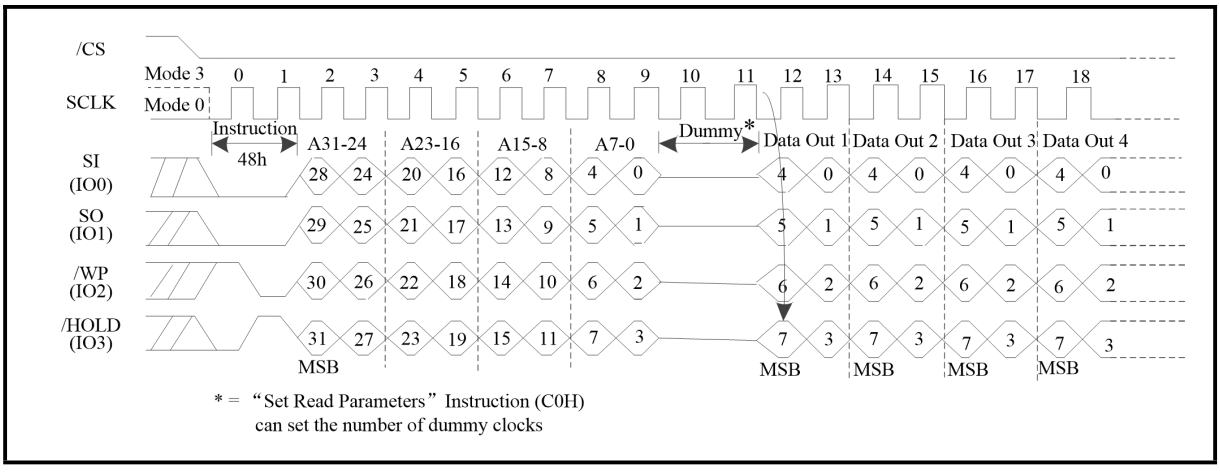


Figure 123. Read Security Registers instruction Sequence Diagram (QPI Mode/4-Byte Address Mode)



7.3.9 Erase Security Registers (44H)

The Single Die BY25Q256FS provides three 512-byte Security Registers which can be erased and programmed individually. These registers may be used by the system manufacturers to store security and other important information separately from the main memory array.

See ***Figure 124-Figure 127***, the Erase Security Registers instruction is similar to Block/Sector Erase instruction. A Write Enable instruction must previously have been executed to set the Write Enable Latch bit.

The Erase Security Registers instruction sequence: /CS goes low sending Erase Security Registers instruction /CS goes high. /CS must be driven high after the eighth bit of the instruction code has been latched in otherwise the Erase Security Registers instruction is not executed. As soon as /CS is driven high, the self-timed Erase Security Registers cycle (whose duration is tSE) is initiated. While the Erase Security Registers cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Erase Security Registers cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch bit is reset. The Security Registers Lock Bit (LB) in the Status Register can be used to OTP protect the security registers. Once the LB bit is set to 1, the Security Registers will be permanently locked; the Erase Security Registers instruction will be ignored.

ADDRESS	A23/31-A16	A15-12	A11-9	A8-0
Security Register #1	00H/0000H	0 0 0 1	0 0 0	Byte Address
Security Register #2	00H/0000H	0 0 1 0	0 0 0	Byte Address
Security Register #3	00H/0000H	0 0 1 1	0 0 0	Byte Address

Figure 124. Erase Security Registers instruction Sequence Diagram (SPI Mode/3-Byte Address Mode)

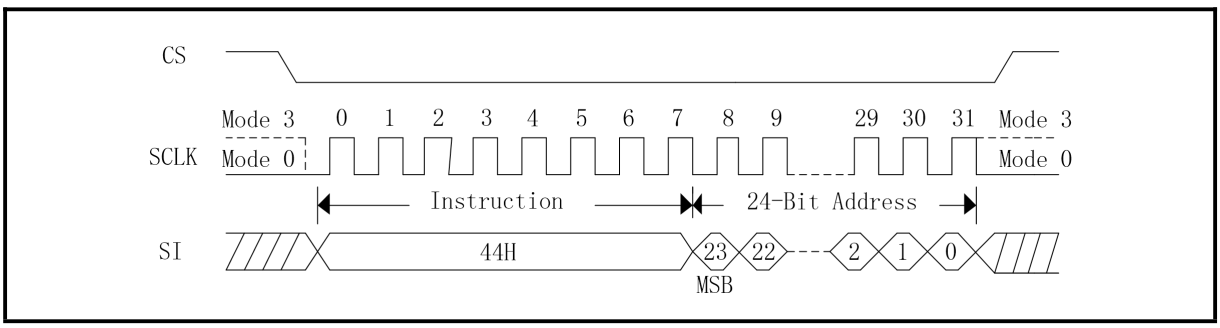


Figure 125. Erase Security Registers instruction Sequence Diagram (SPI Mode/4-Byte Address Mode)

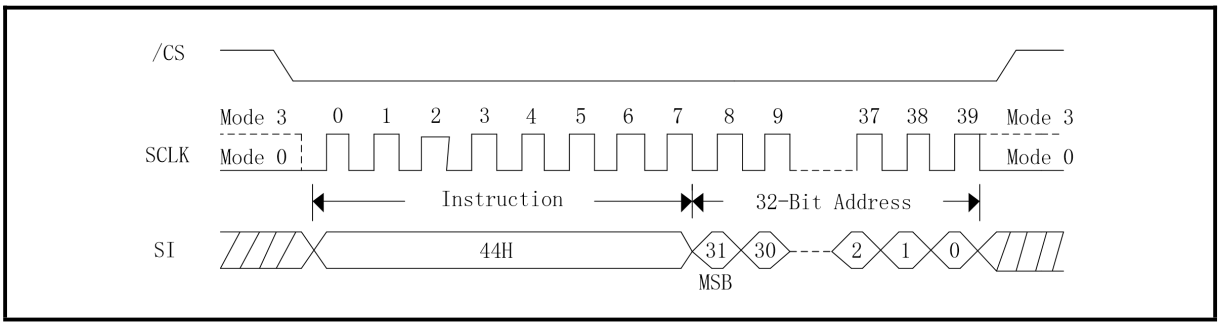


Figure 126. Erase Security Registers instruction Sequence Diagram (QPI Mode/3-Byte Address Mode)

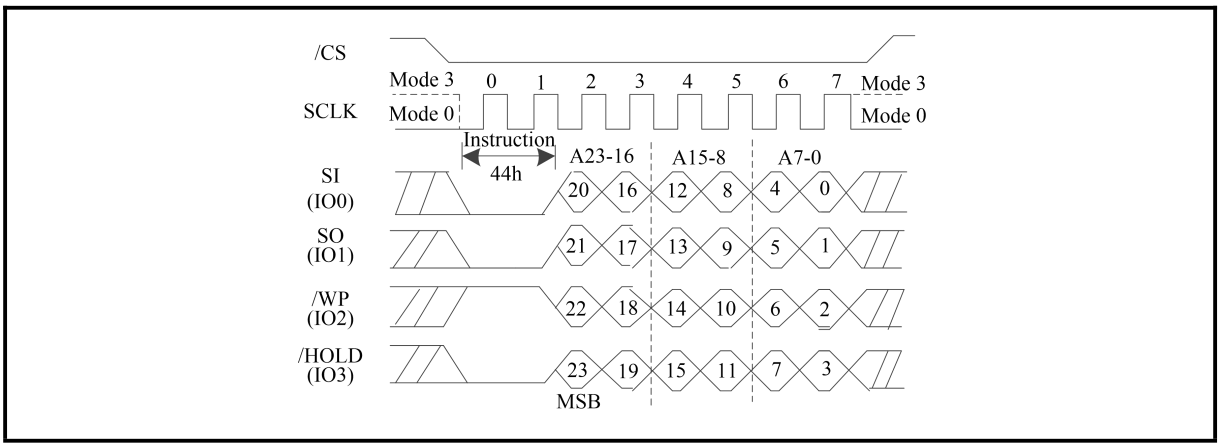
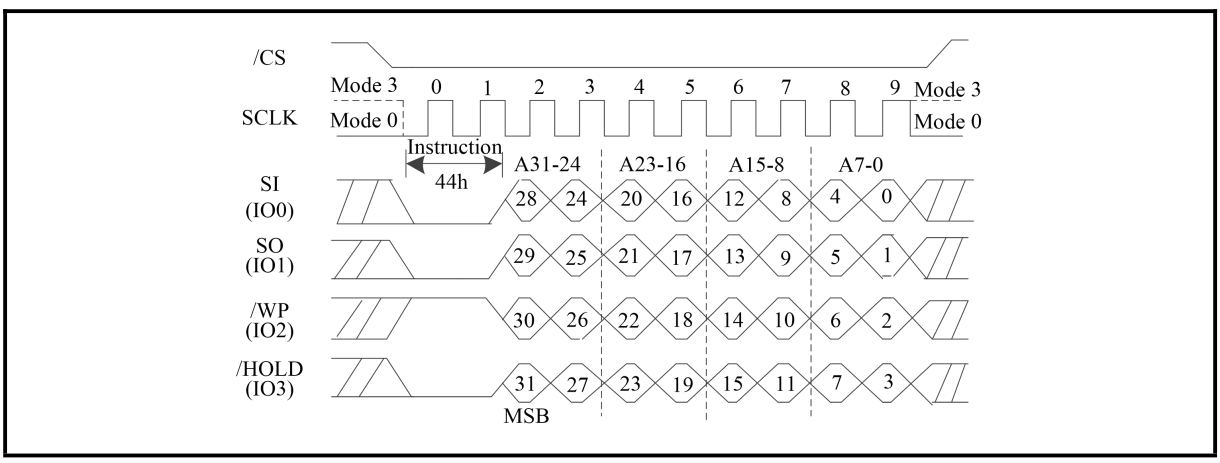


Figure 127. Erase Security Registers instruction Sequence Diagram (QPI Mode/4-Byte Address Mode)



7.3.10 Program Security Registers (42H)

See ***Figure 128-Figure 131***, the Program Security Registers instruction is similar to the Page Program instruction. It allows from one byte to 512 bytes of security register data to be programmed by two times (one time program 256 bytes). A Write Enable instruction must previously have been executed to set the Write Enable Latch bit before sending the Program Security Registers instruction. The Program Security Registers instruction is entered by driving /CS Low, followed by the instruction code (42H), 3/4-byte address and at least one data byte on SI. As soon as /CS is driven high, the self-timed Program Security Registers cycle (whose duration is tPP) is initiated. While the Program Security Registers cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Program Security Registers cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch bit is reset.

If the Security Registers Lock Bit (LB3/LB2/LB1) is set to 1, the Security Registers will be permanently locked. Program Security Registers instruction will be ignored.

ADDRESS	A23/31-A16	A15-12	A11-9	A8-0
Security Register #1	00H/0000H	0 0 0 1	0 0 0	Byte Address
Security Register #2	00H/0000H	0 0 1 0	0 0 0	Byte Address
Security Register #3	00H/0000H	0 0 1 1	0 0 0	Byte Address

Figure 128. Program Security Registers instruction Sequence Diagram (SPI Mode/3-Byte Address Mode)

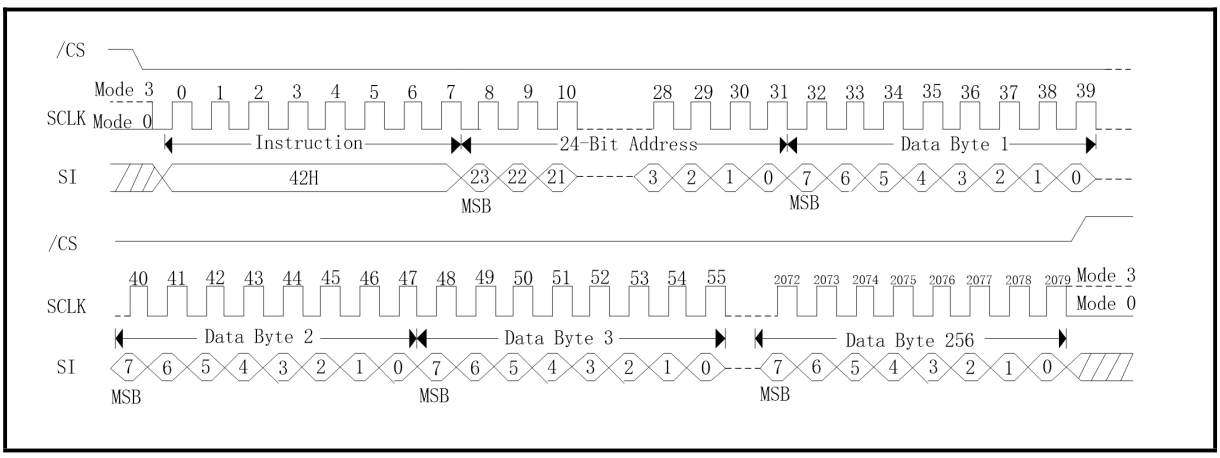


Figure 129. Program Security Registers instruction Sequence Diagram (SPI Mode/4-Byte Address Mode)

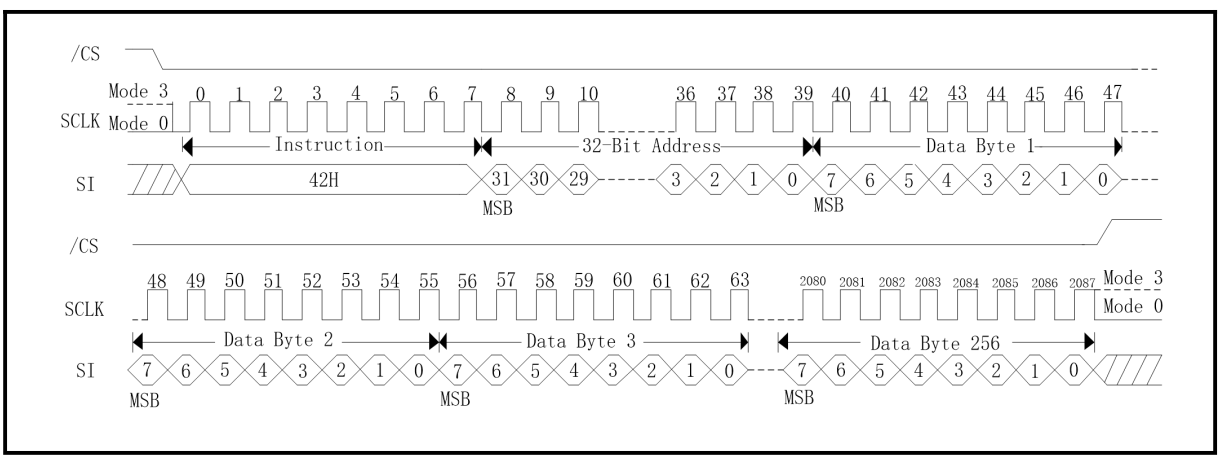


Figure 130. Program Security Registers instruction Sequence Diagram (QPI Mode/3-Byte Address Mode)

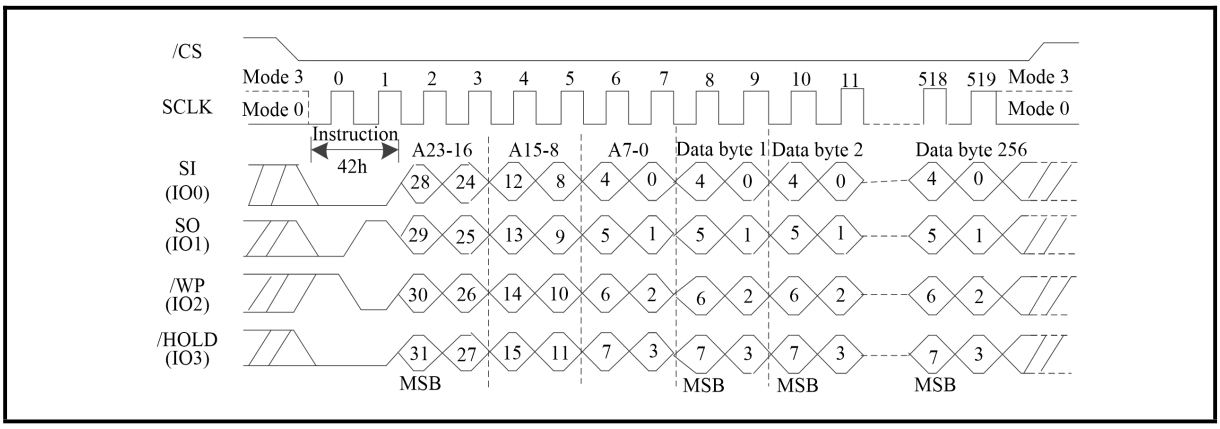
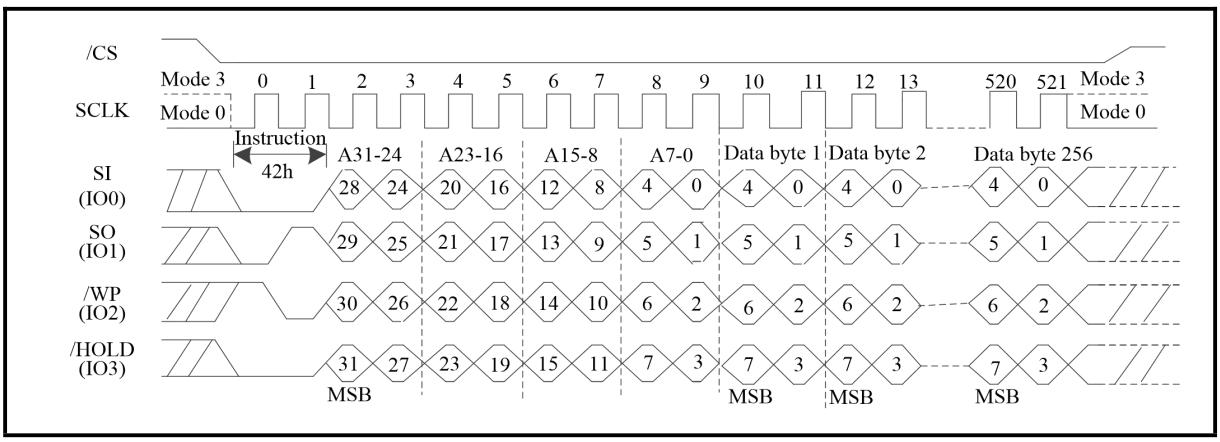


Figure 131. Program Security Registers instruction Sequence Diagram (QPI Mode/4-Byte Address Mode)



7.3.11 Read Serial Flash Discoverable Parameter (5AH)

See ***Figure 132-Figure 133,***The Serial Flash Discoverable Parameter (SFDP) standard provides a consistent method of describing the functional and feature capabilities of serial flash devices in a standard set of internal parameter tables. These parameter tables can be interrogated by host system software to enable adjustments needed to accommodate divergent features from multiple vendors. The concept is similar to the one found in the Introduction of JEDEC Standard, JESD68 on CFI. SFDP is a standard of JEDEC Standard No.216.

The Read SFDP instruction is initiated by driving the /CS pin low and shifting the instruction code “5Ah” followed by a 24-bit address (A23-A0) into the SI pin, regardless of the 3-byte or 4-byte Address Mode. Eight “dummy” clocks are also required in SPI mode. In QPI mode，the number of dummy clocks can be configured by the “Set Read Parameters (C0h)” instruction.

Figure 132. Read Serial Flash Discoverable Parameter instruction Sequence Diagram (SPI Mode)

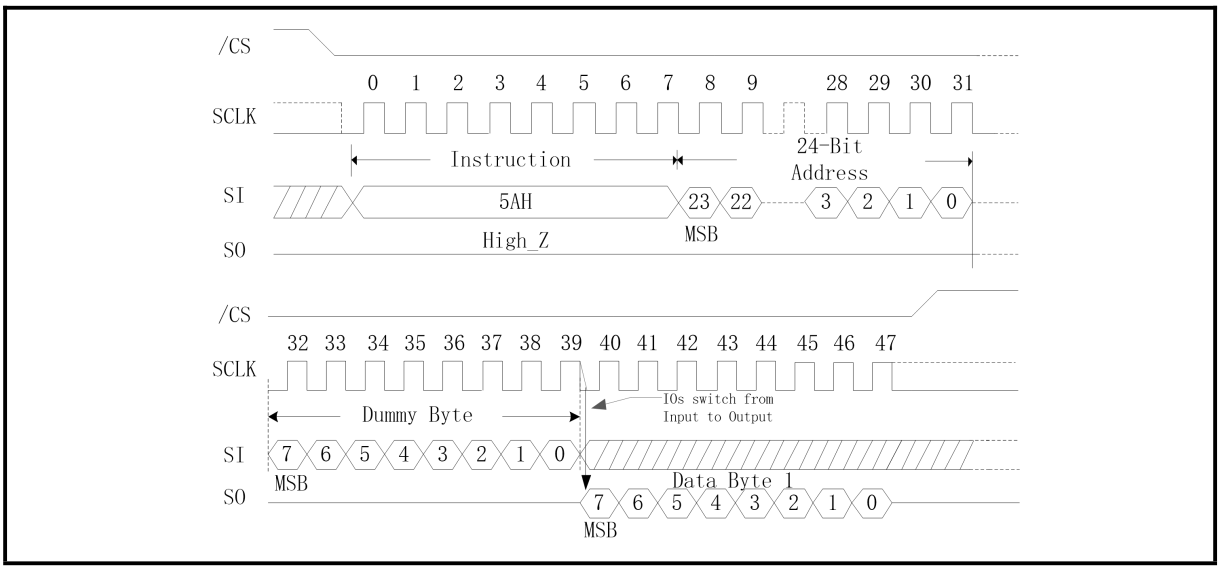
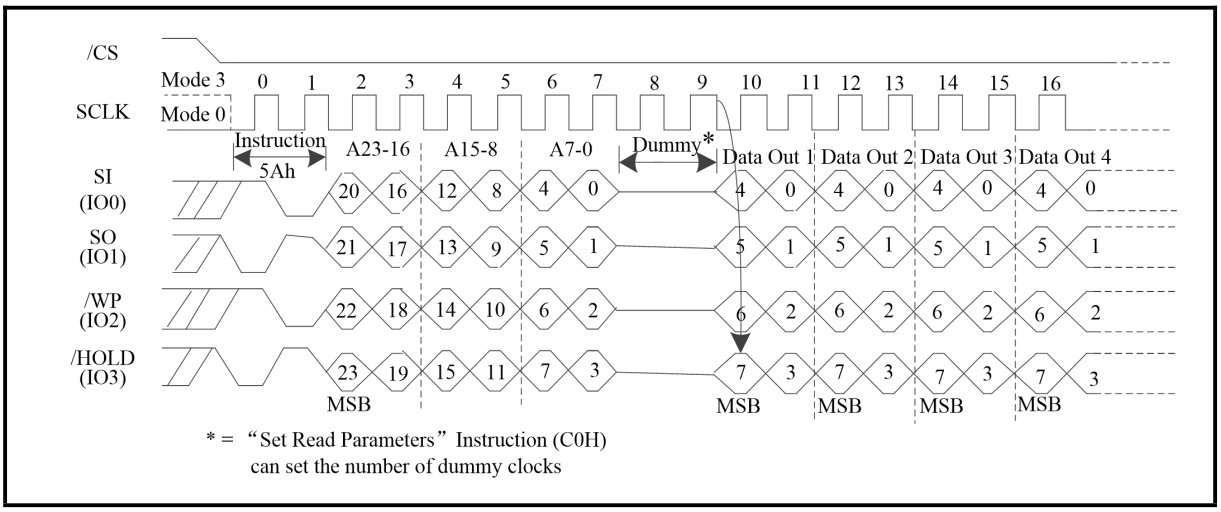


Figure 133. Read Serial Flash Discoverable Parameter instruction Sequence Diagram (QPI Mode)



7.4 Program and Erase Instructions

7.4.1 Page Program (02H)

The Page Program instruction is for programming the memory. A Write Enable instruction must previously have been executed to set the Write Enable Latch bit before sending the Page Program instruction.

See ***Figure 134-Figure 137***, the Page Program instruction is entered by driving /CS Low, followed by the instruction code, 3-byte address and at least one data byte on SI. If the 8 least significant address bits (A7-A0) are not all zero, all transmitted data that goes beyond the end of the current page are programmed from the start address of the same page (from the address whose 8 least significant bits (A7-A0) are all zero). /CS must be driven low for the entire duration of the sequence. The Page Program instruction sequence: /CS goes low-> sending Page Program instruction ->3-byte/4-byte address on SI ->at least 1 byte data on SI-> /CS goes high.

If more than 256 bytes are sent to the device, previously latched data are discarded and the last 256 data bytes are guaranteed to be programmed correctly within the same page. If less than 256 data bytes are sent to device, they are correctly programmed at the requested addresses without having any effects on the other bytes of the same page. /CS must be driven high after the eighth bit of the last data byte has been latched in; otherwise the Page Program instruction is not executed.

As soon as /CS is driven high, the self-timed Page Program cycle (whose duration is tPP) is initiated. While the Page Program cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Page Program cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch bit is reset.

A Page Program instruction applied to a page which is protected by the Block Protect (BP4, BP3, BP2, BP1, BP0) bits (see ***Table 9-Table 10***)、SPB and DPB are not executed.

Figure 134. Page Program Sequence Diagram (SPI Mode/3-Byte Address Mode)

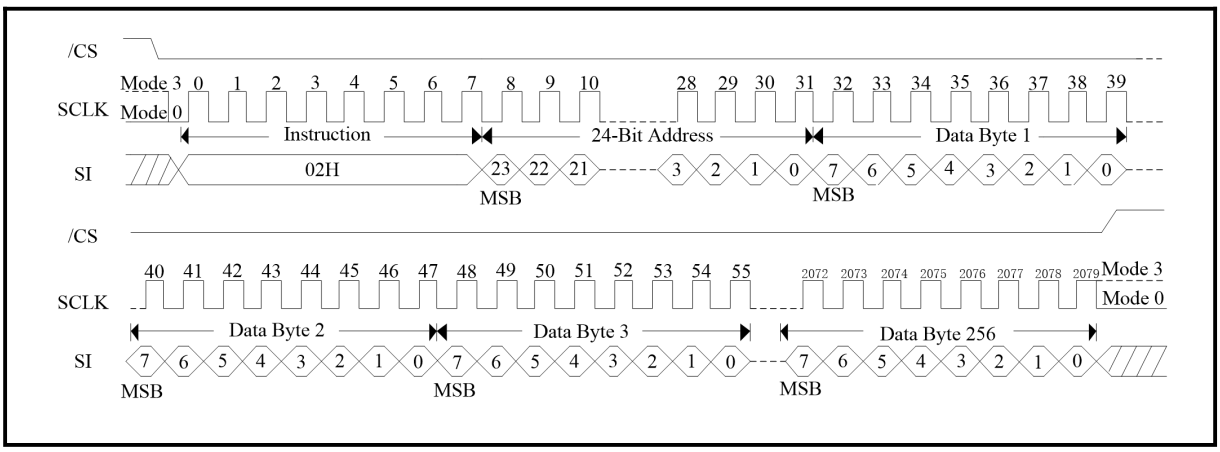


Figure 135. Page Program Sequence Diagram (SPI Mode/4-Byte Address Mode)

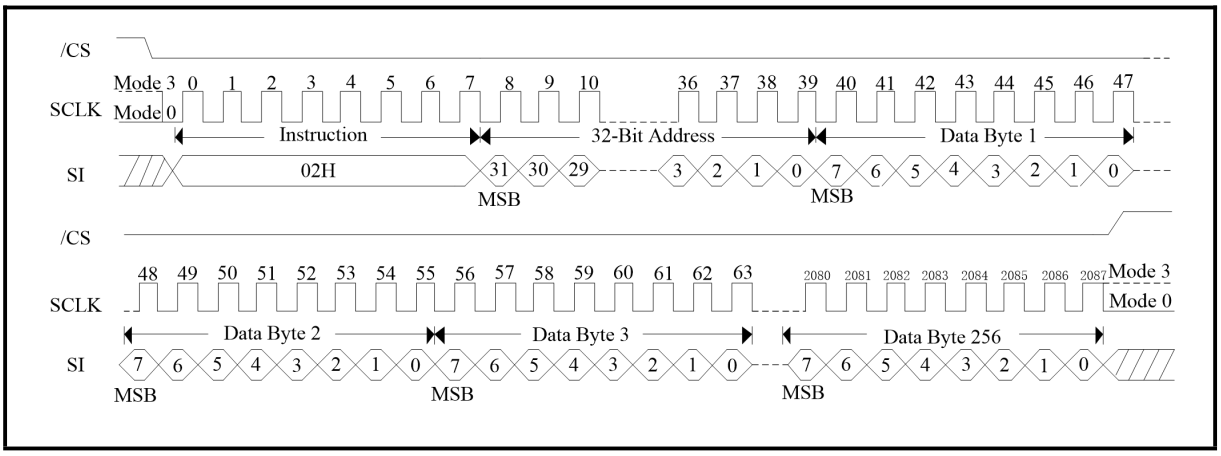


Figure 136. Page Program Sequence Diagram (QPI Mode/3-Byte Address Mode)

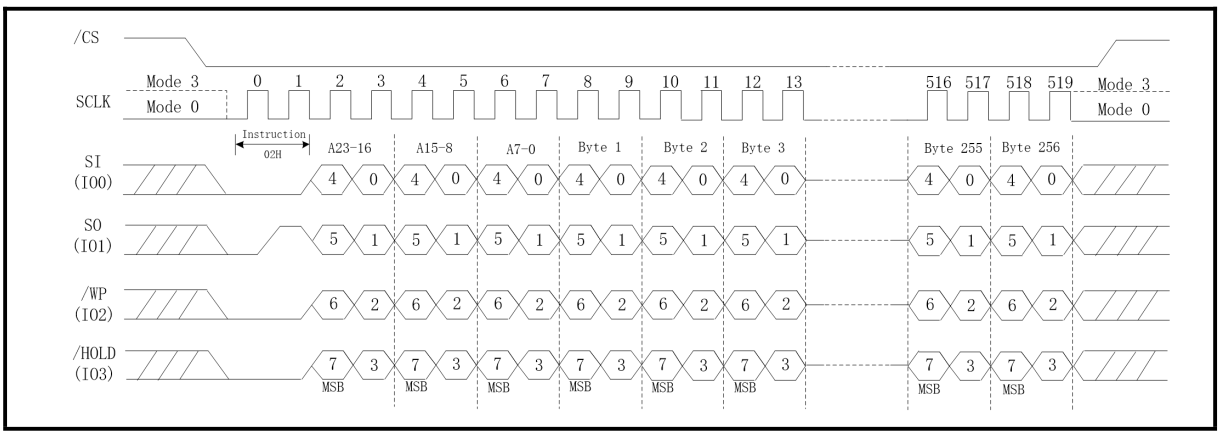
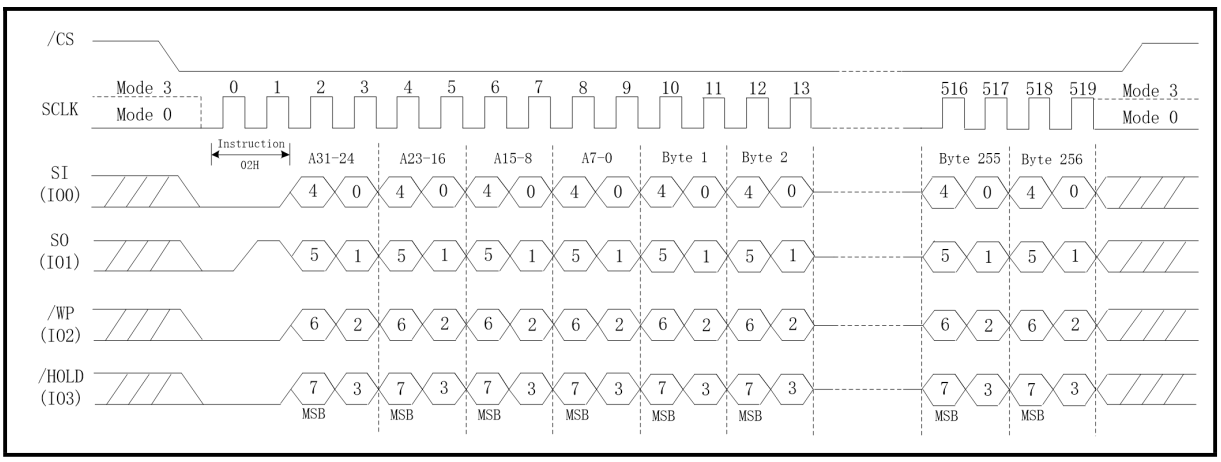


Figure 137. Page Program Sequence Diagram (QPI Mode/4-Byte Address Mode)



7.4.2 Page Program with 4-Byte Address (12H)

The Page Program with 4-Byte Address instruction is similar to the Page Program instruction except that it requires 32-bit address instead of 24-bit address. No matter the device is operating in 3-Byte Address Mode or 4-byte Address Mode, the Page Program with 4-Byte Address instruction will always require 32- bit address to access the entire 256Mb memory.

Figure 138. Page Program with 4-Byte Address (SPI Mode)

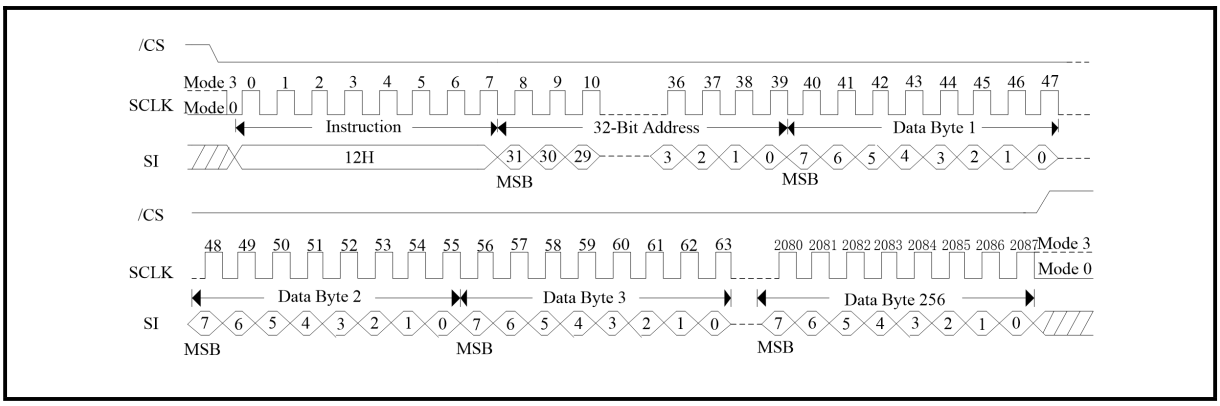
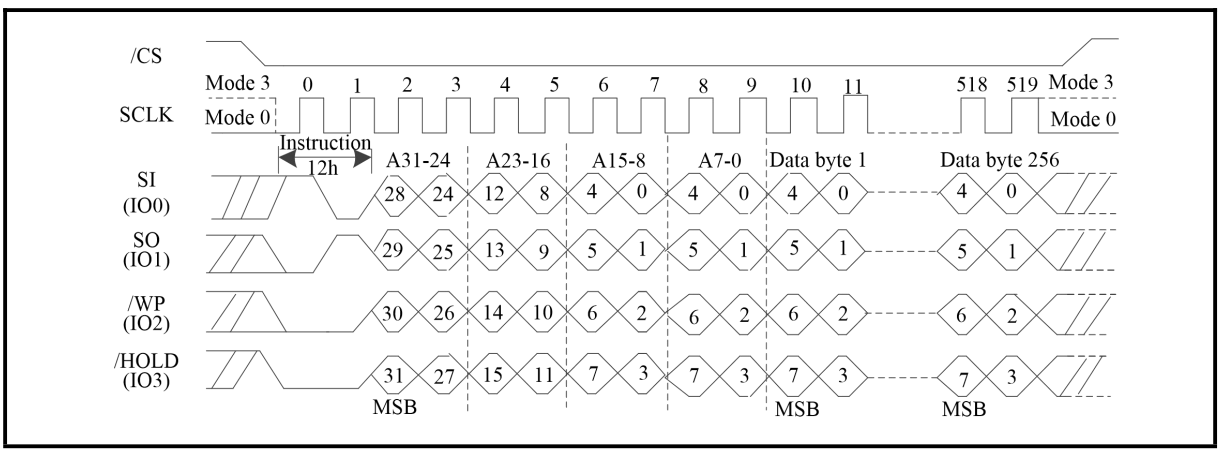


Figure 139. Page Program with 4-Byte Address (QPI Mode)



7.4.3 Quad Page Program (32H)

The Quad Page Program instruction is for programming the memory using for pins: IO0, IO1, IO2 and IO3. To use Quad Page Program the Quad enable in status register Bit9 must be set (QE=1). A Write Enable instruction must previously have been executed to set the Write Enable Latch bit before sending the Page Program instruction. The Quad Page Program instruction is entered by driving /CS Low, followed by the instruction code (32H), three address bytes and at least one data byte on IO pins. The Quad Enable bit (QE) of Status Register must be set to enable.

The instruction sequence is shown in ***Figure 140-Figure 141***. If more than 256 bytes are sent to the device, previously latched data are discarded and the last 256 data bytes are guaranteed to be programmed correctly within the same page. If less than 256 data bytes are sent to device, they are correctly programmed at the requested addresses without having any effects on the other bytes of the same page. /CS must be driven high after the eighth bit of the last data byte has been latched in; otherwise the Quad Page Program instruction is not executed.

As soon as /CS is driven high, the self-timed Quad Page Program cycle (whose duration is tPP) is initiated. While the Quad Page Program cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Quad Page Program cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch bit is reset. A Quad Page Program instruction applied to a page which is protected by the Block Protect (BP4, BP3, BP2, BP1, BP0) bits (see ***Table 9-Table 10***) is not executed

Figure 140. Quad Page Program Sequence Diagram (SPI Mode only/3-Byte Address Mode)

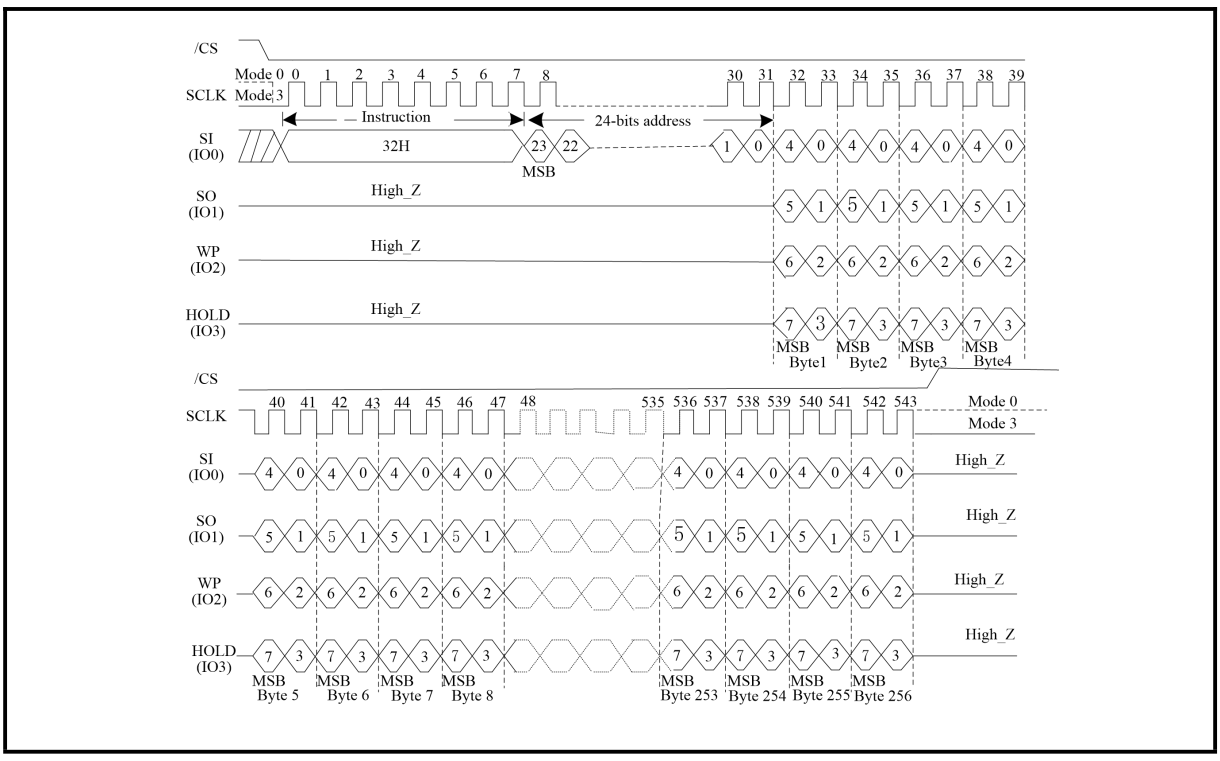
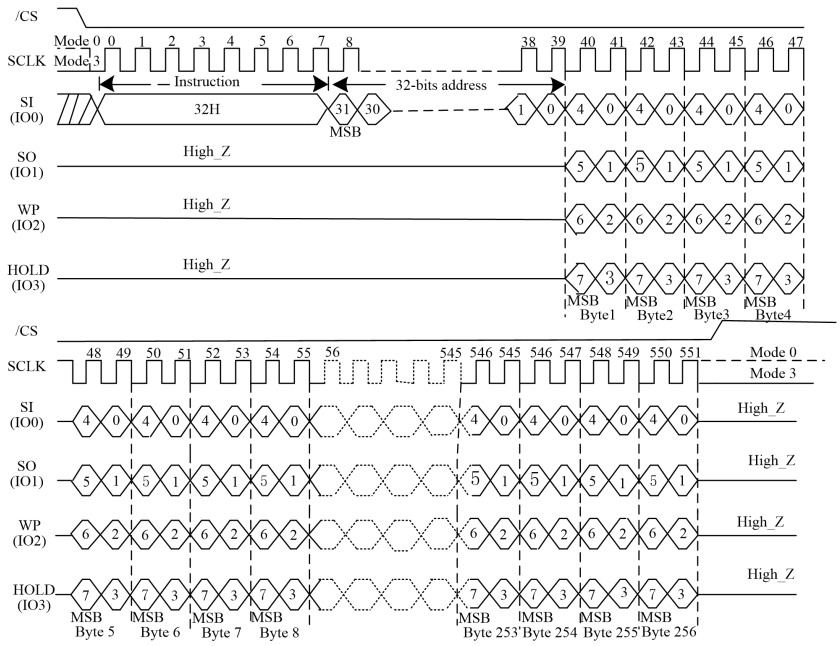


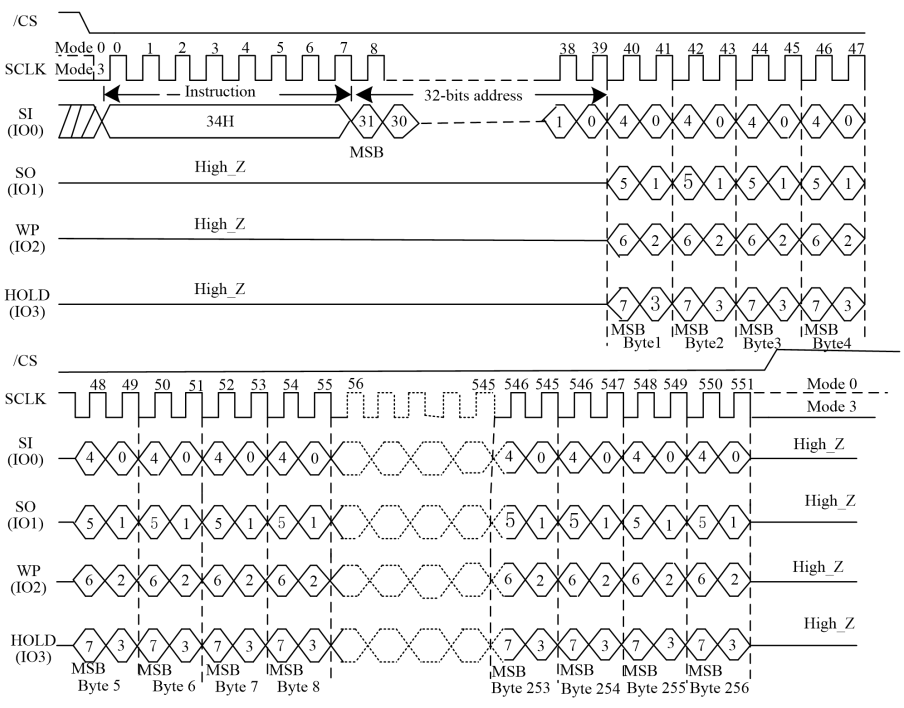
Figure 141. Quad Page Program Sequence Diagram (SPI Mode only/4-Byte Address Mode)



7.4.4 Quad Input Page Program with 4-Byte Address (34H)

The Quad Input Page Program with 4-Byte Address instruction is similar to the Quad Input Page Program instruction except that it requires 32-bit address instead of 24-bit address. No matter the device is operating in 3-Byte Address Mode or 4-byte Address Mode, the Quad Input Page Program with 4-Byte Address instruction will always require 32-bit address to access the entire 256Mb memory. The Quad Enable bit (QE) of Status Register must be set to enable.

Figure 142. Quad Page Program with 4-Byte Address Sequence Diagram (SPI Mode only)



7.4.5 Sector Erase (20H)

The Sector Erase instruction is for erasing the all data of the chosen sector. A Write Enable instruction must previously have been executed to set the Write Enable Latch bit. The Sector Erase instruction is entered by driving /CS low, followed by the instruction code, and 3-address byte on SI. Any address inside the sector is a valid address for the Sector Erase instruction. /CS must be driven low for the entire duration of the sequence.

See ***Figure 143-Figure 146***, The Sector Erase instruction sequence: /CS goes low-> sending Sector Erase instruction-> 3-byte/4-byte address on SI ->/CS goes high. /CS must be driven high after the eighth bit of the last address byte has been latched in; otherwise the Sector Erase instruction is not executed. As soon as /CS is driven high, the self-timed Sector Erase cycle (whose duration is tSE) is initiated. While the Sector Erase cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Sector Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch bit is reset. A Sector Erase instruction applied to a sector which is protected by the Block Protect (BP4, BP3, BP2, BP1, BP0) bits (see ***Table 9-Table 10***) is not executed.

Figure 143. Sector Erase Sequence Diagram (SPI Mode/3-Byte Address Mode)

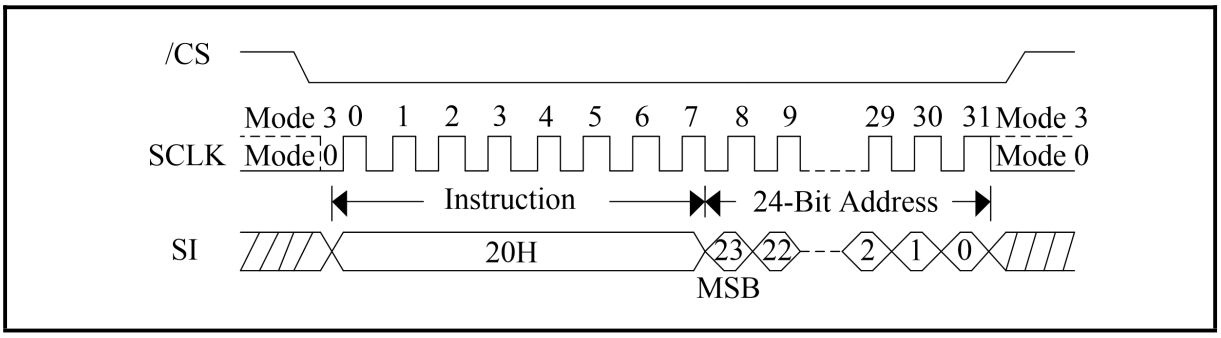


Figure 144. Sector Erase Sequence Diagram (SPI Mode/4-Byte Address Mode)

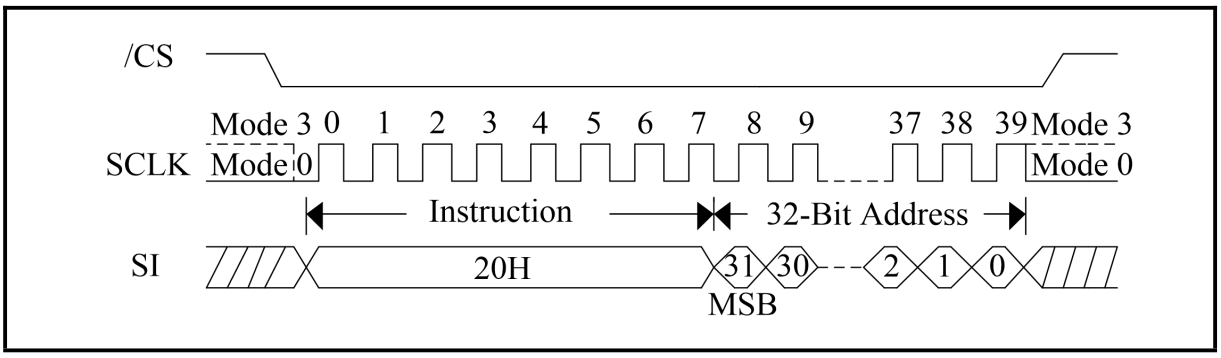


Figure 145. Sector Erase Sequence Diagram (QPI Mode/3-Byte Address Mode)

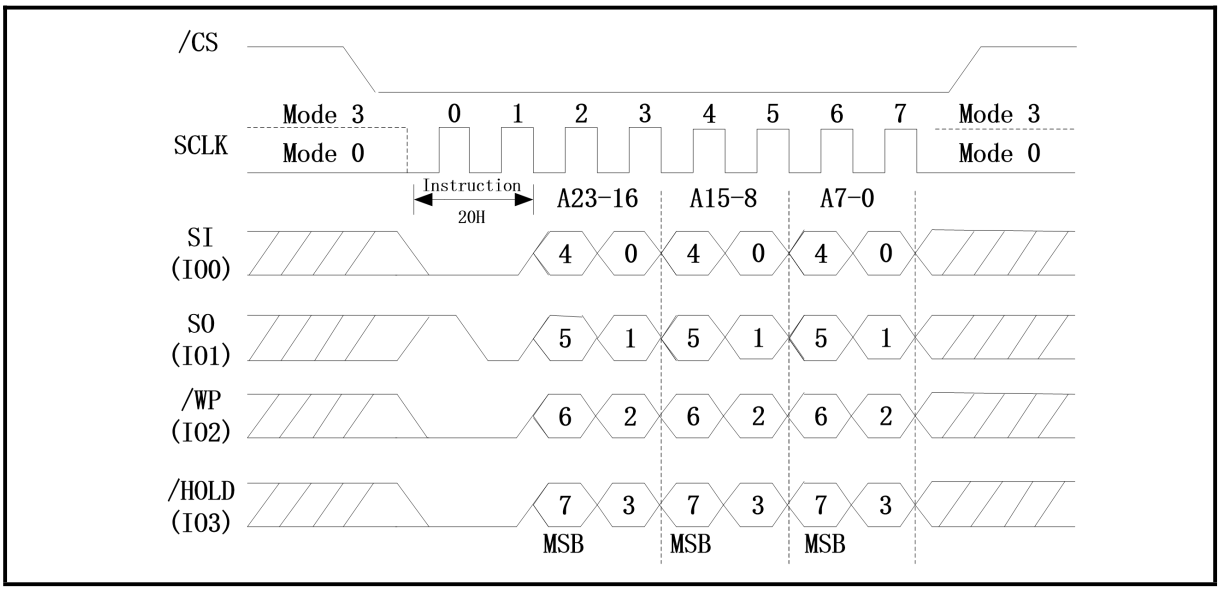
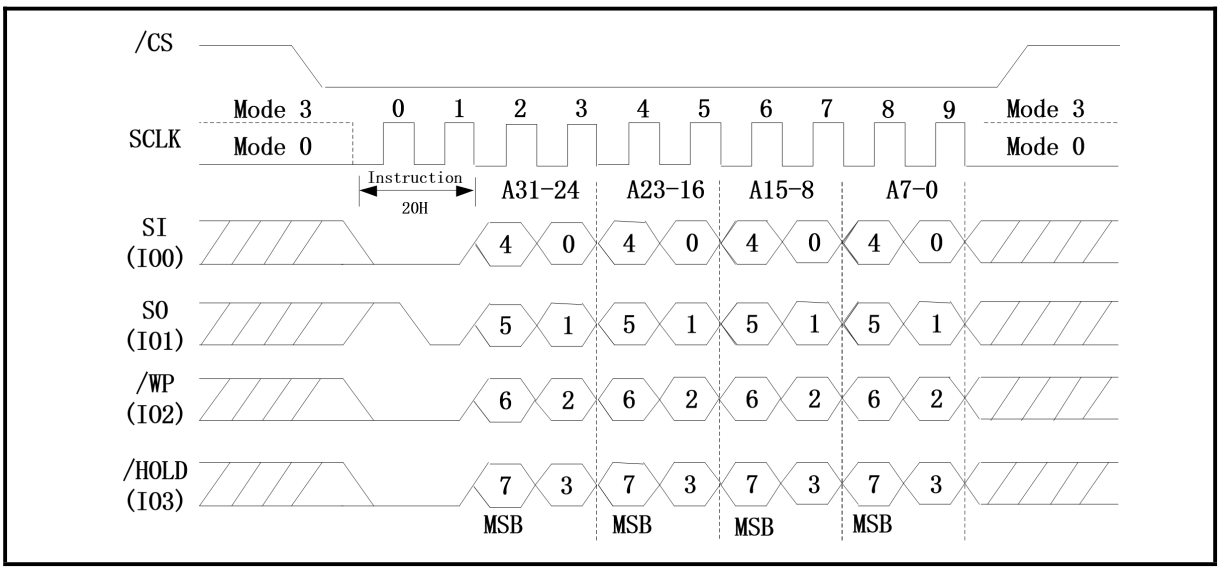


Figure 146. Sector Erase Sequence Diagram (QPI Mode/4-Byte Address Mode)



7.4.6 Sector Erase with 4-Byte Address (21H)

The Sector Erase with 4-Byte Address instruction is similar to the Sector Erase instruction except that it requires 32-bit address instead of 24-bit address. No matter the device is operating in 3-Byte Address Mode or 4-byte Address Mode, the Sector Erase with 4-Byte Address instruction will always require 32-bit address to access the entire 256Mb memory.

Figure 147. Sector Erase with 4-Byte Address (SPI Mode)

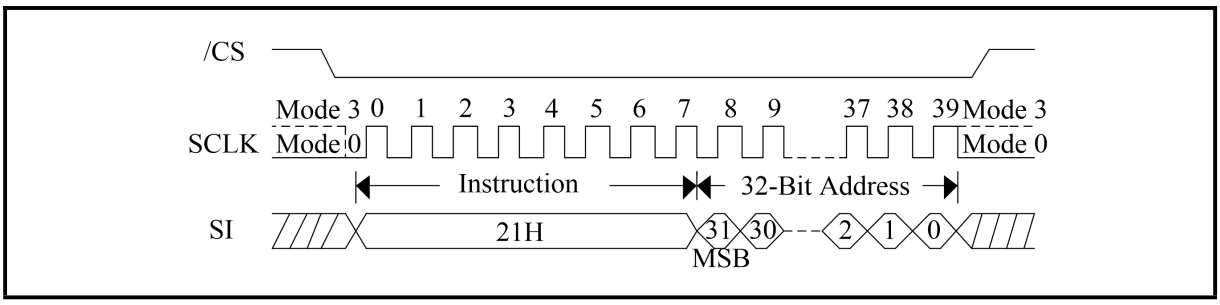
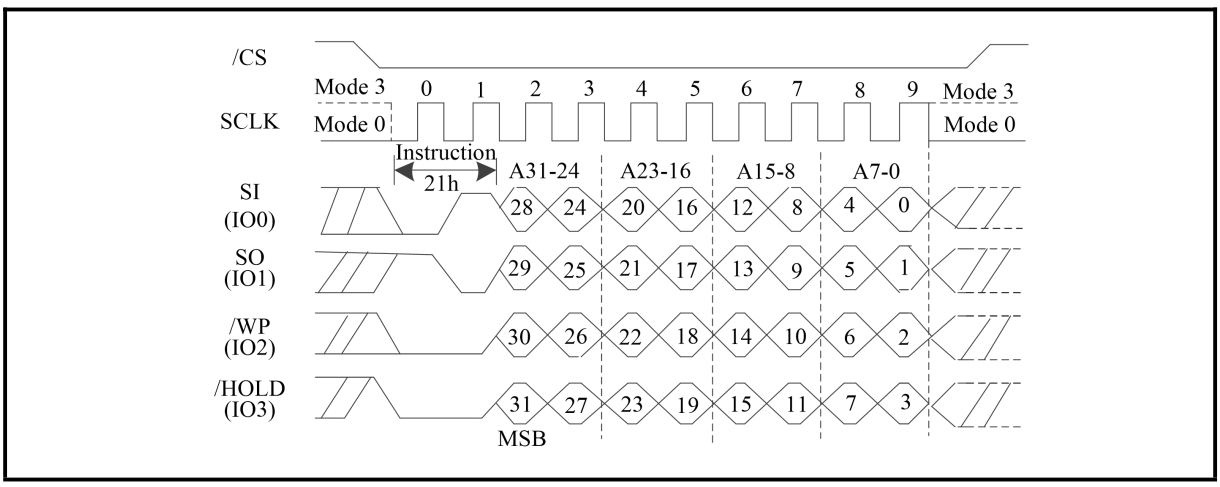


Figure 148. Sector Erase with 4-Byte Address (QPI Mode)



7.4.7 32KB Block Erase (52H)

The 32KB Block Erase instruction is for erasing the all data of the chosen block. A Write Enable instruction must previously have been executed to set the Write Enable Latch bit. The 32KB Block Erase instruction is entered by driving /CS low, followed by the instruction code, and 3-byte/4-byte address on SI. Any address inside the block is a valid address for the 32KB Block Erase instruction. /CS must be driven low for the entire duration of the sequence.

See ***Figure 149-Figure 152***, the 32KB Block Erase instruction sequence: /CS goes low ->sending 32KB Block Erase instruction ->3-byte/4-byte address on SI ->/CS goes high. /CS must be driven high after the eighth bit of the last address byte has been latched in; otherwise the 32KB Block Erase instruction is not executed. As soon as /CS is driven high, the self-timed Block Erase cycle (whose duration is tBE) is initiated. While the Block Erase cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Block Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch bit is reset. A 32KB Block Erase instruction applied to a block which is protected by the Block Protect (BP4, BP3, BP2, BP1, BP0) bits (see ***Table 9-Table 10***) is not executed.

Figure 149. 32KB Block Erase Sequence Diagram (SPI Mode/3-Byte Address Mode)

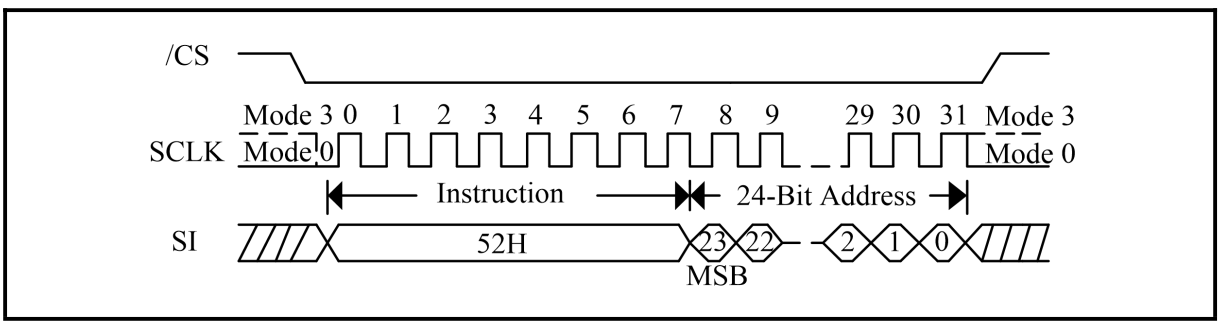


Figure 150. 32KB Block Erase Sequence Diagram (SPI Mode/4-Byte Address Mode)

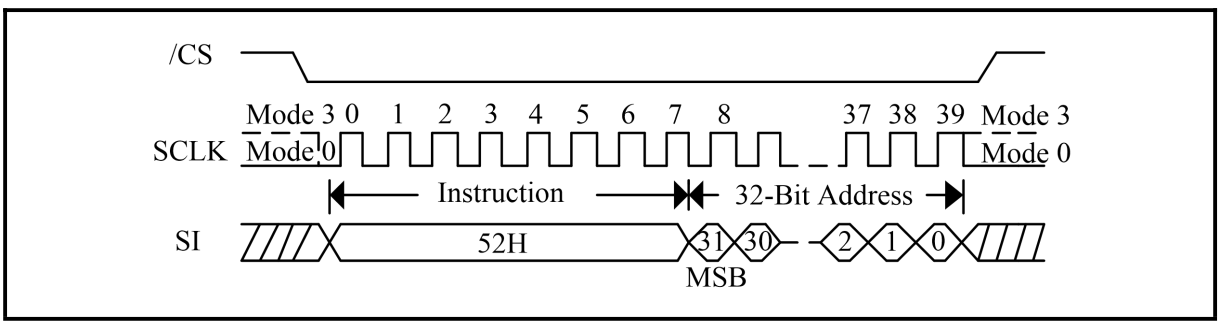


Figure 151. 32KB Block Erase Sequence Diagram (QPI Mode/3-Byte Address Mode)

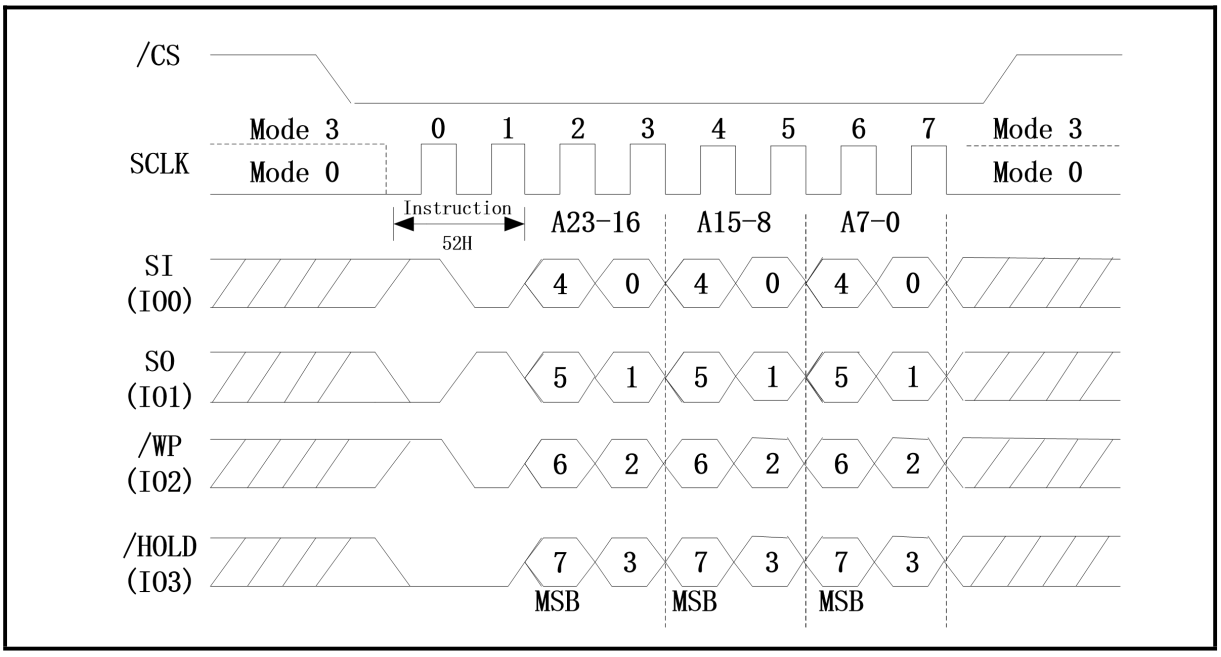
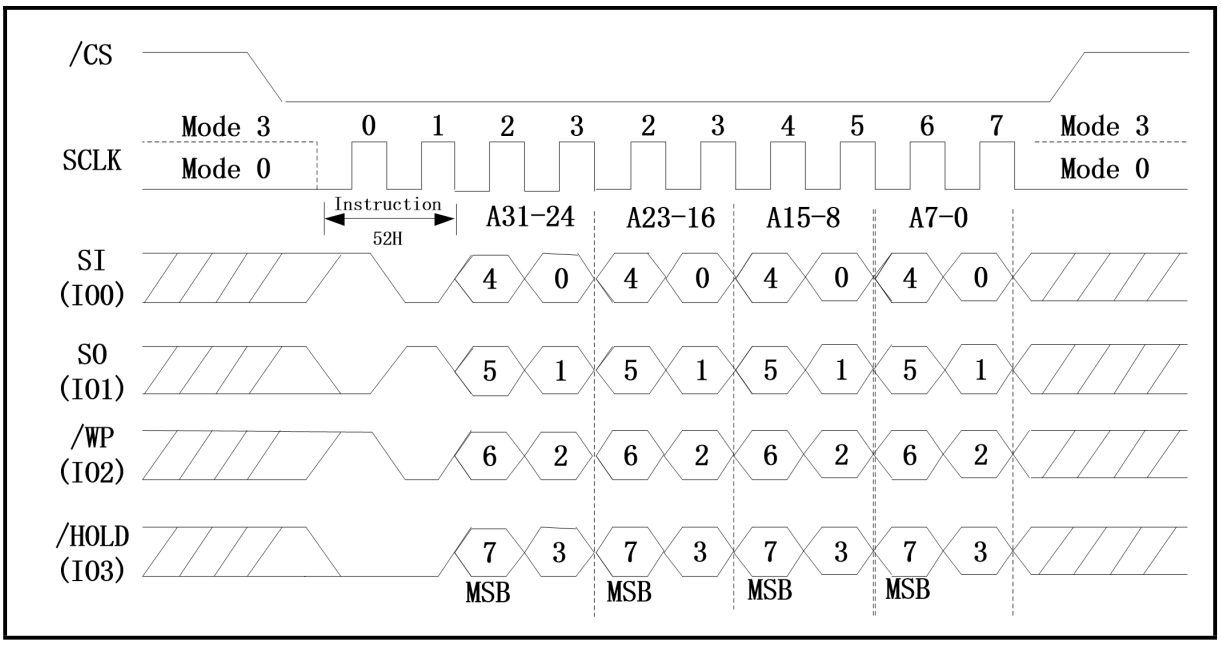


Figure 152. 32KB Block Erase Sequence Diagram (QPI Mode/4-Byte Address Mode)



7.4.8 32KB Block Erase with 4-Byte Address (5CH)

The 32KB Block Erase with 4-Byte Address instruction is similar to the 32KB Block Erase instruction except that it requires 32-bit address instead of 24-bit address. No matter the device is operating in 3-Byte Address Mode or 4-byte Address Mode, the 32KB Block Erase with 4-Byte Address instruction will always require 32-bit address to access the entire 256Mb memory.

Figure 153. 32KB Block Erase with 4-Byte Address (SPI Mode)

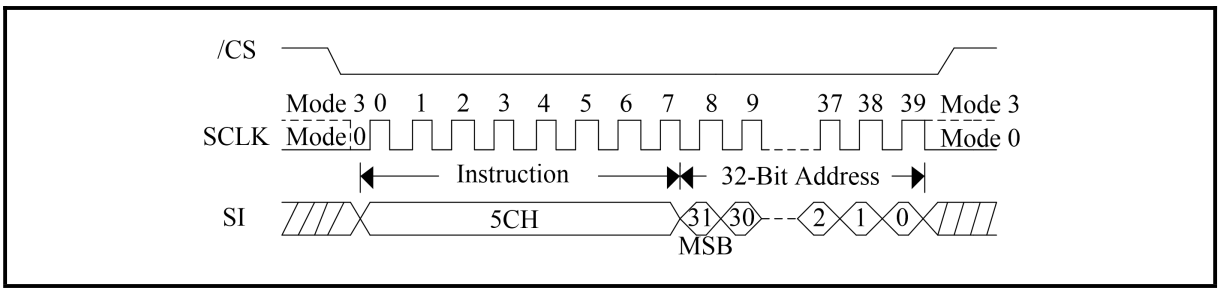
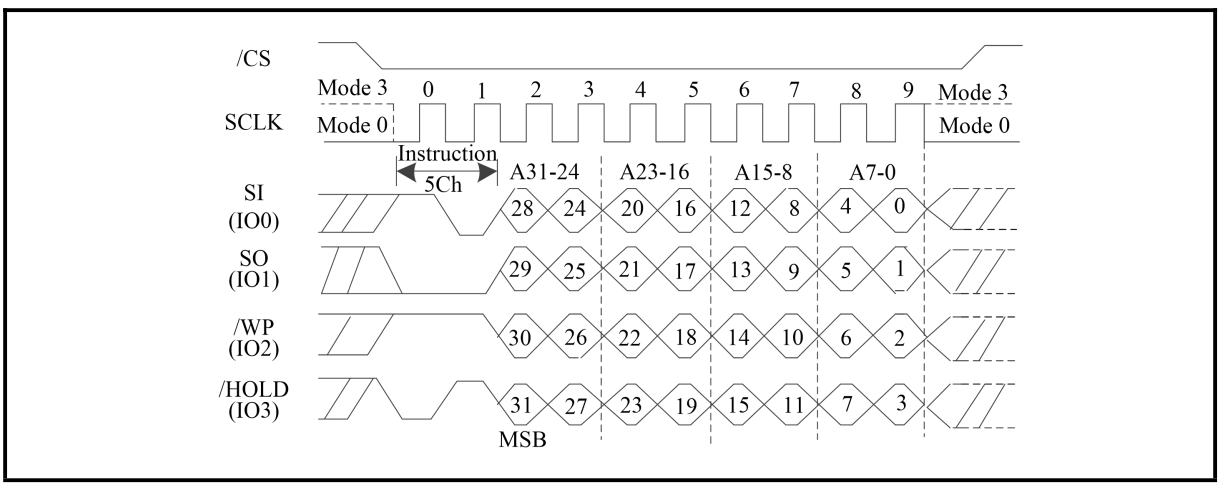


Figure 154. 32KB Block Erase with 4-Byte Address (QPI Mode)



7.4.9 64KB Block Erase (D8H)

The 64KB Block Erase instruction is for erasing the all data of the chosen block. A Write Enable instruction must previously have been executed to set the Write Enable Latch bit. The 64KB Block Erase instruction is entered by driving /CS low, followed by the instruction code, and 3-byte/4-byte address on SI. Any address inside the block is a valid address for the 64KB Block Erase instruction. /CS must be driven low for the entire duration of the sequence.

See ***Figure 155-Figure 158***, the 64KB Block Erase instruction sequence: /CS goes low sending 64KB Block Erase instruction 3-byte/4-byte address on SI /CS goes high. /CS must be driven high after the eighth bit of the last address byte has been latched in; otherwise the 64KB Block Erase instruction is not executed. As soon as /CS is driven high, the self-timed Block Erase cycle (whose duration is tBE) is initiated. While the Block Erase cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Block Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch bit is reset. A 64KB Block Erase instruction applied to a block which is protected by the Block Protect (BP4, BP3, BP2, BP1, BP0) bits (see ***Table 9-Table 10***) is not executed.

Figure 155. 64KB Block Erase Sequence Diagram (SPI Mode/3-Byte Address Mode)

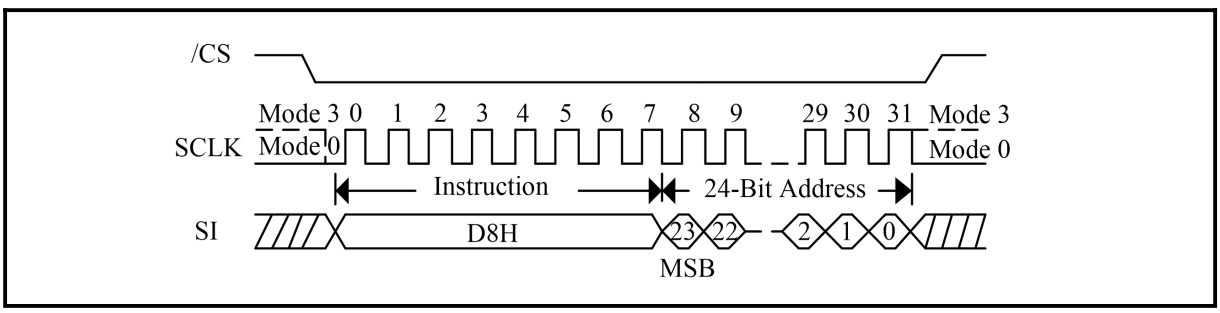


Figure 156. 64KB Block Erase Sequence Diagram (SPI Mode/4-Byte Address Mode)

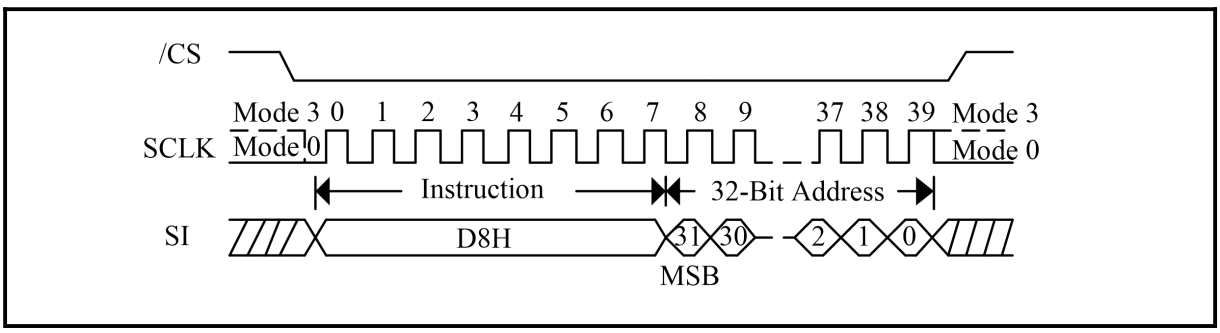


Figure 157. 64KB Block Erase Sequence Diagram (QPI Mode/3-Byte Address Mode)

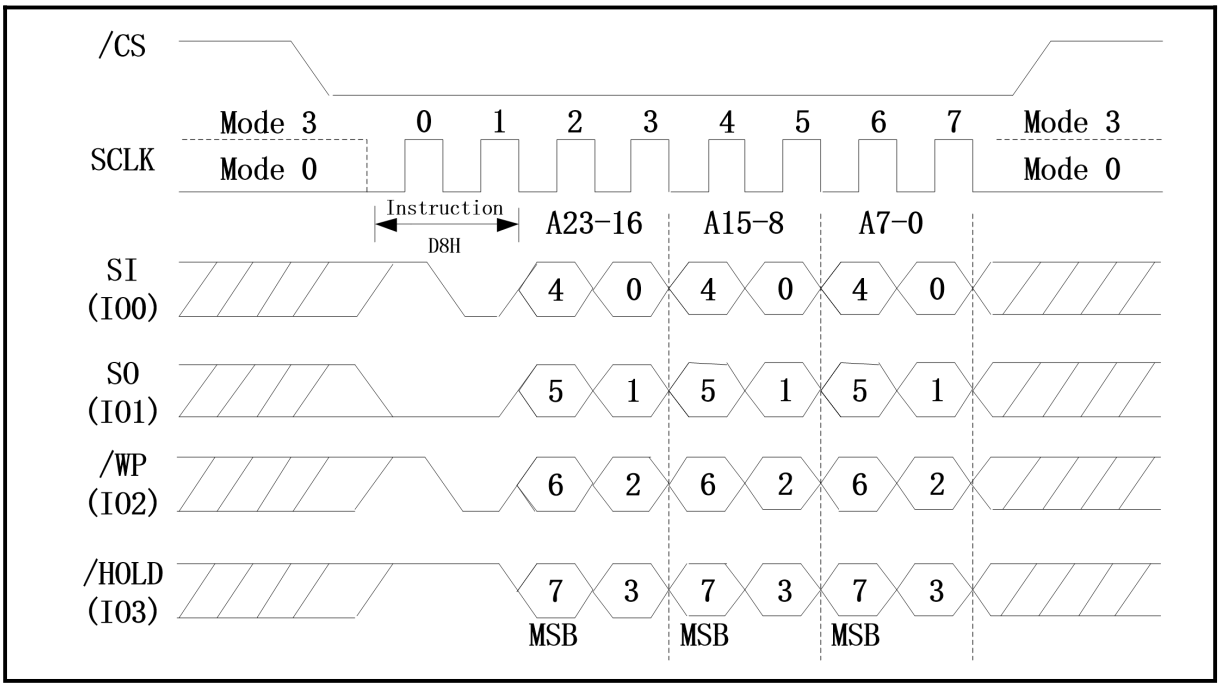
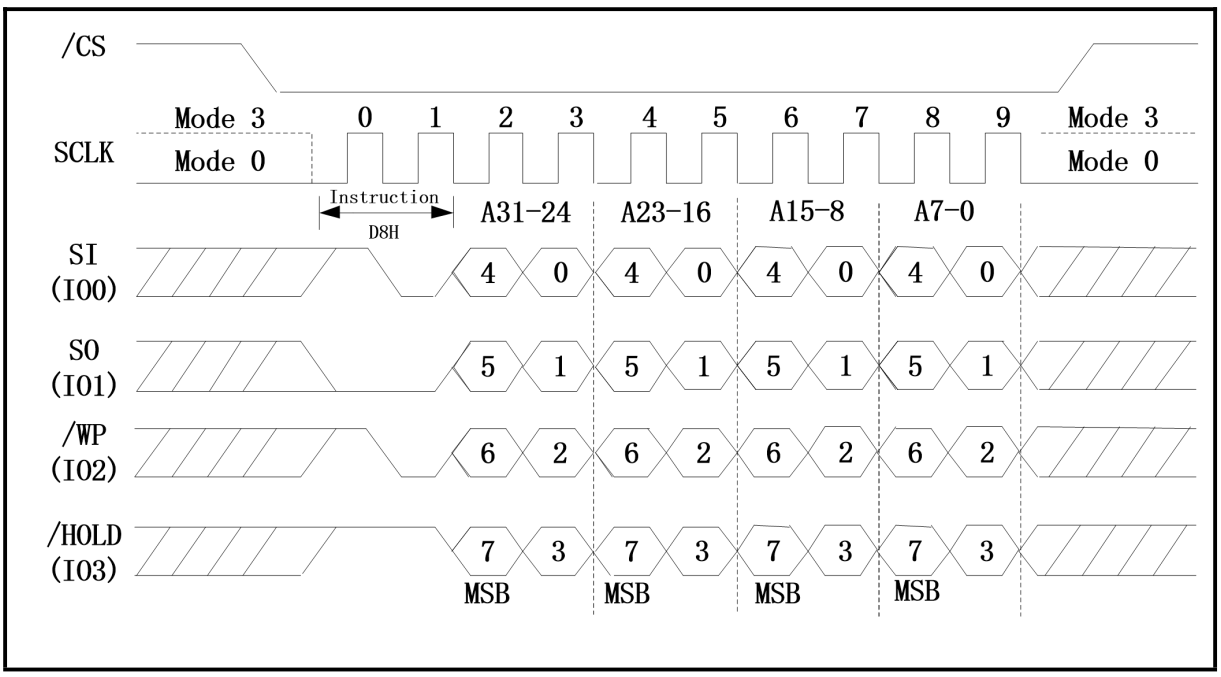


Figure 158. 64KB Block Erase Sequence Diagram (QPI Mode/4-Byte Address Mode)



7.4.10 64KB Block Erase with 4-Byte Address (DCH)

The 64KB Block Erase with 4-Byte Address instruction is similar to the 64KB Block Erase instruction except that it requires 32-bit address instead of 24-bit address. No matter the device is operating in 3-Byte Address Mode or 4-byte Address Mode, the 64KB Block Erase with 4-Byte Address instruction will always require 32-bit address to access the entire 256Mb memory.

Figure 159. 64KB Block Erase with 4-Byte Address (SPI Mode)

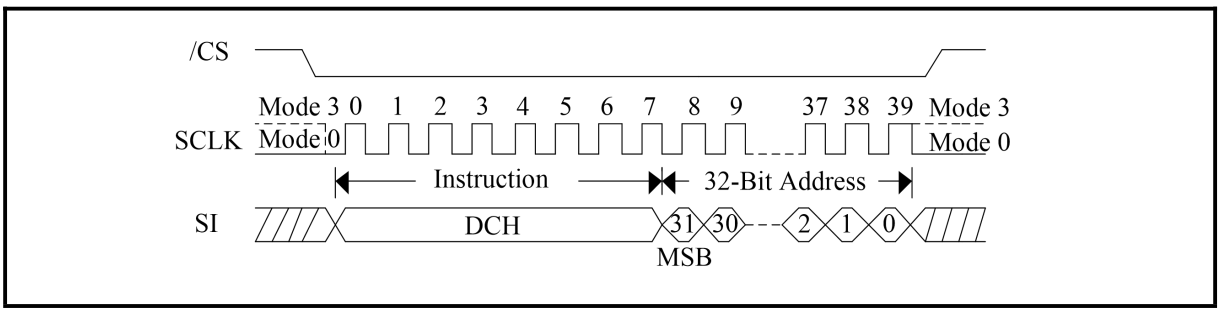
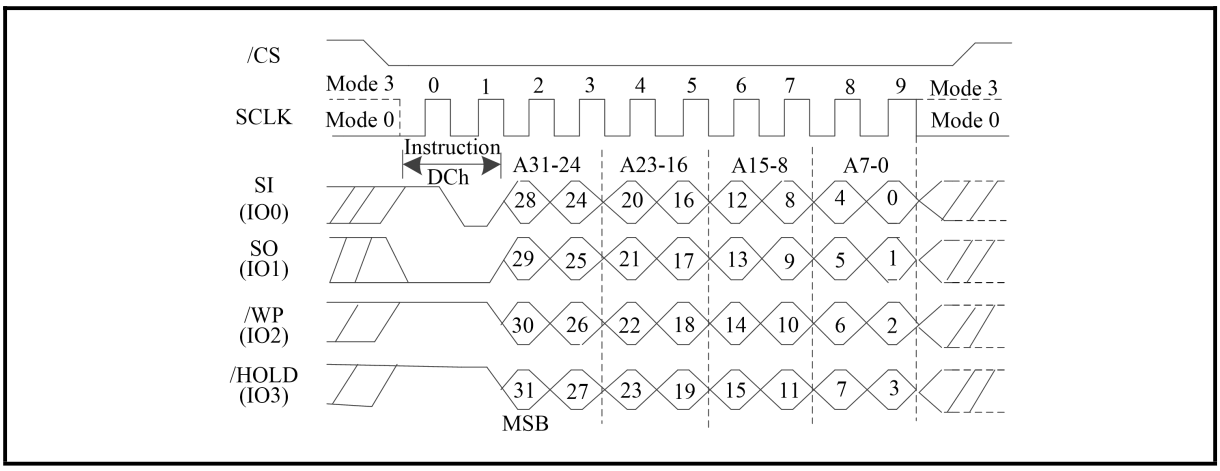


Figure 160. 64KB Block Erase with 4-Byte Address (QPI Mode)



7.4.11 Chip Erase (60/C7H)

The Chip Erase instruction sets all memory within the device to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Chip Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the /CS pin low and shifting the instruction code “C7h” or “60h”. The Chip Erase instruction sequence is shown in ***Figure 161-Figure 162***.

The /CS pin must be driven high after the eighth bit has been latched. If this is not done the Chip Erase instruction will not be executed. After /CS is driven high, the self-timed Chip Erase instruction will commence for a time duration of tCE. While the Chip Erase cycle is in progress, the Read Status Register instruction may still be accessed to check the status of the WIP bit.

The WIP bit is a 1 during the Chip Erase cycle and becomes a 0 when finished and the device is ready to accept other Instructions again. After the Chip Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Chip Erase instruction is executed only if all Block Protect (BP2, BP1, and BP0) bits are 0.The Chip Erase instruction is ignored if one or more sectors are protected.

Figure 161. Chip Erase Sequence Diagram (SPI Mode)

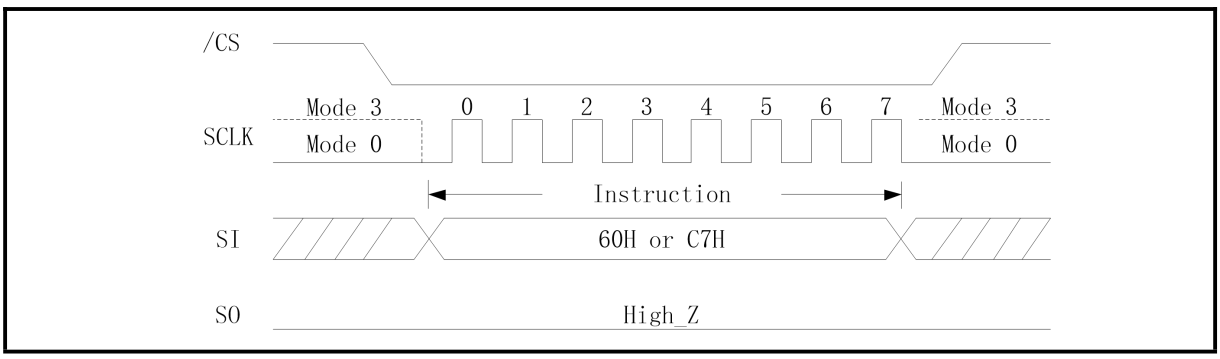
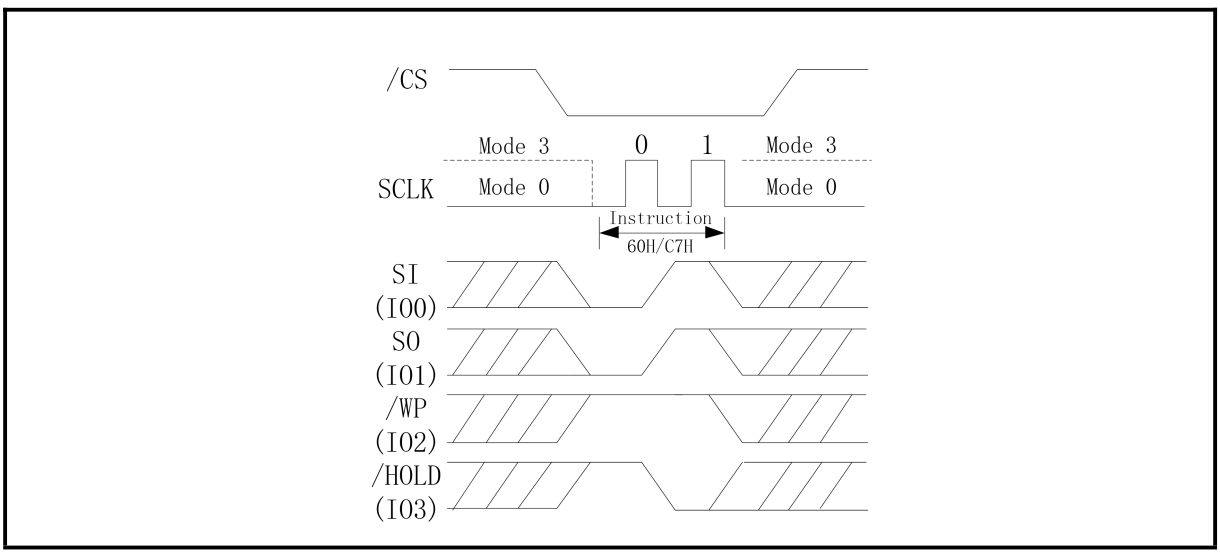


Figure 162. Chip Erase Sequence Diagram (QPI Mode)



7.4.12 Program/Erase Suspend (75H)

The Program/Erase Suspend instruction “75h” allows the system to interrupt a Page Program or a Sector/32K/64K Block Erase operation (The time between the Program/Erase instruction and the Program/Erase Suspend instruction is tPS/tES). After the program operation has entered the suspended state, the memory array can be read or erase except for the page being programmed. And after the erase operation has entered the suspended state, the memory array can be read or programed except for the big block being erased. Write status register operation can't be

suspended. The Program/Erase Suspend instruction sequence is shown in ***Figure 163-Figure 164***.

Table 22. Readable or Erasable Area of Memory While a Program Operation is Suspended

Suspended operation	Readable or Erasable Region Of Memory Array
Page Program	All but the Page being programmed
Page Program with 4-Byte Address	All but the Page being programmed
Quad Page Program	All but the Page being programmed
Quad Page Program with 4-Byte Address	All but the Page being programmed

Table 23. Readable or Programmable Area of Memory While an Erase Operation is Suspended

Suspended operation	Readable Region or Programmable Of Memory Array
Sector Erase(4KB)	All but the Big Block being Erased
Sector Erase with 4-Byte Address (4KB)	All but the Big Block being Erased
Block Erase(32KB)	All but the Big Block being Erased
Block Erase with 4-Byte Address (32KB)	All but the Big Block being Erased
Block Erase(64KB)	All but the Big Block being Erased
Block Erase with 4-Byte Address (64KB)	All but the Big Block being Erased

When the Serial NOR Flash receives the Suspend instruction, there is a latency of tPSL or tESL before the Write Enable Latch (WEL) bit clears to “0” and the SUS2 or SUS1 sets to “1”, after which the device is ready to accept one of the instructions listed in "Table Acceptable Instructions During Program/Erase Suspend after tPSL/tESL" (e.g. FAST READ). Refer to " AC Characteristics" for tPSL and tESL timings. "Table Acceptable instructions During Suspend (tPSL/tESL not required)" lists the Instructions for which the tPSL and tESL latencies do not apply. For example, “05h”, “66h” and “99h” can be issued at any time after the Suspend instruction.

Status Register bit 15 (SUS2) and bit 10 (SUS1) can be read to check the suspend status. The SUS2 (Program Suspend Bit) sets to “1” when a program instruction is suspended. The SUS1 (Erase Suspend Bit) sets to “1” when an erase operation is suspended. The SUS2 or SUS1 clears to “0” when the program or erase instruction is resumed.

Table 24. Acceptable instructions During Program/Erase Suspend after tPSL/tESL

Instruction Name	Instruction code	Suspend Type	
		Program Suspend	Erase Suspend
Software Die Select	C2h	*	*
Read Active Die ID#	F8h	*	*
Write Enable	06h	*	*
Write Disable	04h	*	*
Read Extended Address Register	C8H	*	*
Write Extended Address Register	C5H	*	*
Enter 4-Byte Address Mode	B7h	*	*
Exit 4-Byte Address Mode	E9h	*	*
Enter QPI Mode	38h	*	*
Exit QPI Mode	FFh	*	*
Read Extended Address Register	C8h	*	*
Read Data	03h	*	*
Read Data with 4-Byte Address	13h	*	*

Instruction Name	Instruction code	Suspend Type	
		Program Suspend	Erase Suspend
Fast Read	0Bh	*	*
DTR Fast Read	0Dh	*	*
Fast Read with 4-Byte Address	0Ch	*	*
Dual Output Fast Read	3Bh	*	*
Fast Read Dual Output with 4-Byte Address	3Ch	*	*
Quad Output Fast Read	6Bh	*	*
Fast Read Quad Output with 4-Byte Address	6Ch	*	*
Dual I/O Fast Read	BBh	*	*
DTR Fast Read Dual I/O	BDh	*	*
Fast Read Dual I/O with 4-Byte Address	BCh	*	*
Quad I/O Fast Read	EBh	*	*
DTR Fast Read Quad I/O	EDh	*	*
Fast Read Quad I/O with 4-Byte Address	ECh	*	*
DTR Quad I/O Fast Read with 4- Byte Address	EEh	*	*
Quad I/O Word Fast Read	E7h	*	*
Set Burst with Wrap	77h	*	*
Set Read Parameters	C0h	*	*
Read Mftr./Device ID	90h	*	*
Dual IO Read Mftr./Device ID	92h	*	*
Quad IO Read Mftr./Device ID	94h	*	*
Read JEDEC ID	9Fh	*	*
Read Unique ID Number	4Bh	*	*
Release Powen-down/Device ID	ABh	*	*
Read Securty Registers	48h	*	*
Read SFDP	5Ah	*	*
Page Program	02h		*
Page Program with 4-Byte Address	12h		*
Quad Page Program	32h		*
Quad Input Page Program with 4-Byte Address	34h		*
Sector Erase	20h	*	
Sector Erase with 4-Byte Address	21h	*	
32KB Block Erase	52h	*	
32KB Block Erase with 4-Byte Address	5Ch	*	
64KB Block Erase	D8h	*	
64KB Block Erase with 4-Byte Address	DCh	*	
Program/Erase Resume	7Ah	*	*
Read Lock Register	2Dh	*	*
Read SPB Lock Register	A7h	*	*
Read SPB Status	E2h	*	*
Read DPB Status	3Dh	*	*

Instruction Name	Instruction code	Suspend Type	
		Program Suspend	Erase Suspend
Read Unprotect Solid Protect Bit	AAh	*	*
Read Password Register	27H	*	*

Table 25. Acceptable Instructions During Suspend（tPSL/tESL not required）

Instruction Name	Instruction code	Suspend Type	
		Program Suspend	Erase Suspend
Read Status Register-1	05H	*	*
Read Status Register-2	35H	*	*
Read Status Register-3	15H	*	*
Enable Reset	66H	*	*
Reset Device	99H	*	*

tPSL: Program Suspend Latency; tESL: Erase Suspend Latency.

Figure 163. Program/Erase Suspend Instruction Sequence (SPI Mode)

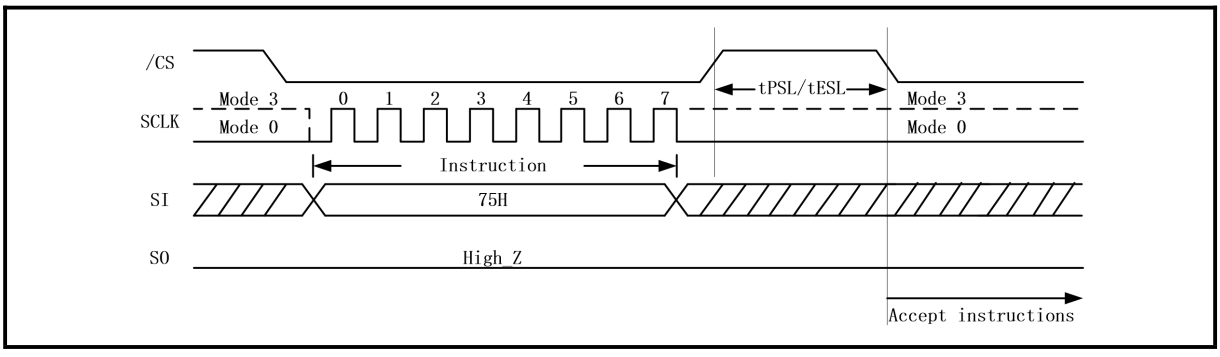
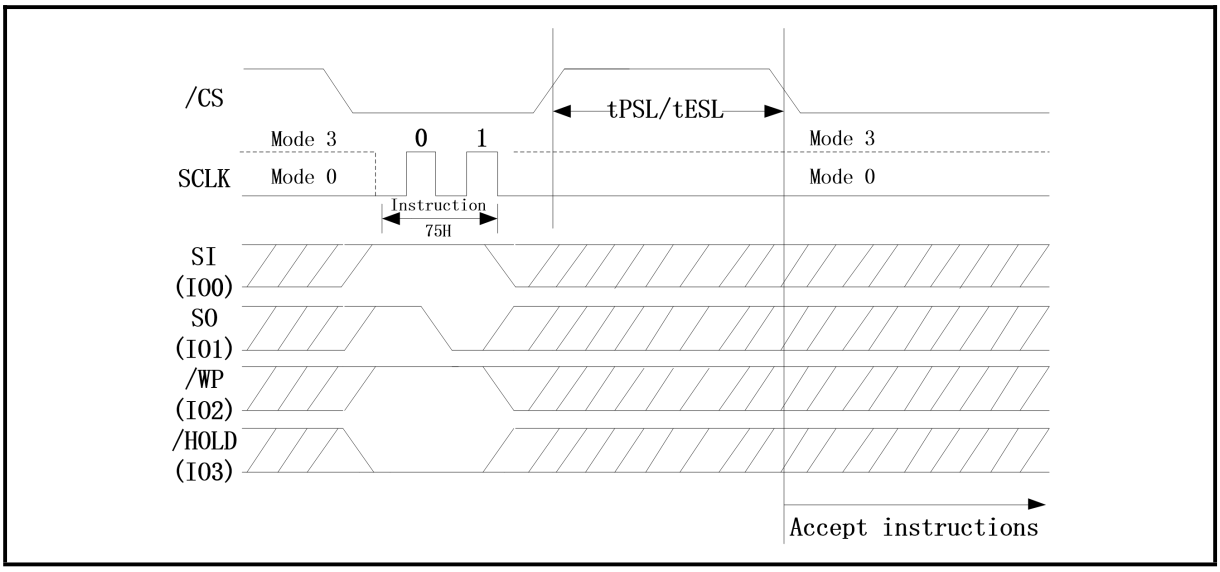


Figure 164. Program/Erase Suspend Instruction Sequence (QPI Mode)



7.4.13 Program/Erase Resume (7AH)

The Program/Erase Resume instruction “7Ah” must be written to resume the Sector or Block Erase operation or the Page Program operation after an Program/Erase Suspend. The Resume instruction “7AH” will be accepted by the device only if the SUS bit in the Status Register equals to 1 and the WIP bit equals to 0.

After the Resume instruction is issued the SUS bit will be cleared from 1 to 0 immediately, the WIP bit will be set from 0 to 1 within 200 ns and the Sector or Block will complete the erase operation or the page will complete the program operation. If the SUS bit equals to 0 or the WIP bit equals to 1, the Resume instruction “7Ah” will be ignored by the device. The Program/Erase Resume instruction sequence is shown in ***Figure 165-Figure 166***.

Figure 165. Program/Erase Resume Instruction Sequence (SPI Mode)

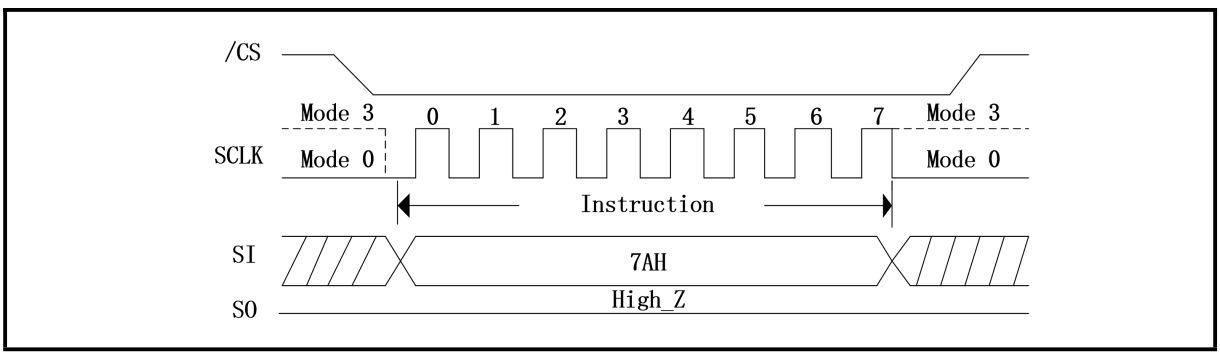
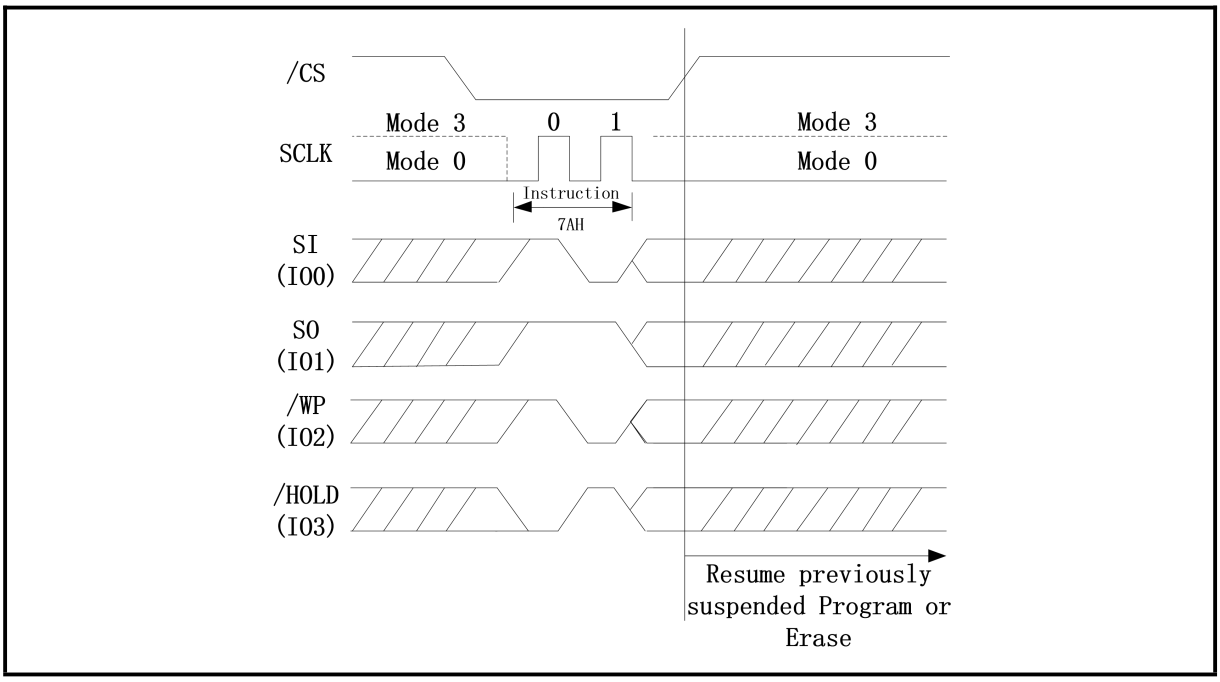


Figure 166. Program/Erase Resume Instruction Sequence (QPI Mode)



7.5 Advanced Block/Sector Protection Instructions

7.5.1 Read Lock Register (2DH)

The Read Lock Register (2Dh) instruction is used to read the Lock Register. The Lock Register is a 16-bit one-time programmable register. Lock Register bits [2:1] select between Solid Protection mode and Password Protection mode.

See ***Figure 167-Figure 168,*** to read out the bit value of the Lock Register, the Read Lock Register (2Dh) instruction must be issued by driving /CS low, shifting the instruction code “2Dh” into the Data Input (SI or IO0-IO3) pin on the rising edge of CLK. The Lock Register value will be shifted out on the SO or IO0-IO3 pin at the falling edge of CLK with most significant bit (MSB) first as shown in Figure.

Figure 167. Read Lock Register (SPI Mode)

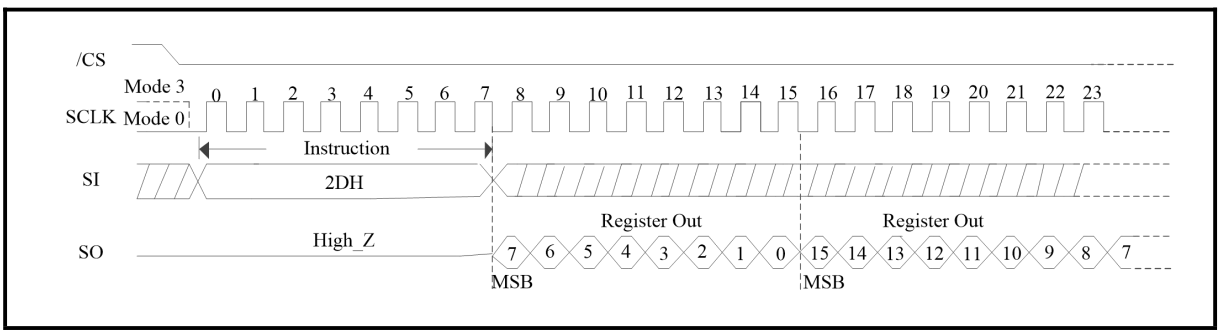
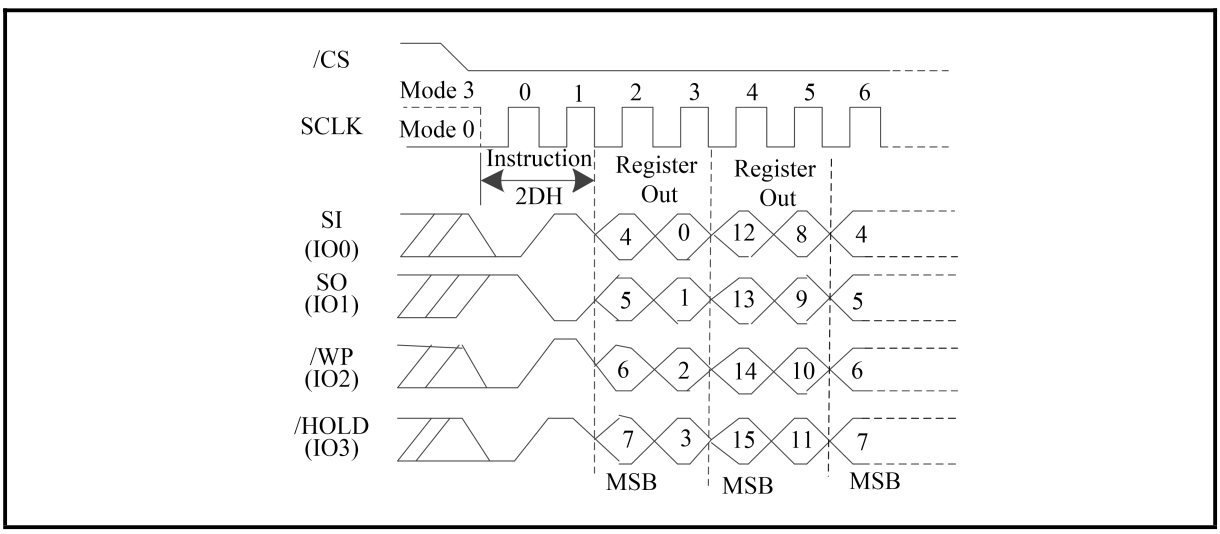


Figure 168. Read Lock Register (QPI Mode)



7.5.2 Write Lock Register (2CH)

The Write Lock Register (2Ch) instruction is used to write the Lock Register. The Lock Register is a 16-bit one-time programmable register. Lock Register bits [2:1] select between Solid Protection mode and Password Protection mode. Programming Lock Register bit 1 to “0” permanently selects Solid Protection mode and permanently disables Password Protection mode. Conversely, programming bit 2 to “0” permanently selects Password Protection mode and permanently disables Solid Protection mode. Bits 1 and 2 cannot be programmed to “0” at the same time otherwise the device will abort the operation.

A Write Enable (06h) instruction must be executed to set the WEL bit before sending the Write Lock Register (2Ch) instruction.

See ***Figure 169-Figure 170***, to write the Lock Register, the Write Lock Register (2Ch) instruction must be issued by driving /CS low, shifting the instruction code “2Ch” into the Data Input (SI or

IO0-IO3) pin on the rising edge of CLK, followed by the value of Lock Register bit 7-0 and bit 15-8, and then driving /CS high.

Figure 169. Write Lock Register (SPI Mode)

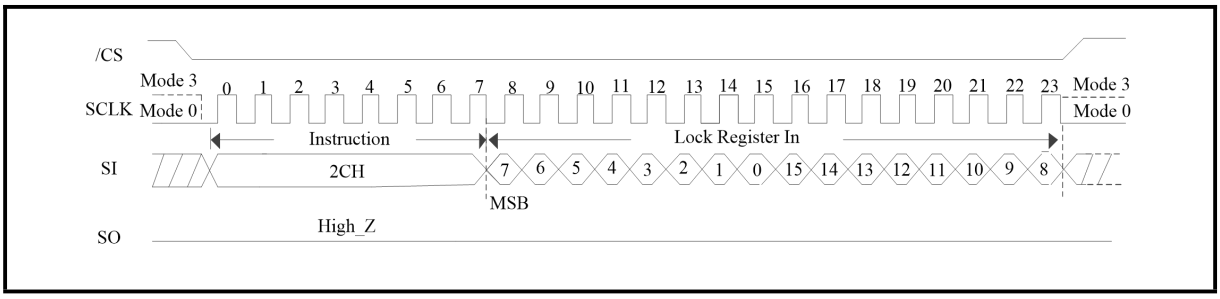
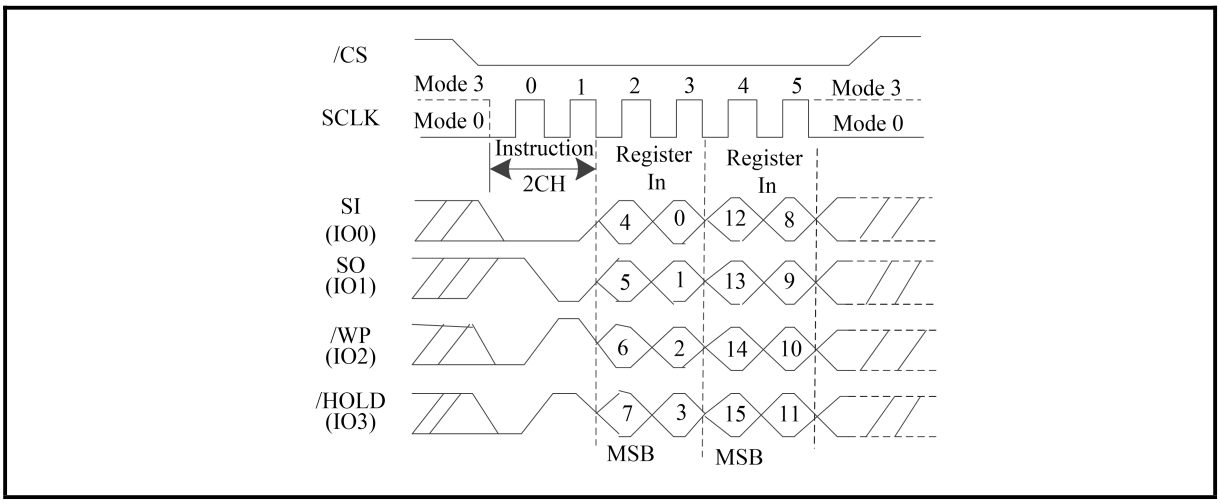


Figure 170. Write Lock Register (QPI Mode)



7.5.3 SPB Lock Bit Clear (A6H)

The SPB Lock Bit Clear (A6h) instruction can be used to write the SPB Lock Bit to “0” and protect the SPB bits.

In Solid Protection mode, once the SPB Lock Bit has been written to “0”, there is no instruction (except a software reset) to set the bit back to “1”. A power-on cycle or reset is required to set the SPB lock bit back to “1”.

In Password Protection mode, the SPB Lock Bit defaults to “0” after power-on or reset. A valid password must be provided to set the SPB Lock Bit to “1” to allow the SPBs to be modified. After the SPBs have been set to the desired status, use the SPB Lock Bit Clear instruction to clear the SPB Lock Bit back to “0” in order to prevent further modification.

A Write Enable (06h) instruction must be executed to set the WEL bit before sending the SPB Lock Bit Clear instruction.

See ***Figure 171-Figure 172***, the instruction must be issued by driving /CS low, shifting the instruction code “A6h” into the Data Input (SI or IO0-IO3) pin on the rising edge of CLK, and then driving /CS high.

Figure 171. SPB Lock Bit Clear (SPI Mode)

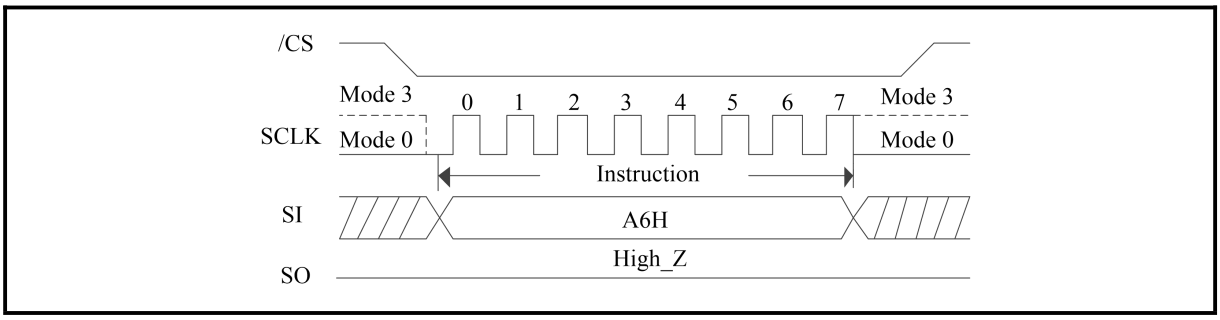
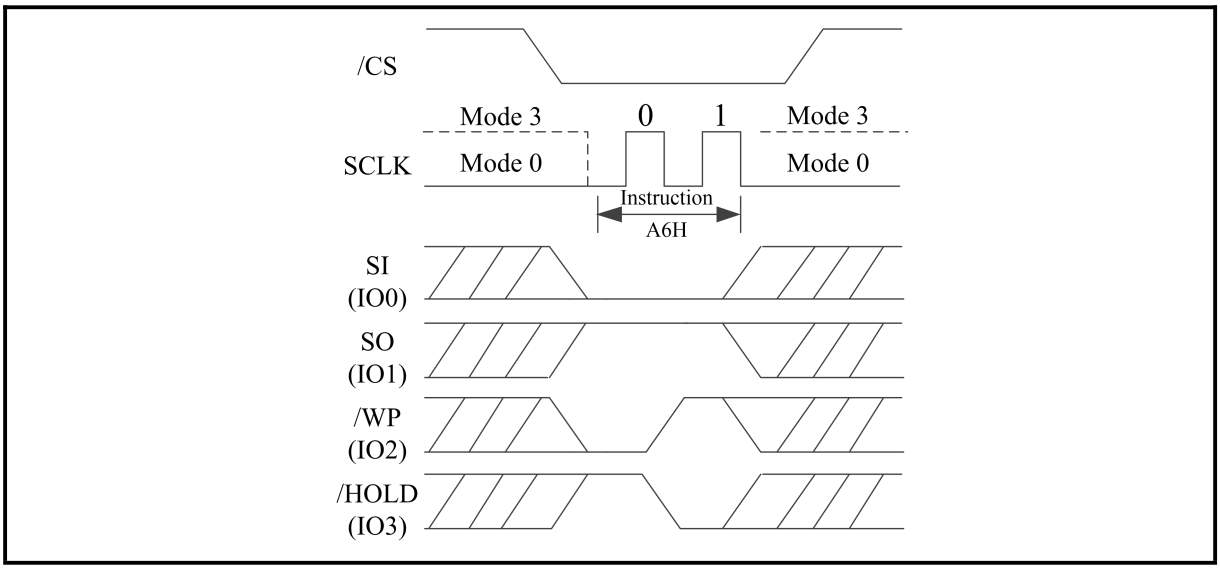


Figure 172. SPB Lock Bit Clear (QPI Mode)



7.5.4 Read SPB Lock Register (A7H)

The Read SPB Lock Register (A7h) instruction is used to read the SPB Lock Register. The SPB Lock Bit is a volatile bit located in bit 0 of the SPB Lock Register.

See ***Figure 173-Figure 174***, to read out the bit value of the SPB Lock Bit, the Read SPB Lock Register (A7h) instruction must be issued by driving /CS low, shifting the instruction code “A7h” into the Data Input (SI or IO0-IO3) pin on the rising edge of CLK. The SPB Lock Register value will be shifted out on the SO or IO0-IO3 pin at the falling edge of CLK with most significant bit (MSB) first.

Figure 173. Read SPB Lock Register (SPI Mode)

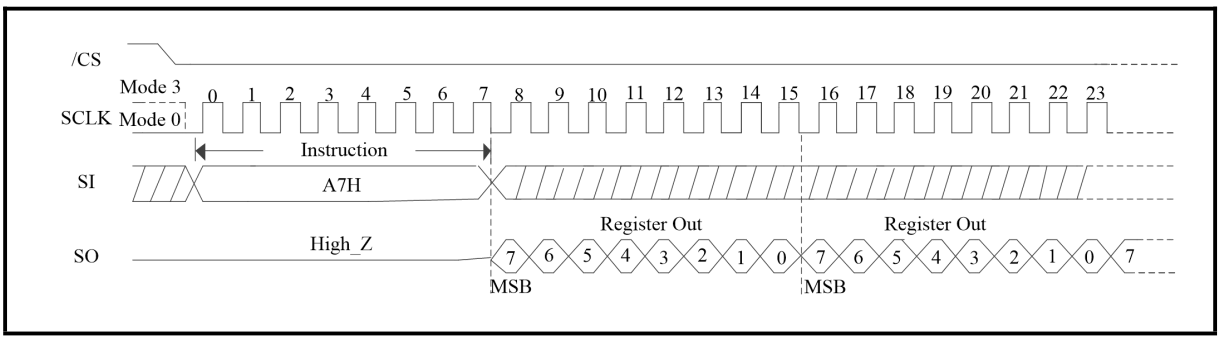
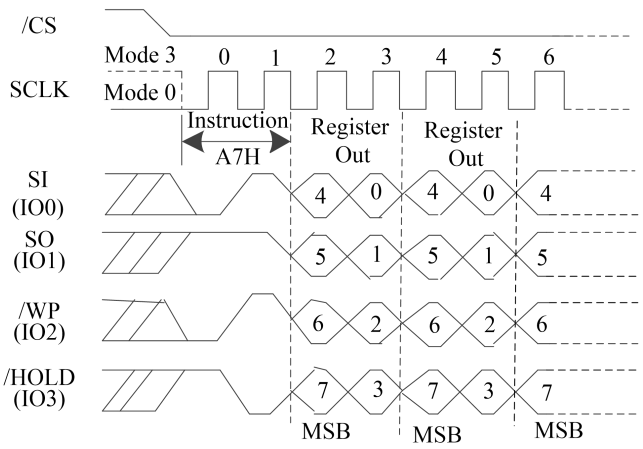


Figure 174. Read SPB Lock Register (QPI Mode)



7.5.5 Read SPB Status (E2H)

The Read SPB Status (E2h) instruction reads the status of the SPB of a sector or block. The Solid Protection Bits (SPBs) are non-volatile bits for enabling or disabling write-protection to sectors and blocks. An SPB is assigned to each 4KB sector in the bottom and top 64KB of memory and to each 64KB block in the remaining memory. The factory default state of the SPB bits is “0”, which has the block/sector write-protection disabled.

The Read SPB Status instruction returns 00h if the SPB is “0”, indicating write-protection is disabled. The Read SPB Status instruction returns FFh if the SPB is “1”, indicating write-protection is enabled.

See ***Figure 175-Figure 178***, to read out the SPB Bit value of a specific block or sector, the Read SPB Status (E2h) instruction must be issued by driving /CS low, shifting the instruction code “E2h” into the Data Input (SI or IO0-IO3) pin on the rising edge of CLK, followed by a 24/32-bit address. In QPI mode, the number of dummy clocks can be configured by the “Set Read Parameters (C0h)” instruction. The SPB Bit value will be shifted out on the SO or IO0-IO3 pin at the falling edge of CLK with most significant bit (MSB) first as shown in Figure, and then driving /CS high. Please note that if not driven /CS high, the SPB Bit value will be repeatedly output.

Figure 175. Read SPB Status (SPI Mode/3-Byte Address Mode)

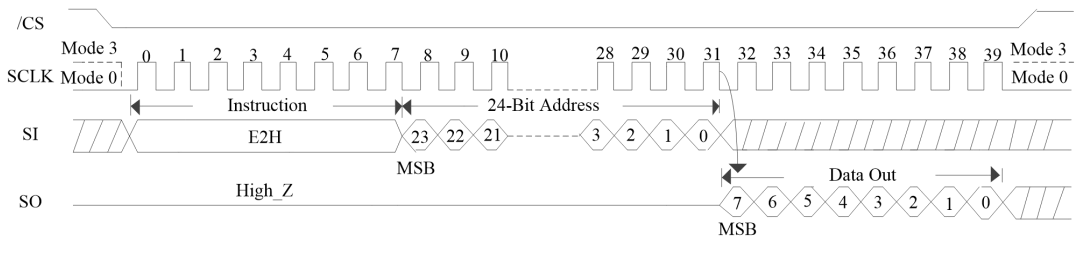


Figure 176. Read SPB Status (SPI Mode/4-Byte Address Mode)

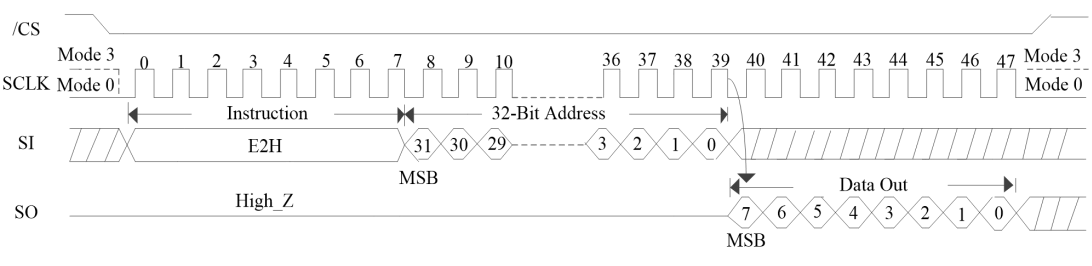


Figure 177. Read SPB Status (QPI Mode/3-Byte Address Mode)

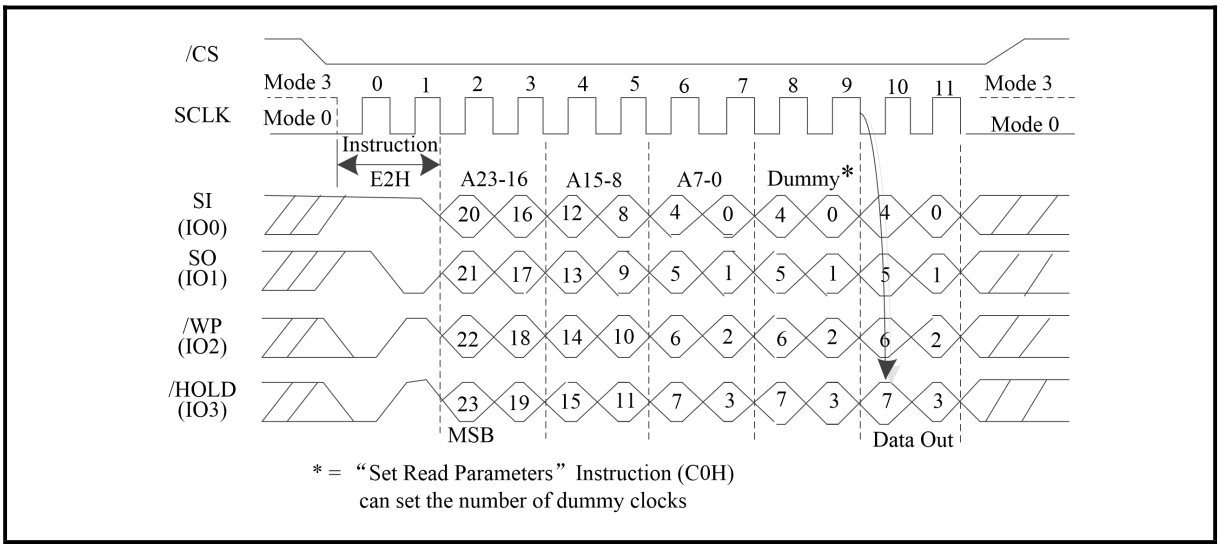
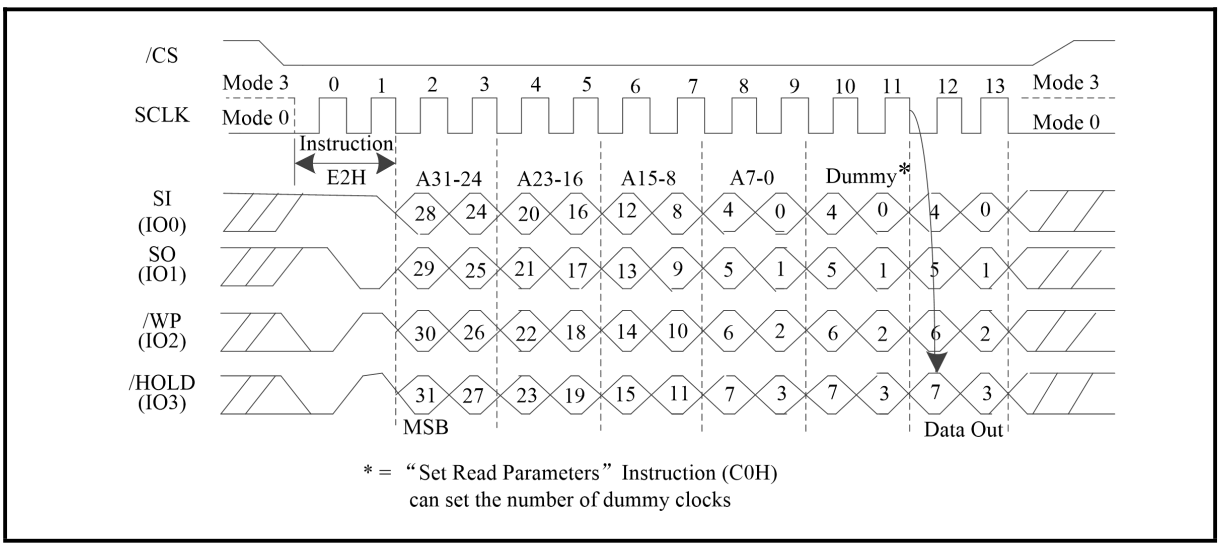


Figure 178. Read SPB Status (QPI Mode/4-Byte Address Mode)



7.5.6 SPB Program (E3H)

The SPB Program (E3h) instruction set SPBs to "1". SPBs can be individually set to "1" by the SPB Program instruction. The Solid Protection Bits (SPBs) are non-volatile bits for enabling or disabling write-protection to sectors and blocks. An SPB is assigned to each 4KB sector in the bottom and top 64KB of memory and to each 64KB block in the remaining memory. The factory default state of the SPB bits is "0", which has the block/sector write-protection disabled. When an SPB is set to "1", the associated sector or block is write-protected. Program and erase operations on the sector or block will be inhibited.

The SPB Lock Bit must be "1" before any SPB can be modified. In Solid Protection mode the SPB Lock Bit defaults to "1" after power-on or reset. Under Password Protection mode, the SPB Lock Bit defaults to "0" after power-on or reset, and a Password Unlock instruction with a correct password is required to set the SPB Lock Bit to "1".

A Write Enable (06h) instruction must be executed to set the WEL bit before sending the SPB Program instruction.

See ***Figure 179-Figure 182***, to set SPB to "1", the SPB Program (E3h) instruction must be issued by driving /CS low, shifting the instruction code "E3h" into the Data Input (SI or IO0-IO3) pin on the rising edge of CLK, followed by a 24/32-bit address, and then driving /CS high.

Figure 179. SPB Program (SPI Mode/3-Byte Address Mode)

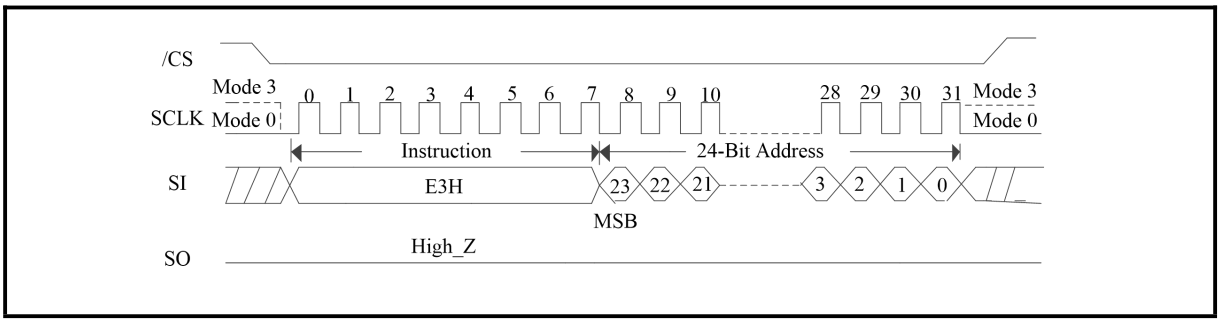


Figure 180. SPB Program (SPI Mode/4-Byte Address Mode)

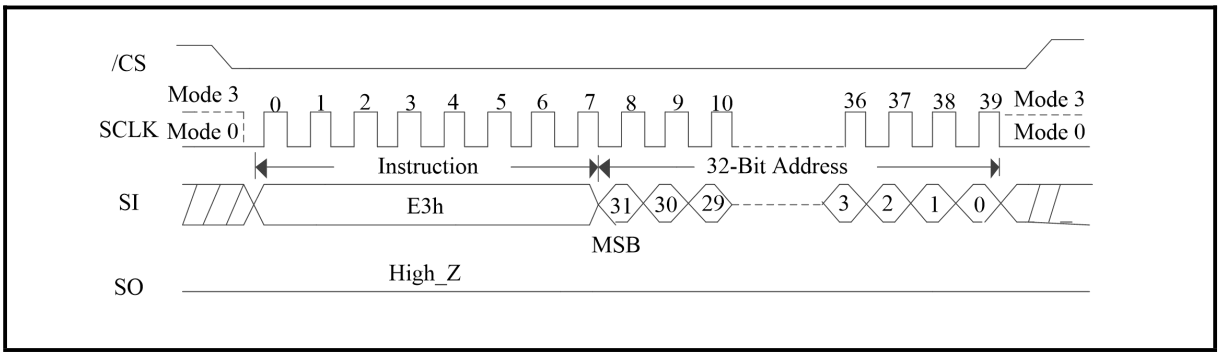


Figure 181. SPB Program (QPI Mode/3-Byte Address Mode)

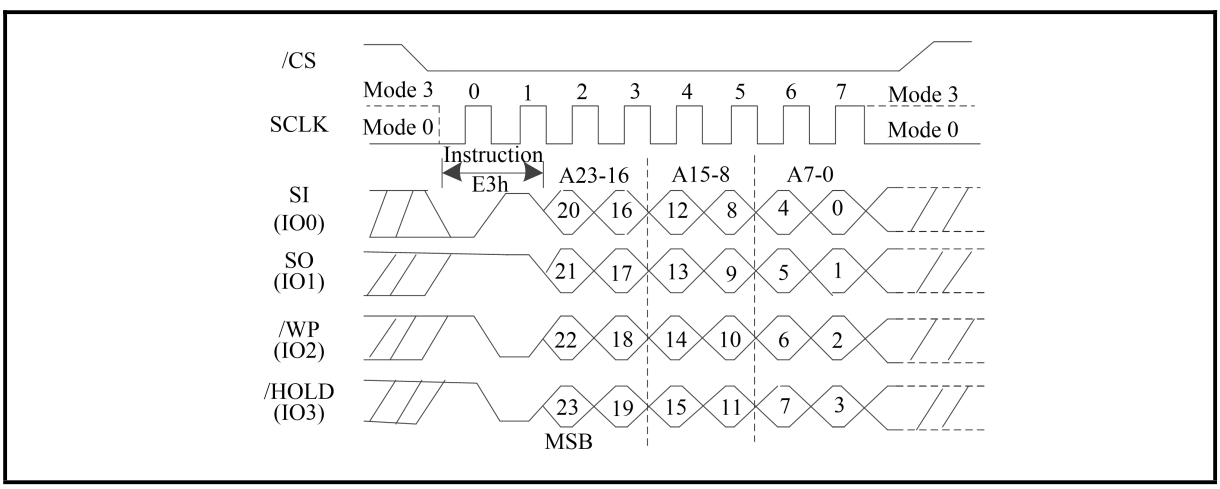
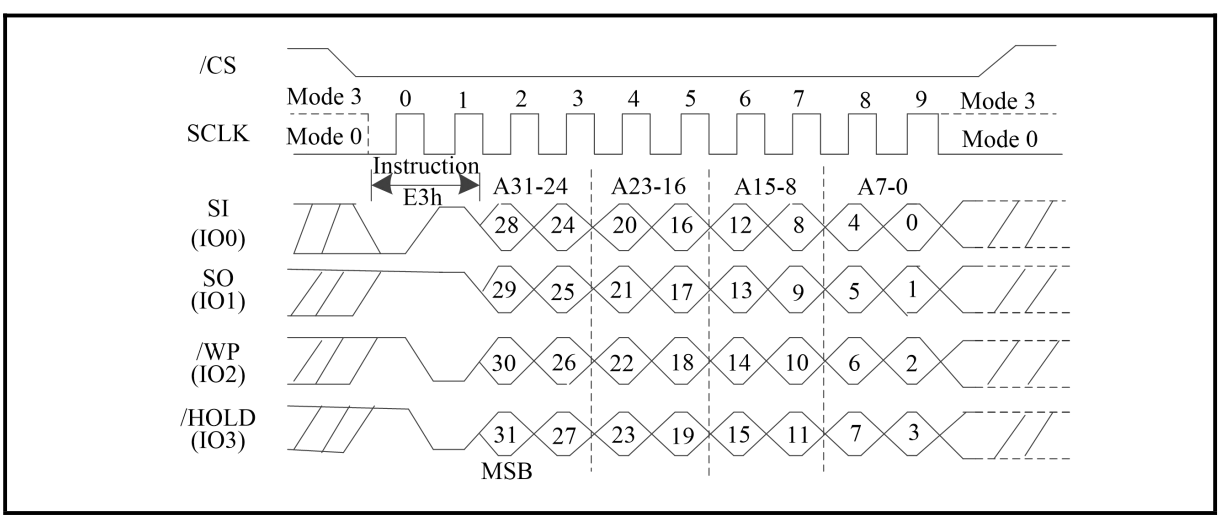


Figure 182. SPB Program (QPI Mode/4-Byte Address Mode)



7.5.7 SPB Erase (E4H)

The SPB Erase (E4h) instruction clears all SPBs to “0”. The SPBs cannot be individually cleared to “0”. The SPB Lock Bit must be “1” before any SPB can be modified. In Solid Protection mode the SPB Lock Bit defaults to “1” after power-on or reset. Under Password Protection mode, the SPB Lock Bit defaults to “0” after power-on or reset, and a Password Unlock instruction with a correct password is required to set the SPB Lock Bit to “1”.

A Write Enable (06h) instruction must be executed to set the WEL bit before sending the SPB Erase instruction.

See ***Figure 183-Figure 184***, to clear all SPBs to “0”, the SPB Erase (E4h) instruction must be issued by driving /CS low, shifting the instruction code “E4h” into the Data Input (SI or IO0-IO3), and then driving /CS high.

Figure 183. SPB Erase (SPI Mode)

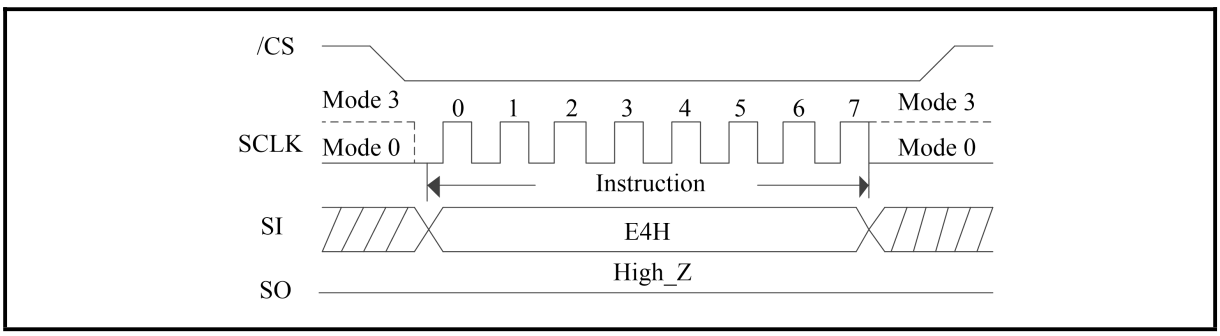
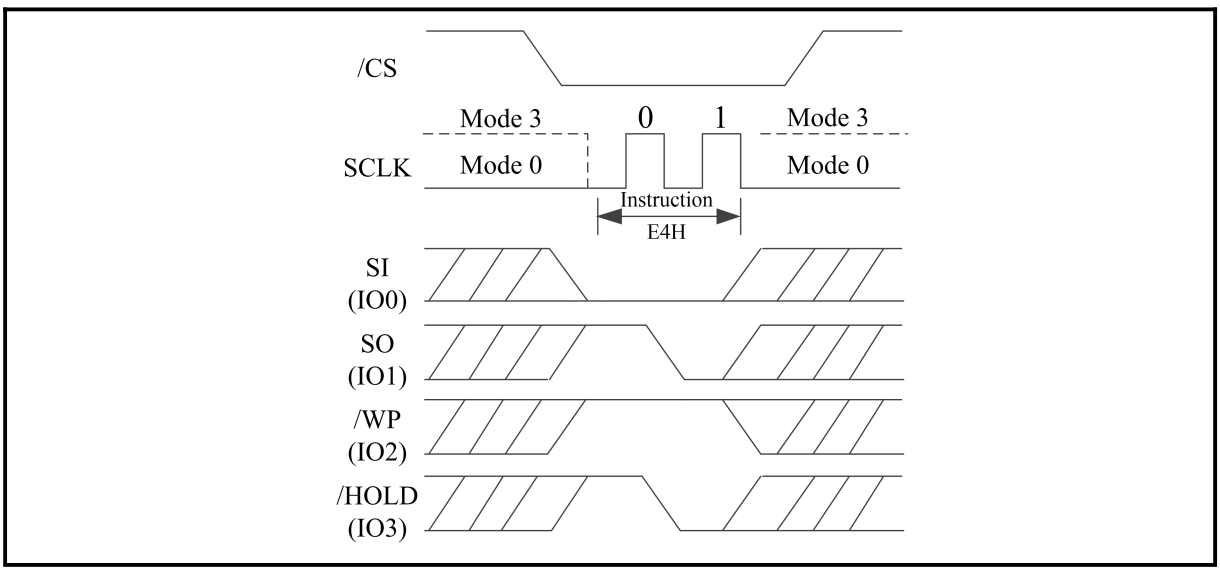


Figure 184. SPB Erase (QPI Mode)



7.5.8 Read DPB Status (3DH)

The Read DPB Status (3Dh) instruction reads the status of the DPB of a sector or block. The Read DPB Status instruction returns 00h if the DPB is “0”, indicating write-protection is disabled. The Read DPB Status instruction returns FFh if the DPB is “1”, indicating write-protection is enabled.

The Dynamic Protection Bits (DPBs) are volatile bits for quickly and easily enabling or disabling write-protection to sectors and blocks. A DPB is assigned to each 4KB sector in the bottom and top 64KB of memory and to each 64KB block in the rest of the memory. When a DPB is “1”, the associated sector or block will be write-protected, preventing any program or erase operation on the sector or block. All DPBs default to “1” after power-on or reset. When a DPB is cleared to “0”, the associated sector or block will be unprotected if the corresponding SPB is also “0”.

See ***Figure 185-Figure 188***, to read out the DPB Bit value of a specific block or sector, the Read DPB Status (3Dh) instruction must be issued by driving /CS low, shifting the instruction code “3Dh”

into the Data Input (SI or IO0-IO3) pin on the rising edge of CLK, followed by a 24/32-bit address. The DPB Bit value will be shifted out on the SO or IO0-IO3 pin at the falling edge of CLK with most significant bit (MSB) first as shown in Figure, and then driving /CS high. Please note that if not driven /CS high, the DPB Bit value will be repeatedly output.

Figure 185. Read DPB Status (SPI Mode/3-Byte Address Mode)

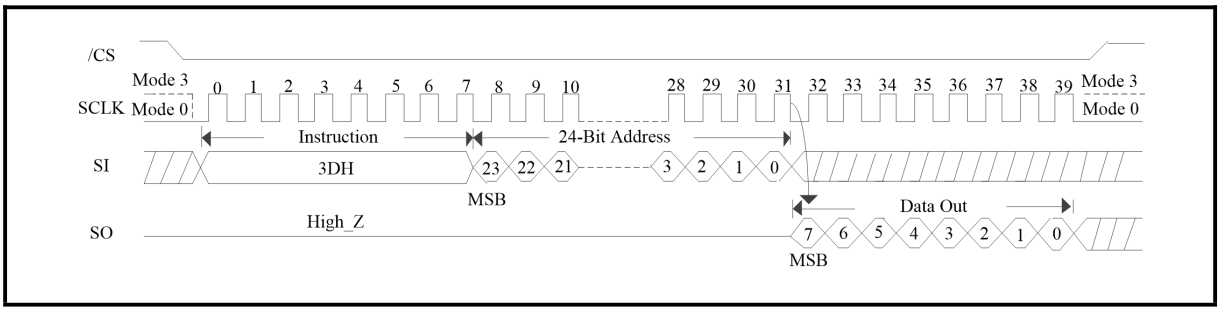


Figure 186. Read DPB Status (SPI Mode/4-Byte Address Mode)

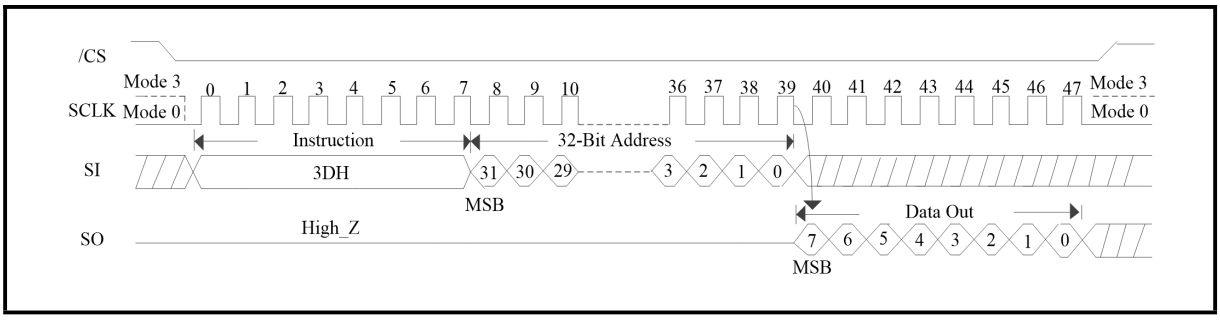


Figure 187. Read DPB Status (QPI Mode/3-Byte Address Mode)

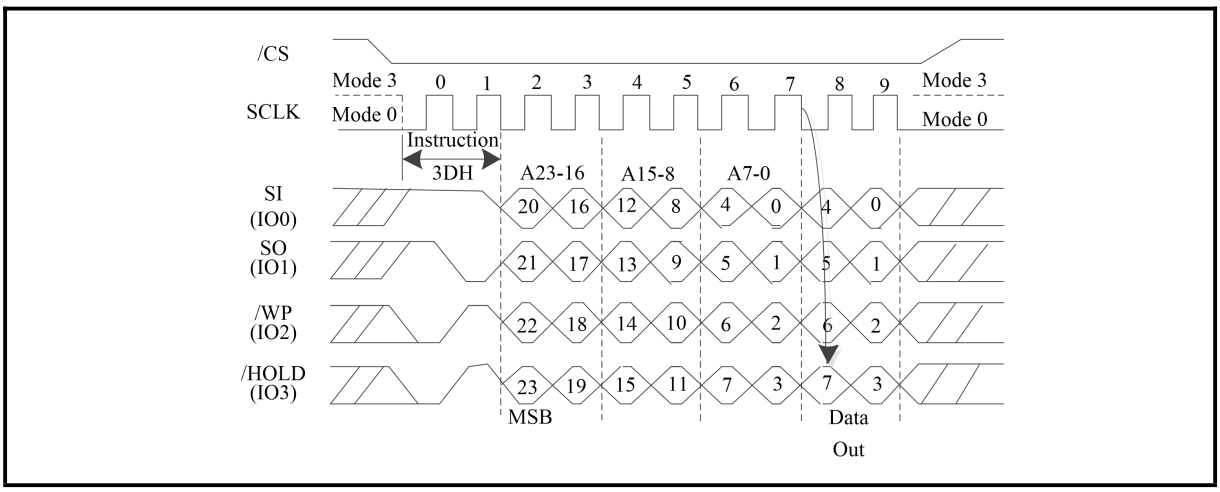
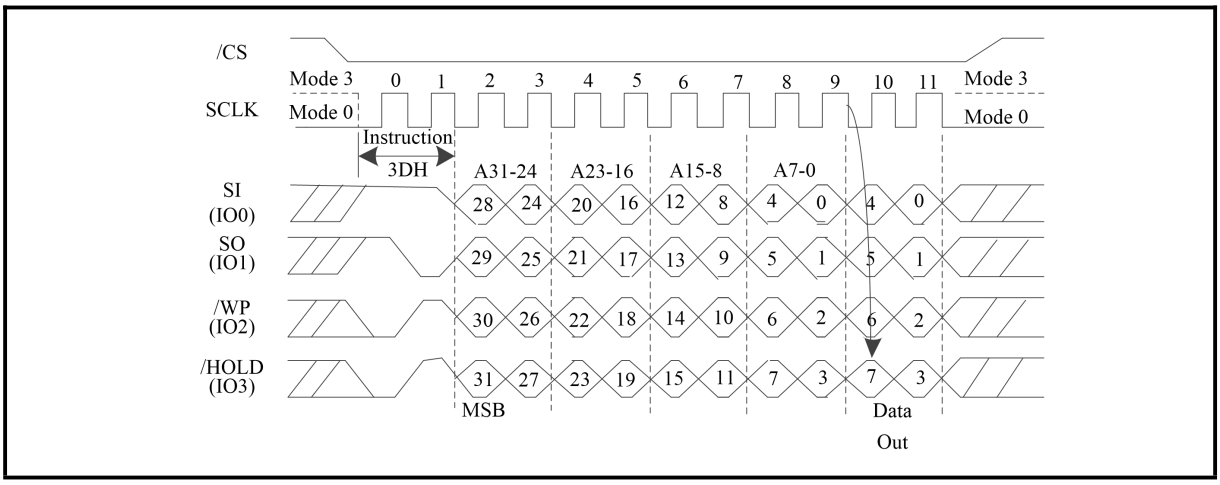


Figure 188. Read DPB Status (QPI Mode/4-Byte Address Mode)



7.5.9 Dynamic Protection Block/Sector Lock (36H)

The Dynamic Protection Block/Sector Lock (36h) instruction can individually set DPB bits to “1”. When a DPB is “1”, the associated sector or block will be write-protected, preventing any program or erase operation on the sector or block. All DPBs default to “1” after power-on or reset. When a DPB is cleared to “0”, the associated sector or block will be unprotected if the corresponding SPB is also “0”.

A Write Enable (06h) instruction must be executed to set the WEL bit before sending the Dynamic Protection Block/Sector Lock instruction.

See ***Figure 189-Figure 192***, to set DPB to “1”, the Dynamic Protection Block/Sector Lock (36h) instruction must be issued by driving /CS low, shifting the instruction code “36h” into the Data Input (SI or IO0-IO3) pin on the rising edge of CLK, followed by a 24/32-bit address, and then driving /CS high.

Figure 189. Dynamic Protection Block/Sector Lock (SPI Mode/3-Byte Address Mode)

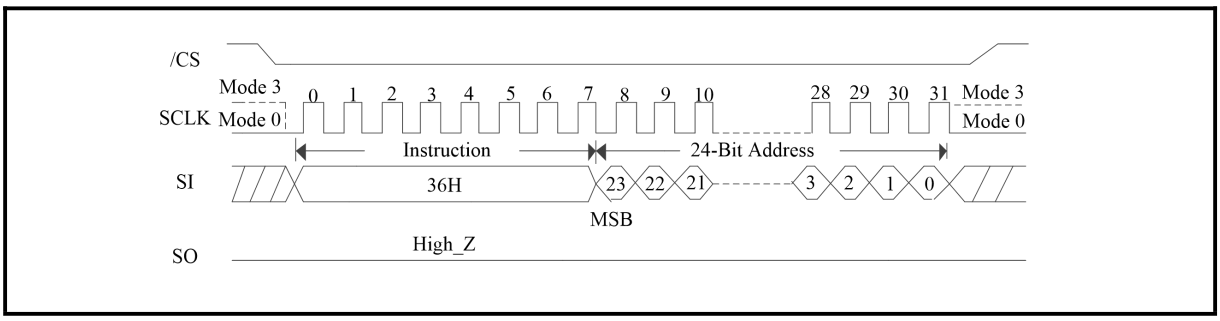


Figure 190. Dynamic Protection Block/Sector Lock (SPI Mode/4-Byte Address Mode)

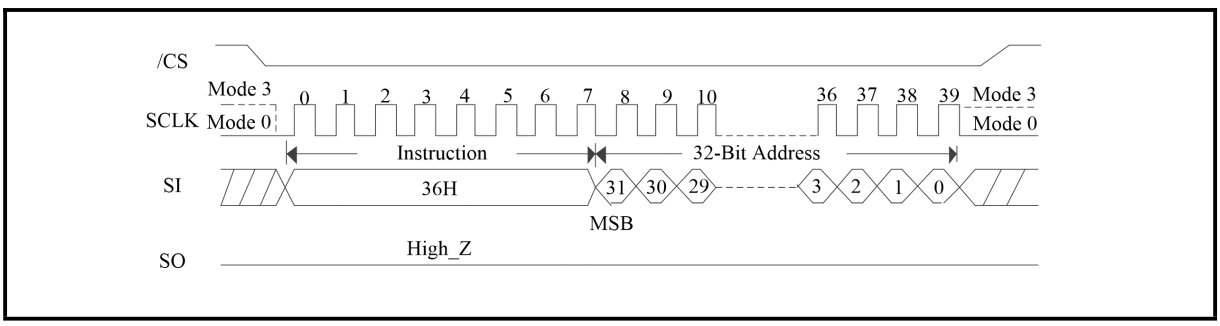


Figure 191. Dynamic Protection Block/Sector Lock (QPI Mode/3-Byte Address Mode)

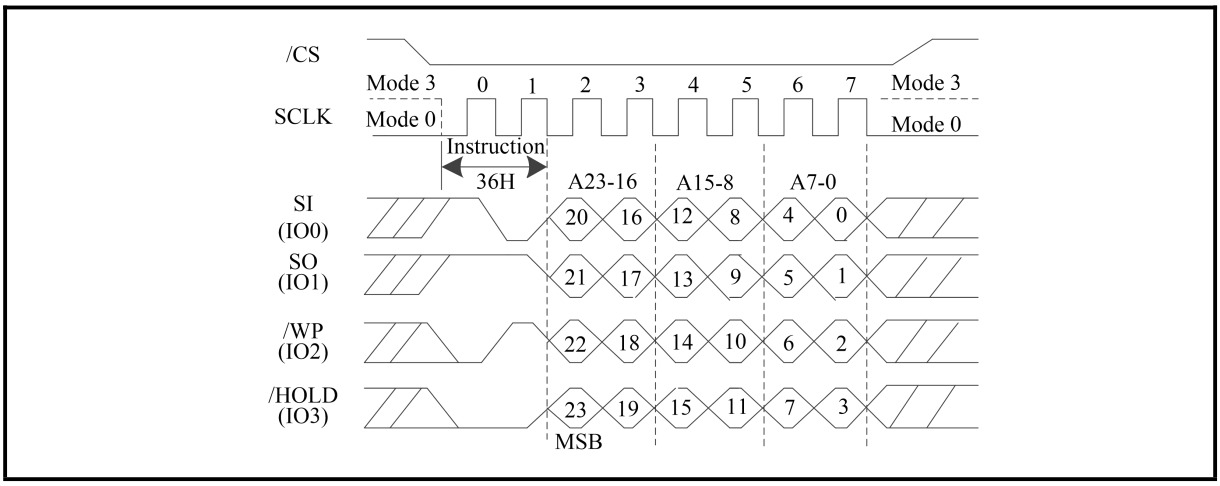
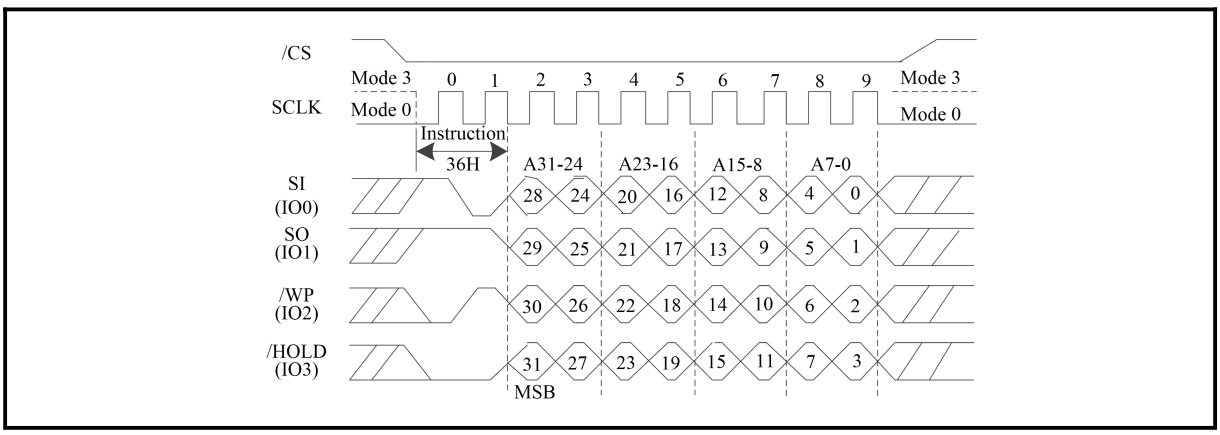


Figure 192. Dynamic Protection Block/Sector Lock (QPI Mode/4-Byte Address Mode)



7.5.10 Dynamic Protection Block/Sector Unlock (39H)

The Dynamic Protection Block/Sector Unlock (39h) instruction can individually set DPB bits to “0”. When a DPB is cleared to “0”, the associated sector or block will be unprotected if the corresponding SPB is also “0”.

A Write Enable (06h) instruction must be executed to set the WEL bit before sending the Dynamic Protection Block/Sector Unlock instruction.

See ***Figure 193-Figure 196***, to set DPB to “0”, the Dynamic Protection Block/Sector Unlock (39h) instruction must be issued by driving /CS low, shifting the instruction code “39h” into the Data Input (SI or IO0-IO3) pin on the rising edge of CLK, followed by a 24/32-bit address, and then driving /CS high.

Figure 193. Dynamic Protection Block/Sector Unlock (SPI Mode/3-Byte Address Mode)

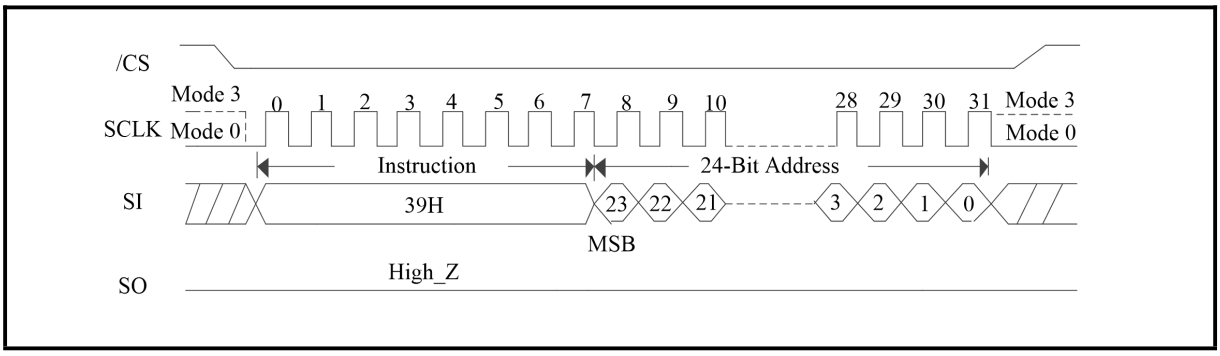


Figure 194. Dynamic Protection Block/Sector Unlock (SPI Mode/4-Byte Address Mode)

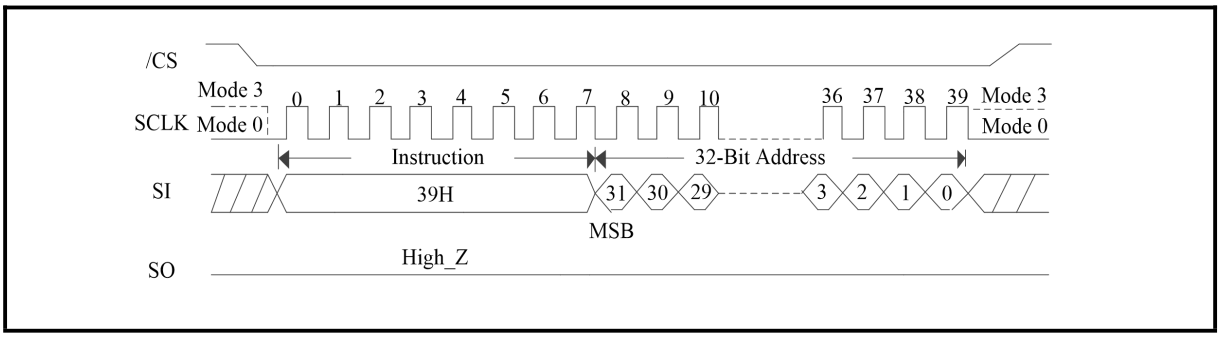


Figure 195. Dynamic Protection Block/Sector Unlock (QPI Mode/3-Byte Address Mode)

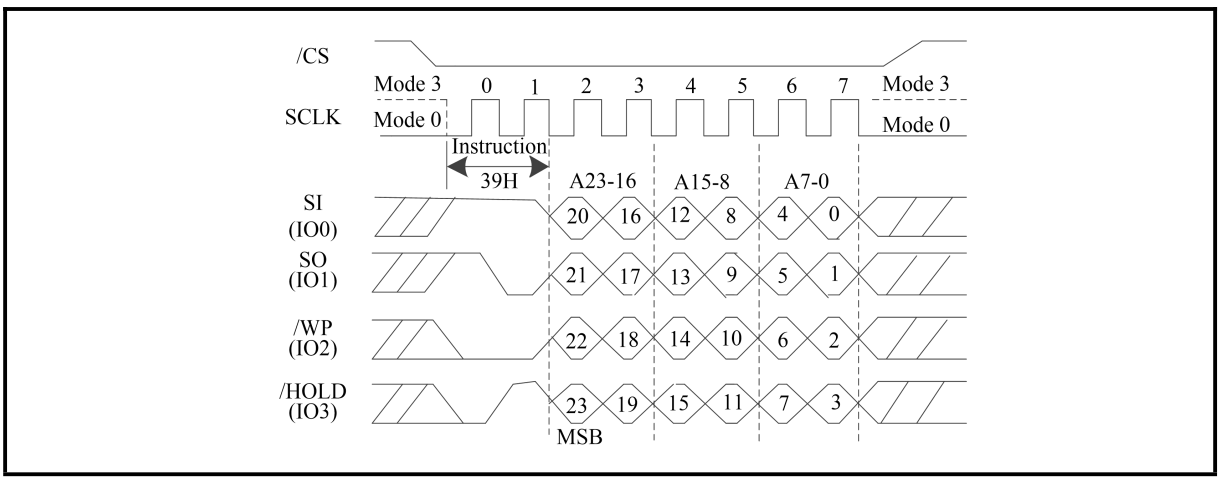
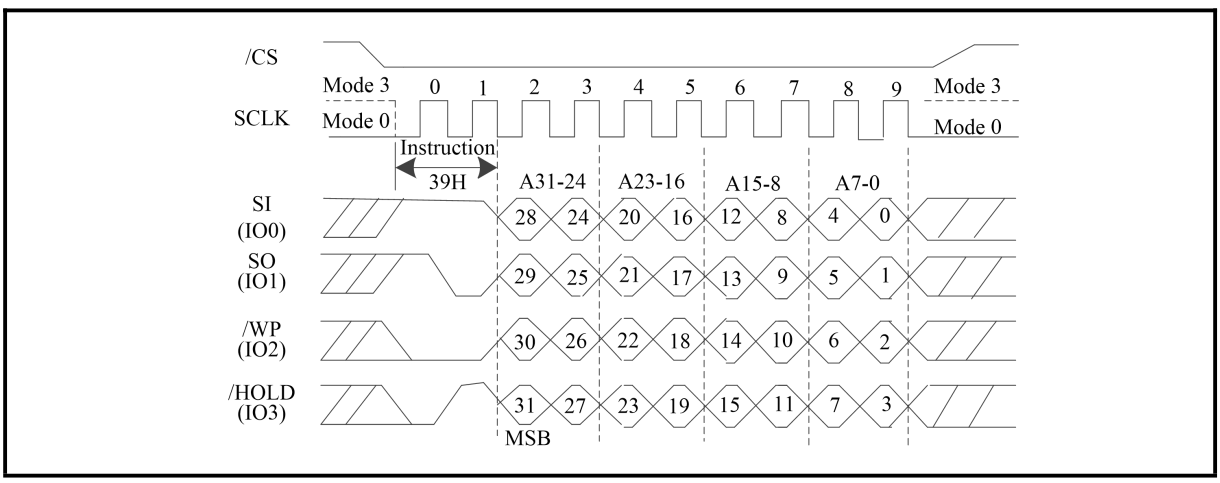


Figure 196. Dynamic Protection Block/Sector Unlock (QPI Mode/4-Byte Address Mode)



7.5.11 Read Unprotect Solid Protect Bit (AAH)

The Read Unprotect Solid Protect Bit (AAh) instruction can read the value of Unprotect Solid Protect Bit. The Unprotect Solid Protect Bit is a volatile bit that defaults to “1” after power-on or reset. When USPB=1, the SPBs have their normal function. When USPB=0 all SPBs are masked and their write-protected sectors and blocks are temporarily unprotected (as long as their corresponding DPBs are “0“).

The USPB can be read, set or cleared as often as needed in Solid Protection mode or after providing a valid password in Password Protection mode.

See ***Figure 197-Figure 198***, to read out the bit value of the Unprotect Solid Protect Bit, the Read Unprotect Solid Protect Bit (AAh) instruction must be issued by driving /CS low, shifting the instruction code “AAh” into the Data Input (SI or IO0-IO3) pin on the rising edge of CLK. The

Unprotect Solid Protect Bit value will be shifted out on the SO or IO0-IO3 pin at the falling edge of CLK with most significant bit (MSB) first.

Figure 197. Read Unprotect Solid Protect Bit (SPI Mode)

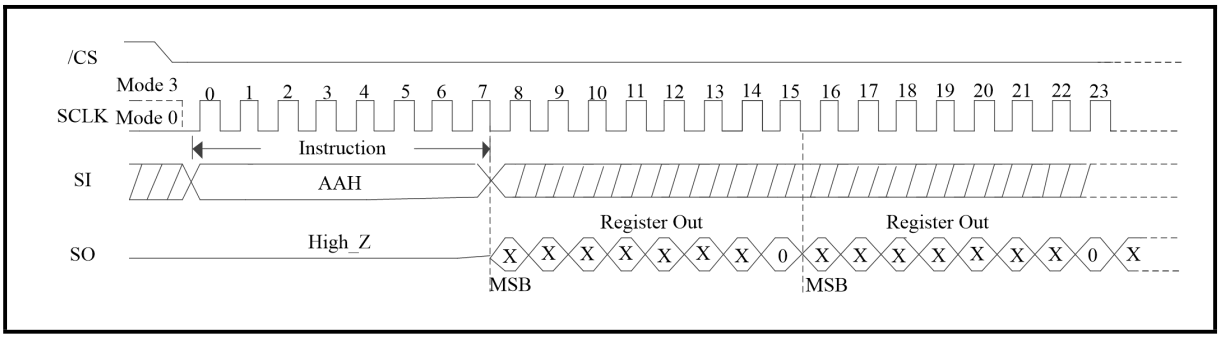
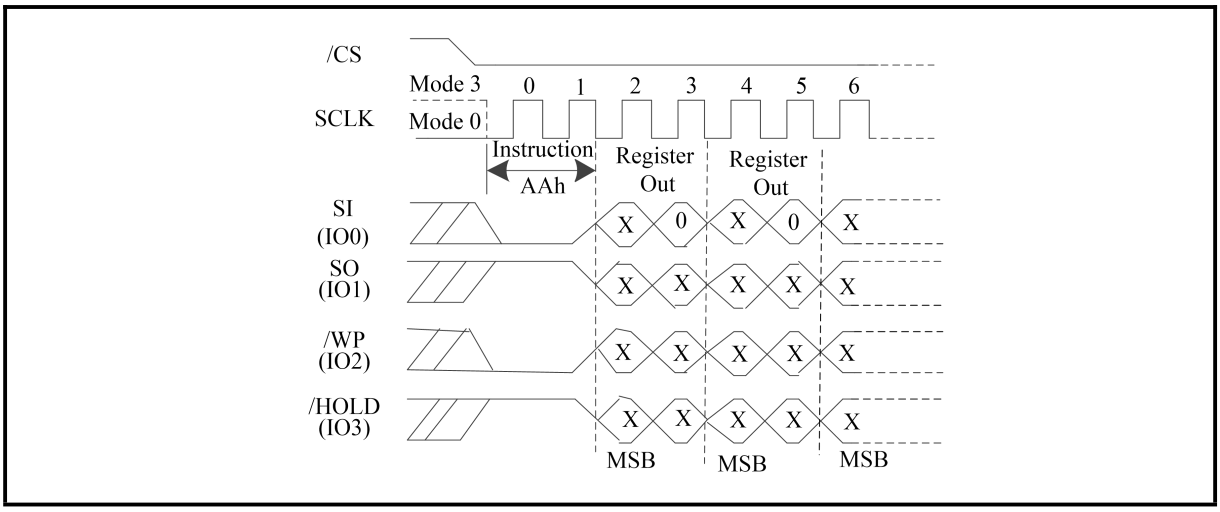


Figure 198. Read Unprotect Solid Protect Bit (QPI Mode)



7.5.12 Unprotect Solid Protect Bit Set (A8H)

The Unprotect Solid Protect Bit Set (A8h) instruction can set the Unprotect Solid Protect Bit can be to 1. The Unprotect Solid Protect Bit is a volatile bit that defaults to “1” after power-on or reset. When USPB=1, the SPBs have their normal function. When USPB=0 all SPBs are masked and their write-protected sectors and blocks are temporarily unprotected (as long as their corresponding DPBs are “0“).

The USPB can be read, set or cleared as often as needed in Solid Protection mode or after providing a valid password in Password Protection mode.

A Write Enable (06h) instruction must be executed to set the WEL bit before sending the Unprotect Solid Protect Bit Set instruction.

See ***Figure 199-Figure 200***, the instruction must be issued by driving /CS low, shifting the instruction code “A8h” into the Data Input (SI or IO0-IO3) pin on the rising edge of CLK, and then driving /CS high.

Figure 199. Unprotect Solid Protect Bit Set (SPI Mode)

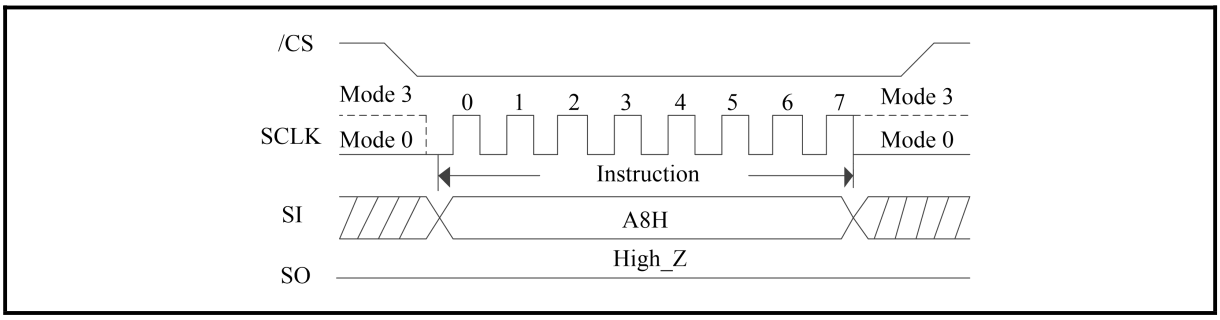
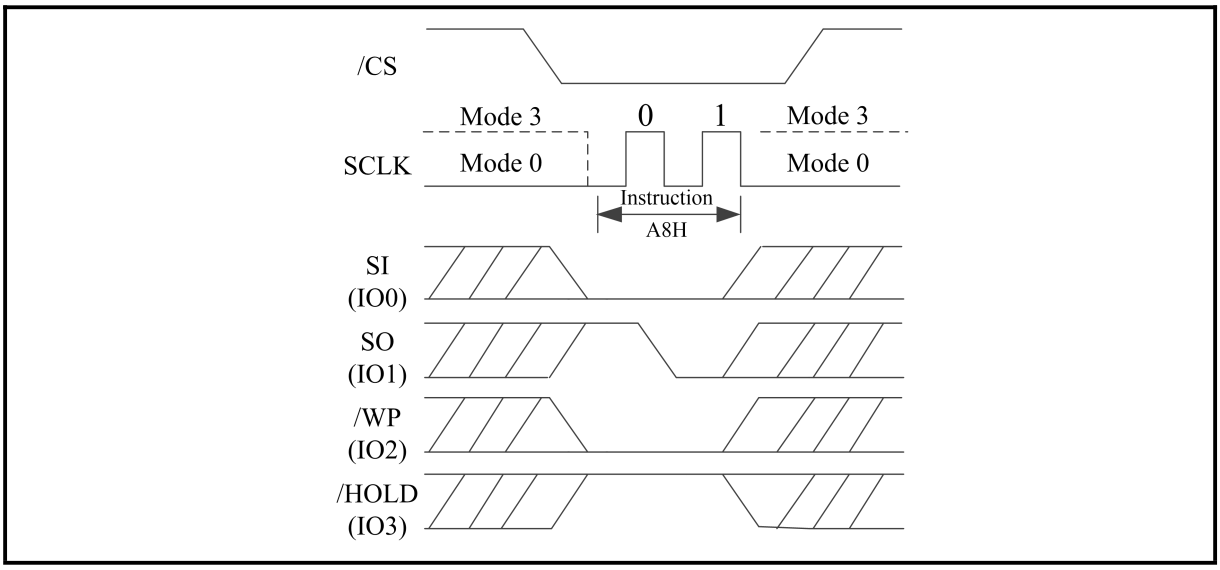


Figure 200. Unprotect Solid Protect Bit Set (QPI Mode)



7.5.13 Unprotect Solid Protect Bit Clear (A9H)

The Unprotect Solid Protect Bit Clear (A9h) instruction can set the Unprotect Solid Protect Bit to 0. The Unprotect Solid Protect Bit is a volatile bit that defaults to “1” after power-on or reset. When USPB=1, the SPBs have their normal function. When USPB=0 all SPBs are masked and their write-protected sectors and blocks are temporarily unprotected (as long as their corresponding DPBs are “0“).

The USPB can be read, set or cleared as often as needed in Solid Protection mode or after providing a valid password in Password Protection mode.

A Write Enable (06h) instruction must be executed to set the WEL bit before sending the Unprotect Solid Protect Bit Clear instruction.

See ***Figure 201-Figure 202***, the instruction must be issued by driving /CS low, shifting the instruction code “A9h” into the Data Input (SI or IO0-IO3) pin on the rising edge of CLK, and then driving /CS high.

Figure 201. Unprotect Solid Protect Bit Clear (SPI Mode)

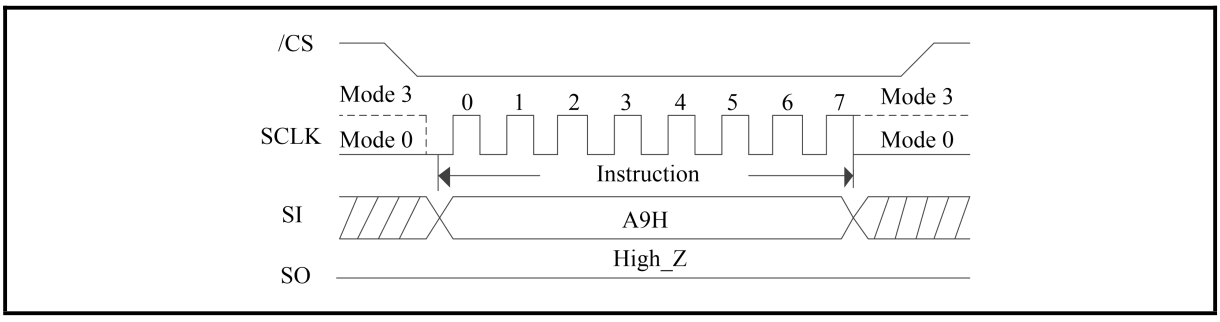
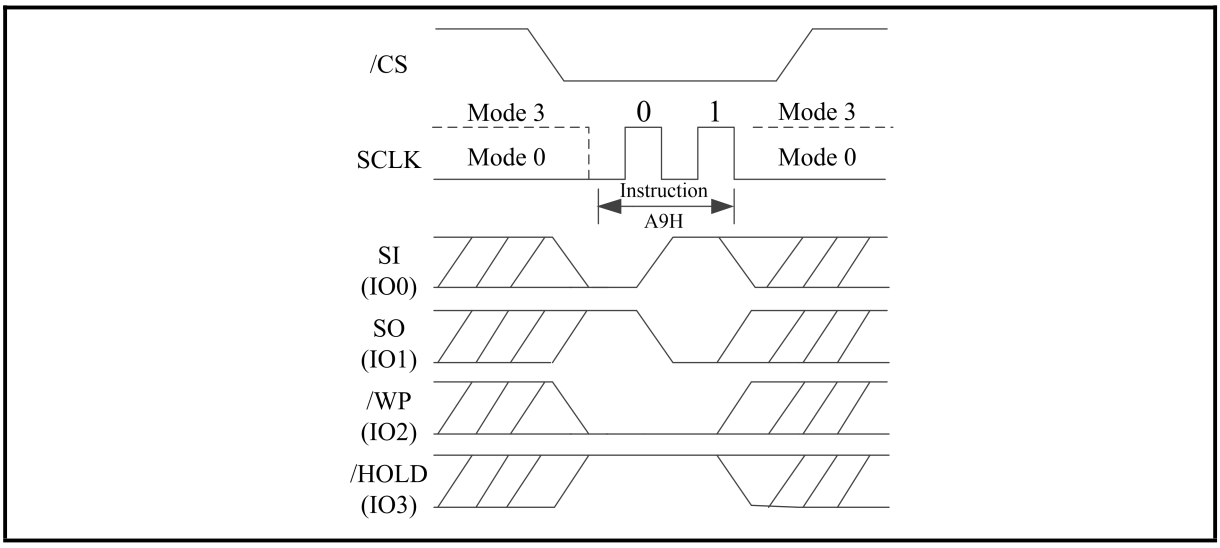


Figure 202. Unprotect Solid Protect Bit Clear (QPI Mode)



7.5.14 Global Block/Sector Lock (7Eh)

The Global Block/Sector Lock (7Eh) instruction can set all Dynamic Protection Bits (DPBs) to 1.

A Write Enable (06h) instruction must be executed to set the WEL bit before sending the Global Block/Sector Lock instruction.

See ***Figure 203-Figure 204***, to set all DPBs to "1", the Global Block/Sector Lock (7Eh) instruction must be issued by driving /CS low, shifting the instruction code "7Eh" into the Data Input (SI or IO0-IO3) pin on the rising edge of CLK, and then driving /CS high.

Figure 203. Global Block/Sector Lock (SPI Mode)

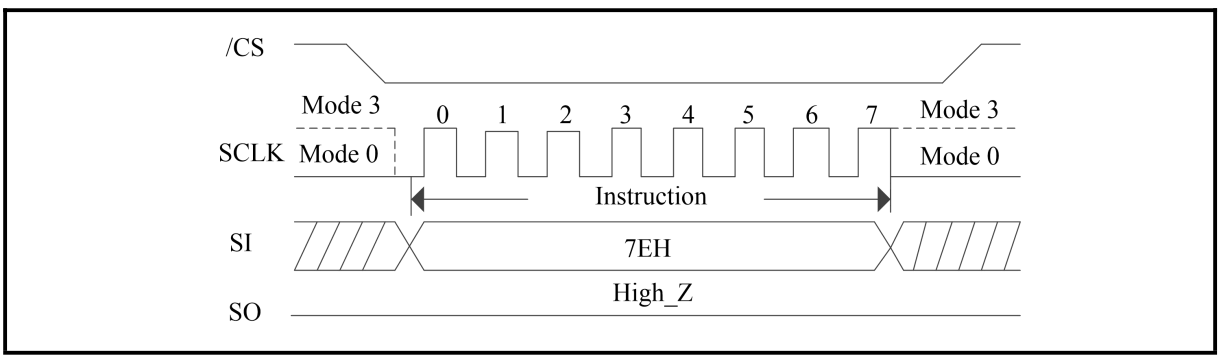
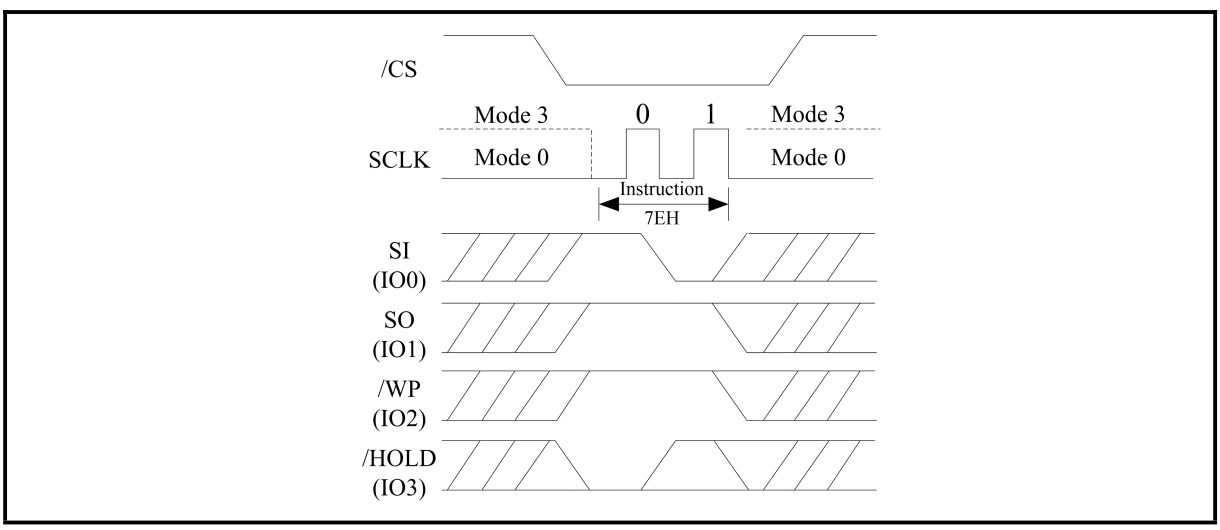


Figure 204. Global Block/Sector Lock (QPI Mode)



7.5.15 Global Block/Sector Unlock (98h)

The Global Block/Sector Unlock (98h) instruction can set all Dynamic Protection Bits (DPBs) to 0.

A Write Enable (06h) instruction must be executed to set the WEL bit before sending the Global Block/Sector Unlock instruction.

See ***Figure 205-Figure 206***, to set all DPBs "0", the Global Block/Sector Unlock (98h) instruction must be issued by driving /CS low, shifting the instruction code "98h" into the Data Input (SI or IO0-IO3) pin on the rising edge of CLK, and then driving /CS high.

Figure 205. Global Block/Sector Unlock (SPI Mode)

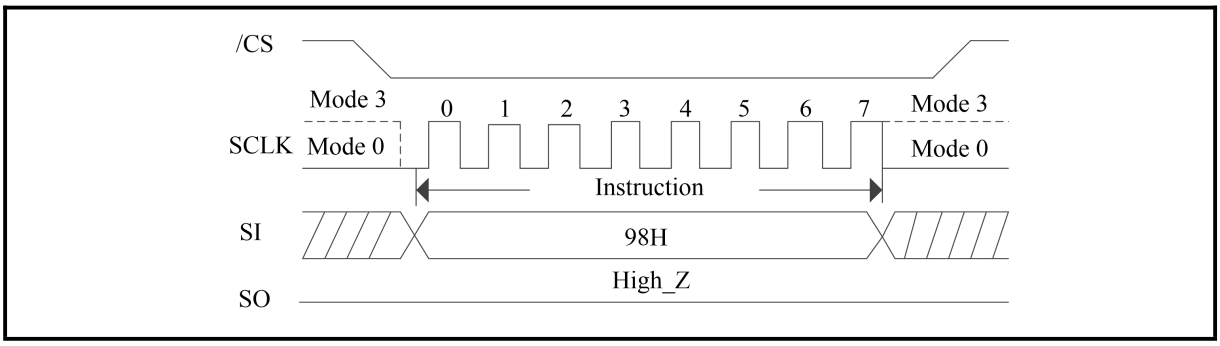
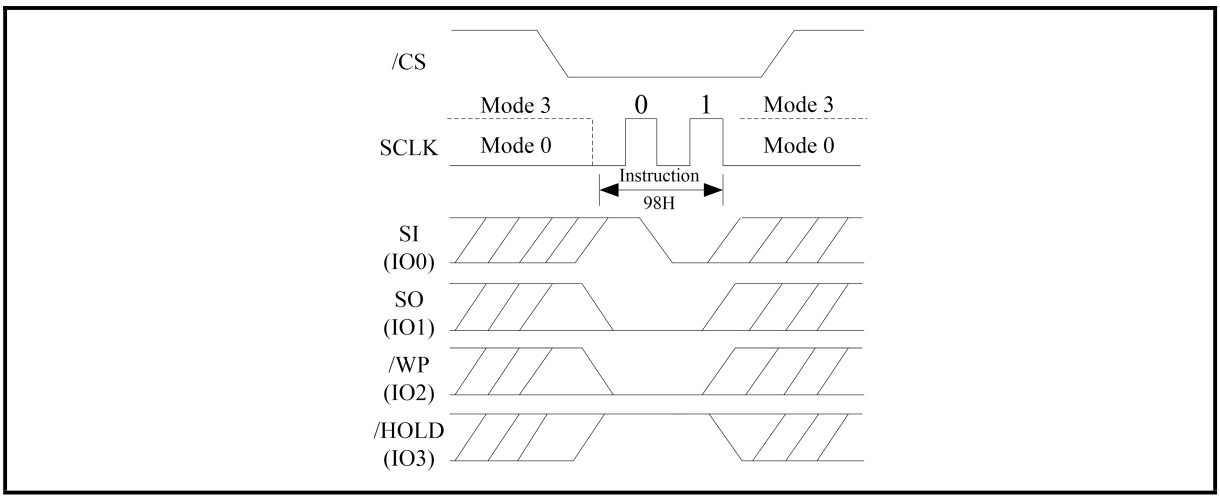


Figure 206. Global Block/Sector Unlock (QPI Mode)



7.5.16 Read Password Register (27H)

The Read Password Register (27H) instruction can reads back the 64-bit password. Password Protection mode potentially provides a higher level of security than Solid Protection mode.

See ***Figure 207-Figure 208***, to reads back the password, the Read Password Register (27H) instruction must be issued by driving /CS low, shifting the instruction code "27h" into the Data Input (SI or IO0-IO3) pin on the rising edge of CLK. The 64-bit password will be shifted out on the SO or IO0-IO3 pin at the falling edge of CLK with most significant bit (MSB) first as shown in Figure.

Figure 207. Read Password Register (SPI Mode)

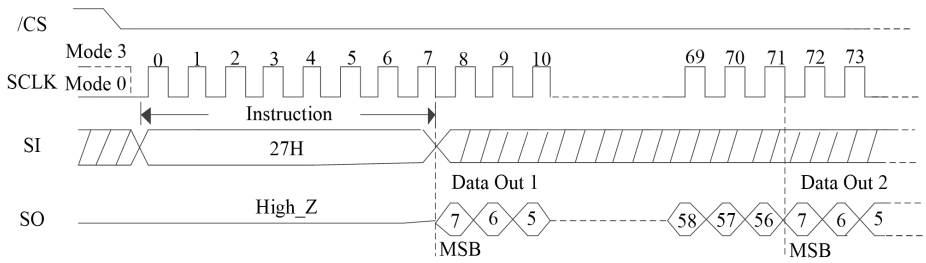
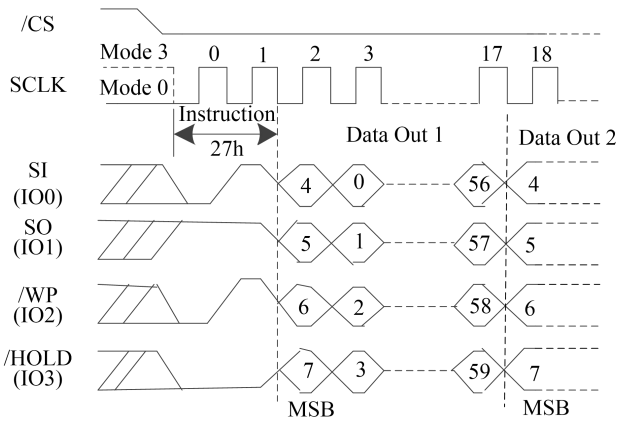


Figure 208. Read Password Register (QPI Mode)



7.5.17 Write Password Register (28H)

The Write Password Register (28H) instruction writes the password. The Password Protection mode potentially provides a higher level of security than Solid Protection mode.

A Write Enable (06h) instruction must be executed to set the WEL bit before sending the Write Password Register instruction.

See ***Figure 209-Figure 210***, to write the password, the Write Password Register (28H) instruction must be issued by driving /CS low, shifting the instruction code “28h” into the Data Input (SI or IO0-IO3) pin on the rising edge of CLK followed by the 64-bit password, and then driving /CS high.

Figure 209. Write Password Register (SPI Mode)

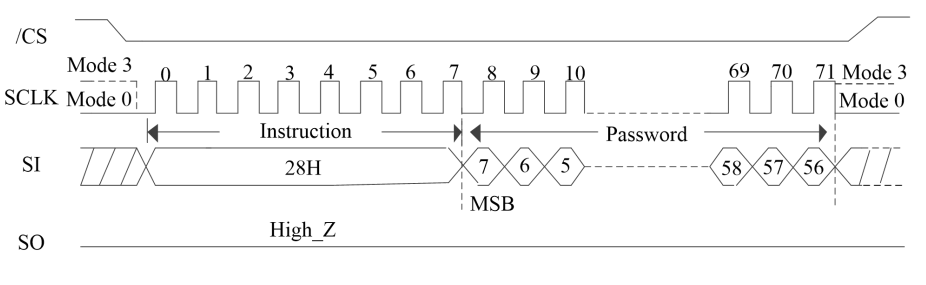
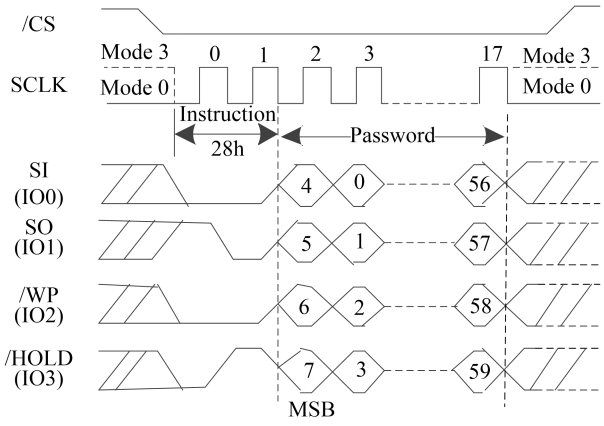


Figure 210. Write Password Register (QPI Mode)



7.5.18 Password Unlock (29H)

The Password Unlock (29H) instruction with the correct password will set the SPB Lock Bit to "1" and unlock the SPB bits.

Password Protection mode potentially provides a higher level of security than Solid Protection mode. In Password Protection mode, the SPB Lock Bit defaults to "0" after a power-on cycle or reset. When SPB Lock Bit=0, the SPBs are locked and cannot be modified. A 64-bit password must be provided to unlock the SPBs. After the correct password is given, a wait of 2us is necessary for the SPB bits to unlock. The Status Register WIP bit will clear to "0" upon completion of the Password Unlock instruction. Once unlocked, the SPB bits can be modified.

A Write Enable (06h) instruction must be executed to set the WEL bit before sending the Password Unlock instruction.

See ***Figure 211-Figure 212***, to give the correct password, the Password Unlock (29H) instruction must be issued by driving /CS low, shifting the instruction code "29h" into the Data Input (SI or IO0-IO3) pin on the rising edge of CLK followed by the 64-bit password, and then driving /CS high.

Figure 211. Password Unlock (SPI Mode)

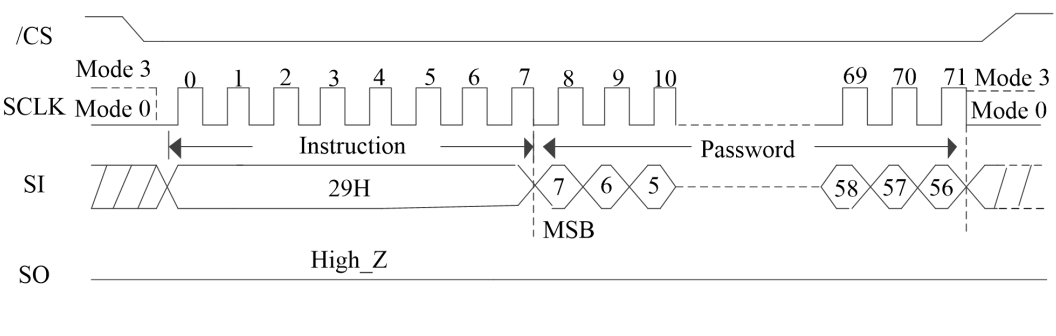
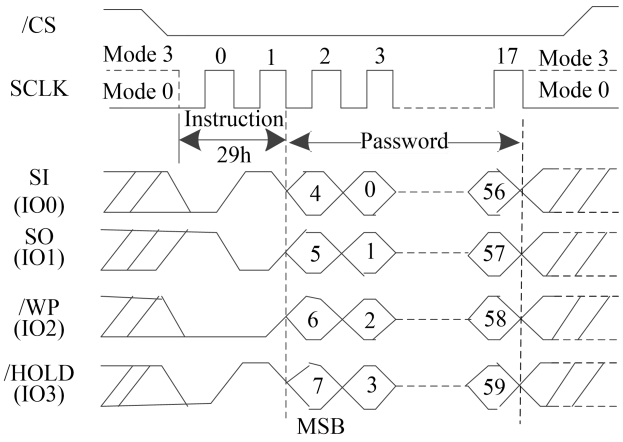


Figure 212. Password Unlock (QPI Mode)



8. Electrical Characteristics

8.1 Absolute Maximum Ratings

Parameter	Symbol	Conditions	Range	Unit.
Supply Voltage	VCC		–0.5 to 4	V
Voltage Applied to Any Pin	VIO	Relative to Ground	–0.5 to 4	V
Transient Voltage on any Pin	VIOT	<20nS Transient Relative to Ground	–2.0V to VCC+2.0V	V
Storage Temperature	TSTG		–65 to +150	°C
Electrostatic Discharge Voltage	VESD	Human Body Model(1)	–2000 to +2000	V

Notes:

1.JEDEC Std JESD22-A114 (C1=100pF, R1=1500 ohms, R2=500 ohms)

8.2 Operating Ranges

Parameter	Symbol	Conditions	Spec		Unit.
			Min	Max	
Supply Voltage	VCC		2.7	3.6	V
Temperature Operating	TA	Commercial	-40	+85	°C
		Industrial	-40	+85	

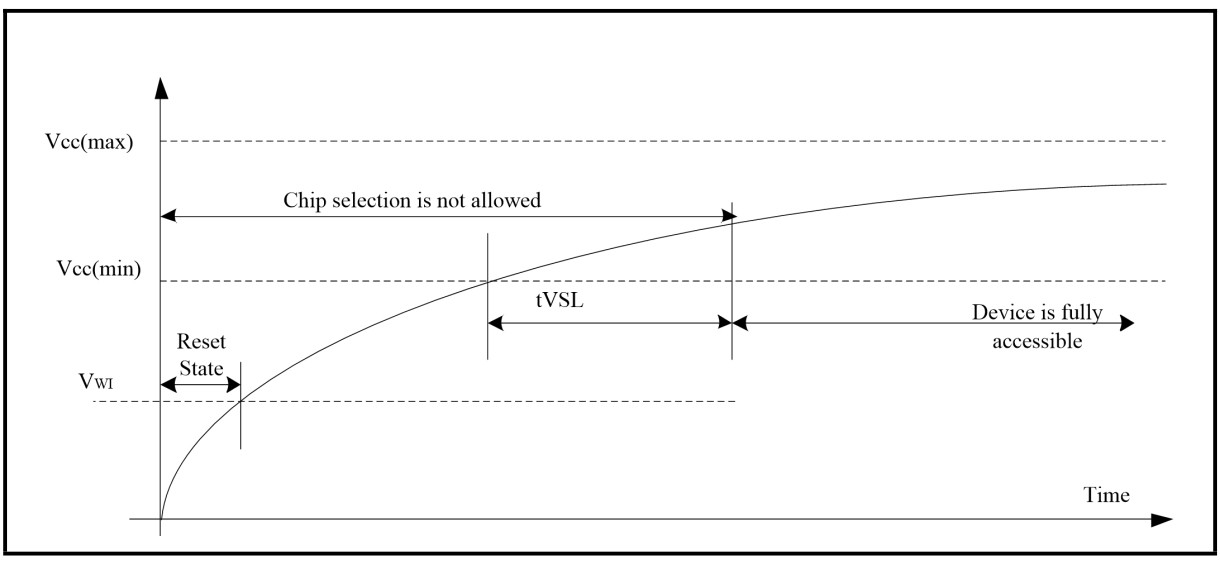
8.3 Latch Up Characteristics

Parameter	Min	Max
Input Voltage Respect To VSS On I/O Pins	-1.0V	VCC+1.0V
VCC Current	-100mA	100mA

8.4 Power-up Timing

Symbol	Parameter	Min	Max	Unit.
tVSL	VCC(min) To /CS Low	300		us
V_{WI}	Write Inhibit Threshold Voltage V_{WI}	1.9	2.3	V

Figure 213. Power-up Timing and Voltage Levels



8.5 DC Electrical Characteristics

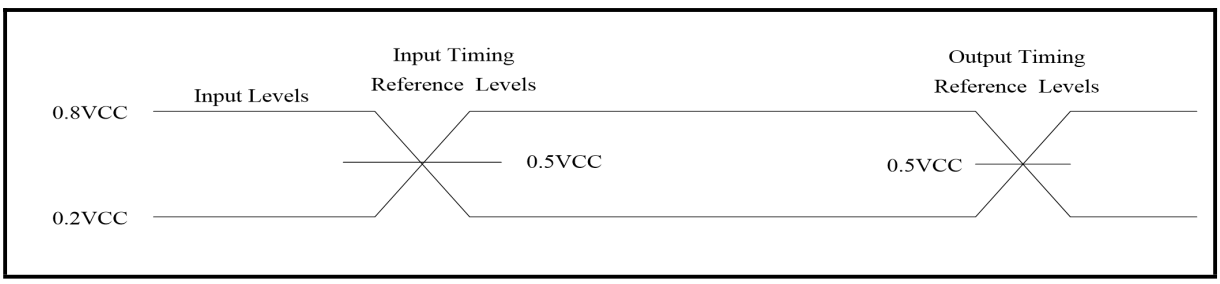
(T= -40℃~85℃, VCC=2.7~3.6V)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
ILI	Input Leakage Current				±2	μA
ILO	Output Leakage Current				±2	μA
ICC1	Standby Current	/CS=VCC, VIN=VCC or VSS		112	480	μA
ICC2	Deep Power-Down Current	/CS=VCC, VIN=VCC or VSS		8	60	μA
ICC3	Operating Current: (Read)	SCLK=0.1VCC/ 0.9VCC, at 120MHz,Q=Open(*1,*,2*4 I/O)		15	20	mA
		SCLK=0.1VCC/ 0.9VCC, at 80MHz,Q=Open(*1,*,2*4 I/O)		13	18	mA
ICC4	Operating Current(Page Program)	/CS=VCC			15	mA
ICC5	Operating Current(WRSR)	/CS=VCC			5	mA
ICC6	Operating Current(Sector Erase)	/CS=VCC			20	mA
ICC7	Operating Current(Block Erase)	/CS=VCC			20	mA
ICC8	Operating Current (Chip Erase)	/CS=VCC			20	mA
VIL	Input Low Voltage		-0.5		0.2VCC	V
VIH	Input High Voltage		0.8VCC		VCC+0.4	V
VOL	Output Low Voltage	IOL =100μA			0.4	V
VOH	Output High Voltage	IOH =-100μA	VCC-0.2			V

8.6 AC Measurement Conditions

Symbol	Parameter	Min	Tpy.	Max	Unit.	Conditions
CL	Load Capacitance			30	pF	
TR, TF	Input Rise And Fall time			5	ns	
VIN	Input Pause Voltage	0.2VCC to 0.8VCC			V	
IN	Input Timing Reference Voltage	0.5VCC			V	
OUT	Output Timing Reference Voltage	0.5VCC			V	

Figure 214. AC Measurement I/O Waveform



8.7 AC Electrical Characteristics

(T= -40℃~85℃, VCC=2.7~3.6V)

Symbol	Parameter	Min.	Typ.	Max.	Unit.
Fc	Clock frequency for all instructions, except Read Data instruction (03H) & Read Data instruction with 4-Byte Address (13H) & Read SPB Status instruction (E2H) & DTR instructions, on 3.0 - 3.6V power supply	DC.		100	MHz
Fc	Clock frequency for all instructions, except Read Data instruction (03H) & Read Data instruction with 4-Byte Address (13H) & Read SPB Status instruction (E2H) & DTR instructions, on 2.7-2.9V power supply	DC.		80	MHz
fR	Clock freq. for Read Data instruction (03H), Read Data instruction with 4-Byte Address (13H) and Read SPB Status instruction (E2H)	DC.		55	MHz
F_R	Clock freq. for DTR instructions	DC.		54	MHz
tCLH	Serial Clock High Time	4			ns
tCLL	Serial Clock Low Time	4			ns
tCLCH	Serial Clock Rise Time (Slew Rate)	0.1(1)			V/ns
tCHCL	Serial Clock Fall Time (Slew Rate)	0.1(1)			V/ns
tSLCH	/CS Active Setup Time	5			ns
tCHSH	/CS Active Hold Time	5			ns
tSHCH	/CS Not Active Setup Time	5			ns
tCHSL	/CS Not Active Hold Time	5			ns

Symbol	Parameter	Min.	Typ.	Max.	Unit.
tSHSL	/CS High Time（read/write）	20			ns
tSHQZ	Output Disable Time			6	ns
tCLQX	Output Hold Time	0			ns
tDVCH	Data In Setup Time	2			ns
tCHDX	Data In Hold Time	2			ns
tHLCH	/Hold Low Setup Time (relative to Clock)	5			ns
tHHCH	/Hold High Setup Time (relative to Clock)	5			ns
tCHHL	/Hold High Hold Time (relative to Clock)	5			ns
tCHHH	/Hold Low Hold Time (relative to Clock)	5			ns
tHLQZ	/Hold Low To High-Z Output			6	ns
tHHQX	/Hold Low To Low-Z Output			6	ns
tCLQV	Clock Low To Output Valid			7	ns
tWHSL	Write Protect Setup Time Before /CS Low	20			ns
tSHWL	Write Protect Hold Time After /CS High	100			ns
tDP	/CS High To Deep Power-Down Mode			20	μs
tRES1	/CS High To Standby Mode Without Electronic Signature Read			20	μs
tRES2	/CS High To Standby Mode With Electronic Signature Read			20	μs
tESL	Erase Suspend Latency			30	μs
tPSL	Program Suspend Latency			30	μs
tPS	Latency between Program and next Suspend	20			μs
tES	Latency between Erase and next Suspend	20			μs
tPRS	Latency between Program Resume and next Suspend	20			μs
tERS	Latency between Erase Resume and next Suspend	20			μs
tRST	/CS High To Next Instruction After Reset			300	μs
tW	Write Status Register Cycle Time		5	30(2)	ms
tBP1	Byte Program Time (First Byte) (2)		30	50	μs
tBP2	Additional Byte Program Time (After First Byte) (2)		2.5	12	μs
tPP	Page Programming Time		0.6	2.4	ms
tSE	Sector Erase Time		50	300	ms
tBE	Block Erase Time(32K Bytes/64K Bytes)		0.15/0.25	1.6/2	S
tCE	Chip Erase Time(Single Die BY25Q256FS)		80	120	S
tPW1	Latency between providing the correct password and the WIP=0		2		μs
tPW2	Latency between providing the incorrect password and the WIP=0	80	100	120	μs

Notes:
1. Tested with clock frequency lower than 50 MHz.
2. For multiple bytes after first byte within a page, tBPn = tBP1 + tBP2 * N, where N is the number of bytes programmed.

Figure 215. Serial input Timing

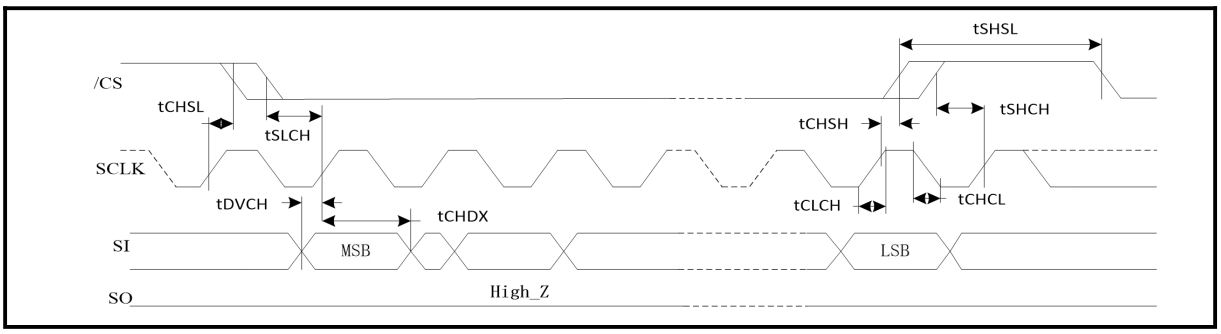


Figure 216. Output Timing

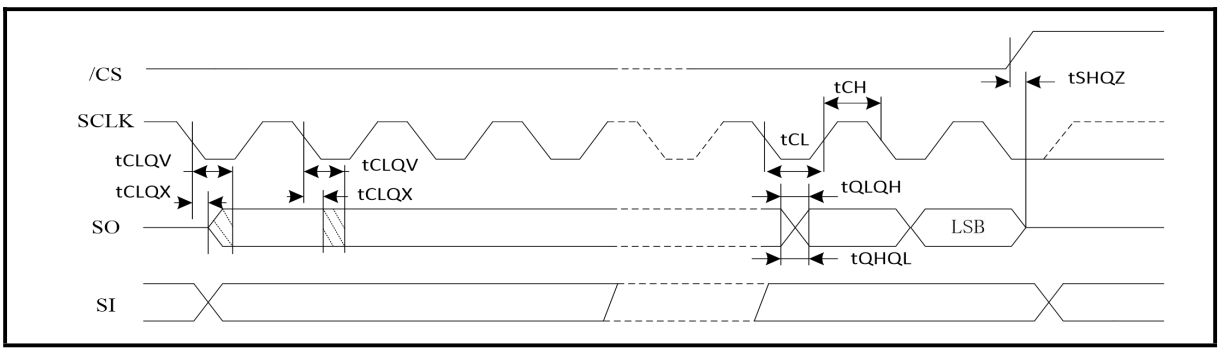


Figure 217. Hold Timing

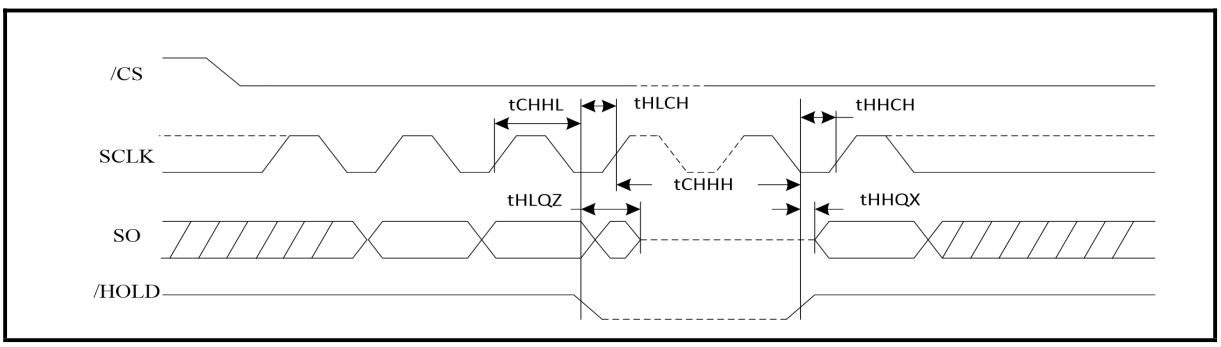
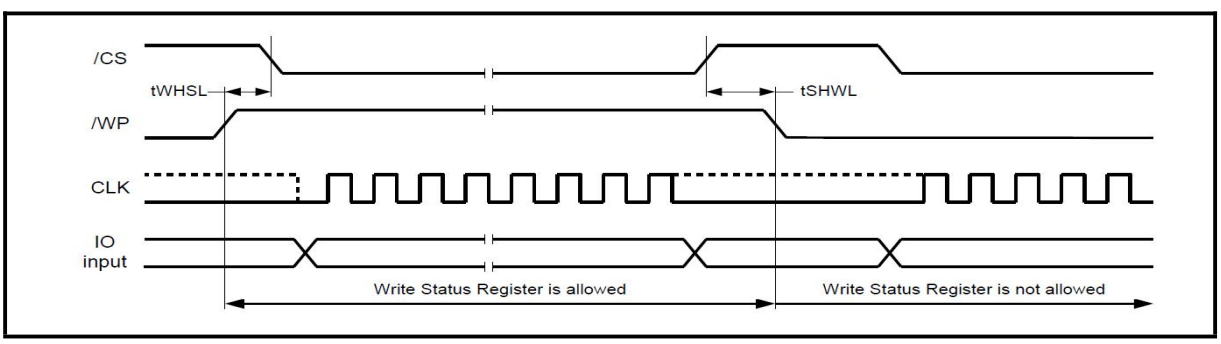
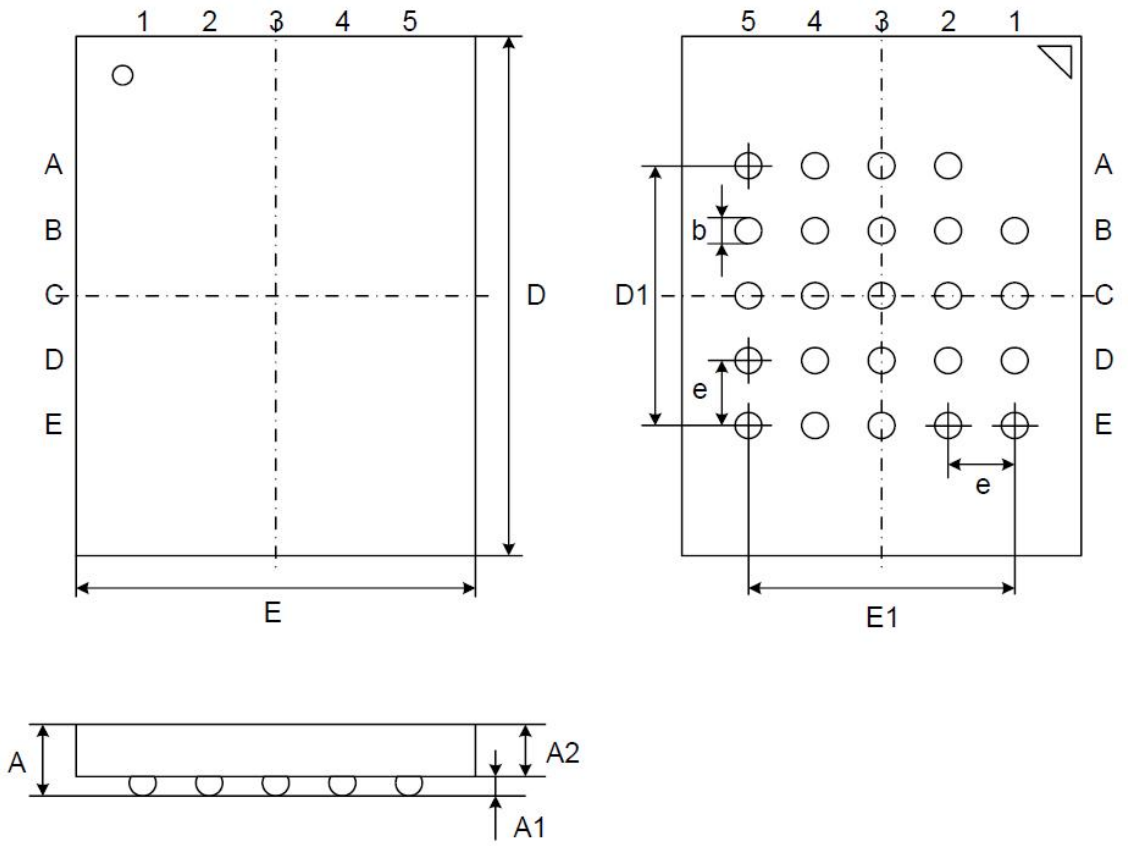


Figure 218. /WP Timing



9. Package Information

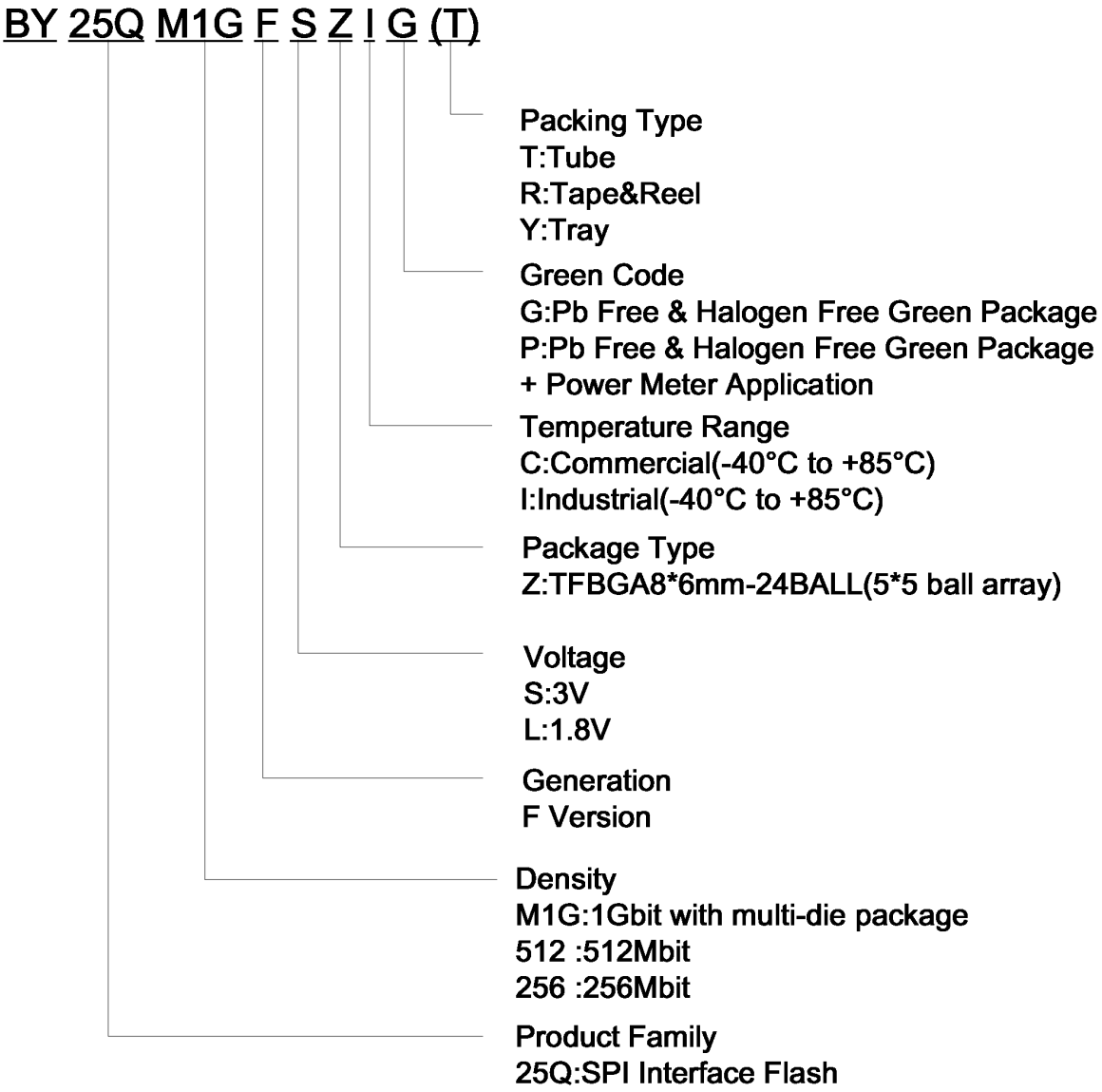
9.1 Package TFBGA8*6mm-24BALL (5*5 ball array)



Dimensions

Symbol / Unit		A	A1	A2	b	E	E1	D	D1	e
mm	Min	-	0.20	0.75	0.35	5.90	4.00	7.90	4.00	1.00
	Nom	-	0.25	0.85	0.40	6.00		8.00		
	Max	1.20	0.37	0.93	0.45	6.10		8.10		

10. Order Information



10.1 Valid part Numbers and Top Side Marking

The following table provides the valid part numbers for BY25QM1GFS SPI Flash Memory. Pls contact BY Technology for specific availability by density and package type.

For consumer and industry application:

Package Type	Density	Product Number	Top Side Marking
Z TFBGA8*6mm-24BALL (5*5 ball array)	1G-bit	BY25QM1GFSZIG	Boya 25QM1GFSZIG YYWW

10.2 Minimum Packing Quantity (MPQ)

Package Type	Packing Type	Qty for 1 Tube or Reel	Vacuum bag/ Inner Box	MPQ
TFBGA8*6mm-24BALL (5*5 ball array)	Tray	377ea/Tray	10+1 Trays/Bag 1Bag/InnerBox	3,770

11. Document Change History

REVISION	CHANGE DESCRIPTION	CLAUSE	ORIGINATOR DATE
1.0	Initiate; Based on BY25Q512FS_v1.1;	/	Zuohuan Yu 2019-11-21
1.1	Add Chinese feature descriptions; Remove SOP16 package type;	/	Zuohuan Yu 2019-11-22
1.2	Add XIP (execute in place) Operation description;	/	Zuohuan Yu 2019-11-26
1.3	Change device ID	/	Zuohuan Yu 2019-11-29
1.4	Add TFBGA24 package	/	Zuohuan Yu 2020-7-16
1.5	Modify Data Retention and Endurance	/	Zuohuan Yu 2020-7-21
1.6	Rename part number as BY25QM1GFS	/	Zuohuan Yu 2020-9-1
1.7	Update Standby Icc and DeepPowerDown Icc spec	/	Zuohuan Yu 2020-12-7
1.8	1, Update powerdown current and active current spec on the first page. 2, remove WSON6*8 package type	/	Zuohuan Yu 2022-10-26
1.9	Add SOP16-300mil package type	/	Zuohuan Yu 2022-10-27
2.0	Update Commercial Temperature Range	/	Zuohuan Yu 2023-02-10
2.1	Change the frequency of Fast Read、Dual I/O、Quad I/O & QPI、DTR Quad I/O Data transfer.	/	Zuohuan Yu 2023-02-17
2.2	Change MPQ of TFBGA24 package	/	Zuohuan Yu 2023-03-17
2.3	Update the logo and abbreviation	/	Zuohuan Yu 2023-04-04
2.4	Revised the description of chip stacking information and package	/	Zuohuan Yu 2023-06-02
2.5	Update package type	/	Zuohuan Yu 2024-4-15