DATASHEET

FOR

2M BIT SPI NOR FLASH

BY25Q20BL

Features

- **Serial Peripheral Interface (SPI)**
  - Standard SPI: SCLK, /CS, SI, SO, /WP, /HOLD
  - Dual SPI: SCLK, /CS, IO0, IO1, /WP, /HOLD
  - Quad SPI: SCLK, /CS, IO0, IO1, IO2, IO3
  - Software Reset
  - Hardware Reset
- **Read**
  - Normal Read Data : 33MHz clock rate
  - others Read Data : 85MHz clock rate
- **Program**
  - Serial-input Page Program up to 256bytes
  - Dual-input Page Program up to 256bytes
  - Quad-input Page Program up to 256bytes
  - Program Suspend and Resume
- **Erase**
  - Page erase (256-byte)
  - Block erase (64/32 KB)
  - Sector erase (4 KB)
  - Chip erase
  - Erase Suspend and Resume
- **Program/Erase Speed**
  - Page Program time: 2ms typical
  - Page Erase time: 8ms typical
  - Sector/Block Erase time: 8ms typical
  - Chip Erase time: 8ms typical
- **Flexible Architecture**
  - Sector of 4K-byte
  - Block of 32/64K-byte
- **Low Power Consumption**
  - 3mA maximum active current
  - 0.6uA maximum power down current
- **Software/Hardware Write Protection**
  - 3x512-Byte Security Registers with OTP Lock
  - Enable/Disable protection with WP Pin
  - Write protect all/portion of memory via software protect
  - Top or Bottom, Sector or Block selection
- **Single Supply Voltage**
  - Full voltage range: 1.65~2.0V
- **Temperature Range**
  - Commercial (0℃ to +70℃)
  - Industrial (-40℃ to +85℃)
- **Cycling Endurance/Data Retention**
  - Typical 100k Program-Erase cycles on any sector
  - Typical 20-year data retention at +55℃

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1. Description

The BY25Q20BL is 2M-bit Serial Peripheral Interface (SPI) Flash memory, designed for using in a wide variety of high-volume consumer based applications in which program code is shadowed from Flash memory into embedded or external RAM for execution. The flexible erase architecture of the device, with its page erase granularity it is ideal for data storage as well, eliminating the need for additional data storage devices.

The erase block sizes of the device have been optimized to meet the needs of today's code and data storage applications. By optimizing the size of the erase blocks, the memory space can be used much more efficiently. Because certain code modules and data storage segments must reside by themselves in their own erase regions, the wasted and unused memory space that occurs with large sectored and large block erase Flash memory devices can be greatly reduced. This increased memory space efficiency allows additional code routines and data storage segments to be added while still maintaining the same overall device density.

The device uses a single low voltage power supply, ranging from 1.65 Volt to 2.0 Volt, and supports JEDEC standard manufacturer and device ID, a 128-bit Unique Serial Number and three 512-bytes Security Registers.

Figure 1. Logic diagram

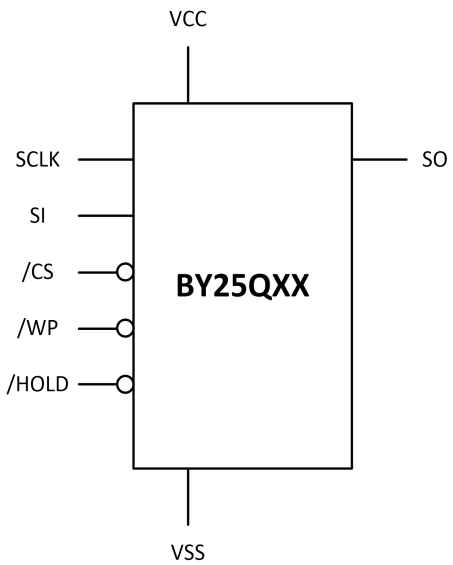


Figure 2. Pin Configuration SOP8/TSSOP8

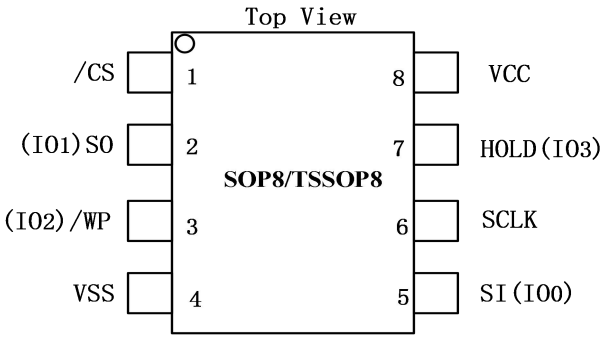


Figure 3a. Pin Configuration DFN8 2*3/1.5*1.5 mm

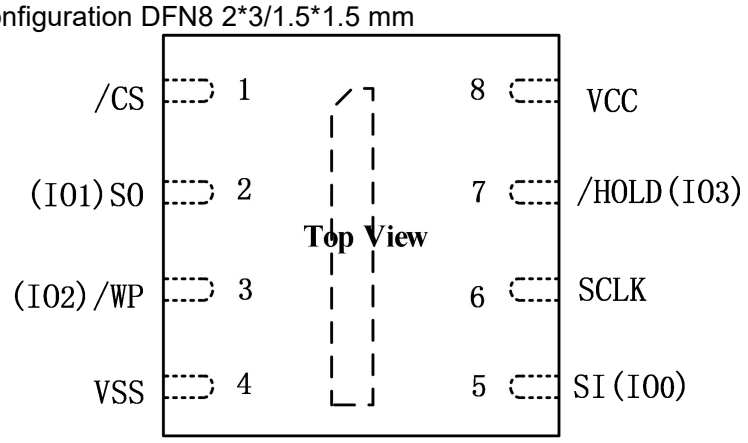
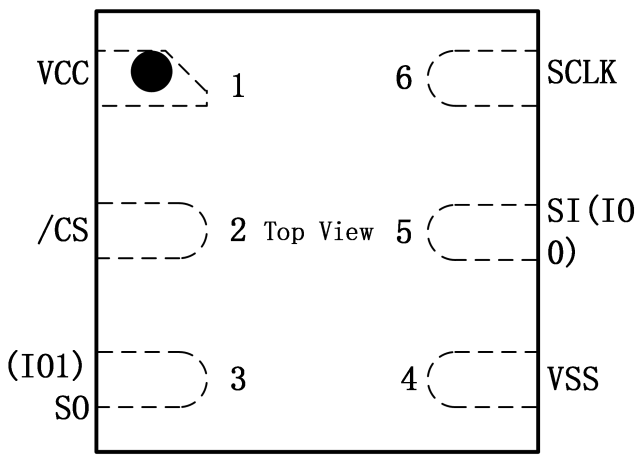


Figure 3b. Pin Configuration DFN6 1.2*1.2 mm



(Note: Hold function and WP function and quad read mode is not available for DFN6 package.)

2. Signal Description

During all operations, VCC must be held stable and within the specified valid range: VCC(min) to VCC(max).

All of the input and output signals must be held High or Low (according to voltages of VIH, VOH, VIL or VOL, see Section 8.4, *DC Electrical Characteristics*). These signals are described next.

2.1 Input/Output Summary

Table 1a. Signal Names

Pin Name	I/O	Description
/CS	I	Chip Select
SO (IO1)	I/O	Serial Output for Standard SPI mode IO1 for Dual or Quad SPI mode
/WP (IO2)	I/O	Write Protect in Standard SPI mode or Dual SPI mode IO2 in Quad SPI mode. The signal has an internal pull-up resistor and may be left unconnected in the host system if not used for Quad SPI mode. (Note: This signal and relevant function is not available for 6-pin package.)
VSS		Ground
SI (IO0)	I/O	Serial Input for Standard SPI mode. IO0 for Dual or Quad SPI mode.
SCLK	I	Serial Clock
/HOLD (IO3)	I/O	Hold (pause) serial transfer in Standard SPI mode or Dual SPI mode. IO3 in Quad SPI mode. The signal has an internal pull-up resistor and may be left unconnected in the host system if not used for Quad SPI mode. (Note: This signal and relevant function is not available for 6-pin package.)
VCC		Core and I/O Power Supply

Table 1b. Signal Names for WLCSP

BALL NO.	PIN NAME	I/O	FUNCTION
A1	VCC		Power Supply
A2	/HOLD (IO3)	I/O	Hold Input (Data Input Output 3)(2)
A3	/CS	I	Chip Select Input
B1	CLK	I	Serial Clock Input
B2	DO (IO1)	I/O	Data Output (Data Input Output 1)(1)
C1	DI (IO0)	I/O	Data Input (Data Input Output 0)(1)
C2	/WP (IO2)	I/O	Write Protect Input (Data Input Output 2)(2)
C3	GND		Ground

2.2 Chip Select (/CS)

The chip select signal indicates when an instruction for the device is in process and the other signals are relevant for the memory device. When the /CS signal is at the logic high state, the device is not selected and all input signals are ignored and all output signals are high impedance. Unless an internal Program, Erase or Write Status Registers embedded operation is in progress, the device will be in the Standby Power mode. Driving the /CS input to logic low state enables the device, placing it in the Active Power mode. After Power Up, a falling edge on /CS is required prior to the start of any instruction.

2.3 Serial Clock (SCLK)

This input signal provides the synchronization reference for the SPI interface. Instructions, addresses, or data input are latched on the rising edge of the SCLK signal. Data output changes after the falling edge of SCLK.

2.4 Serial Input (SI)/IO0

This input signal is used to transfer data serially into the device. It receives instructions, addresses, and data to be programmed. Values are latched on the rising edge of serial SCK clock signal.

SI becomes IO0 an input and output during Dual and Quad SPI mode for receiving instructions, addresses, and data to be programmed (values latched on rising edge of serial SCK clock signal) as well as shifting out data (on the falling edge of SCK).

2.5 Serial Data Output (SO)/IO1

This output signal is used to transfer data serially out of the device. Data is shifted out on the falling edge of the serial SCK clock signal.

SO becomes IO1 an input and output during Dual and Quad SPI mode for receiving instructions, addresses, and data to be programmed (values latched on rising edge of serial SCK clock signal) as well as shifting out data (on the falling edge of SCK).

2.6 Write Protect (/WP)/IO2

When /WP is driven Low (VIL), while the Status Register Protect bits (SRP1 and SRP0) of the Status Registers (SR2[0] and SR1[7]) are set to 0 and 1 respectively, it is not possible to write to the Status Registers. This prevents any alteration of the Status Registers. As a consequence, all the data bytes in the memory area that are protected by the Block Protect, BP4, BP3 bits in the status registers, are also hardware protected against data modification while /WP remains Low. The /WP function is not available when the Quad mode is enabled (QE) in Status Register 2 (SR2[1]=1).

The /WP function is replaced by IO2 for input and output during Quad mode for receiving addresses, and data to be programmed (values are latched on rising edge of the SCK signal) as well as shifting out data (on the falling edge of SCK). /WP has an internal pull-up resistance; when unconnected; /WP is at VIH and may be left unconnected in the host system if not used for Quad mode.

This signal and relevant function is not available for 6-pin package.

2.7 HOLD (/HOLD)/RESET /IO3

The /HOLD function is only available when QE=0, which can be configured either as a /HOLD pin or as a /RESET pin depending on Status Register setting. If QE=1, the /HOLD function is disabled, the pin acts as dedicated data I/O pin, and the /HOLD or /RESET function is not available.

When QE=0 and HOLD/RES= 0, the /HOLD signal goes low to stop any serial communications with the device, but doesn't stop the operation of write status register, programming, or erasing in progress.

The operation of HOLD, need /CS keep low, and starts on falling edge of the /HOLD signal, with SCLK signal being low (if SCLK is not being low, HOLD operation will not start until SCLK being low). The HOLD condition ends on rising edge of /HOLD signal with SCLK being low (If SCLK is not being low, HOLD operation will not end until SCLK being low).

This signal and relevant function is not available for 6-pin package.

2.8 VCC Power Supply

VCC is the supply voltage. It is the single voltage used for all device functions including read, program, and erase.

2.9 VSS Ground

VSS is the reference for the VCC supply voltage.

3. Block/Sector Addresses

Table 2. Block/Sector Addresses of BY25Q20BL

Memory Density	Block(64k byte)	Block(32k byte)	Sector No.	Sector Size(KB)	Address range
2Mbit	Block 0	Half block 0	Sector 0	4	000000h-000FFFh
			:	:	:
			Sector 7	4	007000h-007FFFh
		Half block 1	Sector 8	4	008000h-008FFFh
			:	4	:
			Sector 15	4	00F000h-00FFFFh
	Block 1	Half block 2	Sector 16	4	010000h-010FFFh
			:	:	:
			Sector 23	4	017000h-017FFFh
		Half block 3	Sector 24	4	018000h-018FFFh
			:	:	:
			Sector 31	4	01F000h-01FFFFh
	Block 2	Half block 4	Sector 32	4	020000h-020FFFh
			:	:	:
			Sector 39	4	027000h-027FFFh
		Half block 5	Sector 40	4	028000h-028FFFh
			:	:	:
			Sector 47	4	02F000h-02FFFFh
	Block 3	Half block 6	Sector 48	4	030000h-030FFFh
			:	:	:
			Sector 55	4	037000h-037FFFh
		Half block 7	Sector 56	4	038000h-038FFFh
			:	:	:
			Sector 63	4	03F000h-03FFFFh

Notes:
1. Block = Uniform Block, and the size is 64K bytes.
2. Half block = Half Uniform Block, and the size is 32k bytes.
3. Sector = Uniform Sector, and the size is 4K bytes.

4. Function Descriptions

4.1 Standard SPI Instructions

The BY25Q20BL features a serial peripheral interface on 4 signals bus: Serial Clock (SCLK), Chip Select (/CS), Serial Data Input (SI) and Serial Data Output (SO). Both SPI bus mode 0 and 3 are supported.

4.2 Dual SPI Instructions

The BY25Q20BL supports Dual SPI operation when using the “Dual Output Fast Read” and “Dual I/O Fast Read” (3Bh and BBh) instructions. These instructions allow data to be transferred to or from the device at two times the rate of the standard SPI. When using the Dual SPI instruction the SI and SO pins become bidirectional I/O pins: IO0 and IO1

4.3 Quad SPI Instructions

The BY25Q20BL supports Quad SPI operation when using the “Quad Output Fast Read”, “Quad I/O Fast Read”, (6Bh, EBh,) instructions. These instructions allow data to be transferred to or from the device at four times the rate of the standard SPI. When using the Quad SPI instruction the SI and SO pins become bidirectional I/O pins: IO0 and IO1, and /WP and /HOLD pins become IO2 and IO3. Quad SPI instructions require the non-volatile Quad Enable bit (QE) in Status Register-2 to be set to 1. This mode is not available for 6-pin package.

All of the above three SPI mode (Standard SPI, Dual SPI and Quad SPI) have input bits (including instructions, addresses, data, M7~M0, W6~W4 etc.) latched on the rising edge of SCLK and output bits shifted out on the falling edge of SCLK.

5. Operation Features

5.1 Supply Voltage

5.1.1 Operating Supply Voltage

Prior to selecting the memory and issuing instructions to it, a valid and stable VCC voltage within the specified [VCC(min), VCC(max)] range must be applied (see *operating ranges*). In order to secure a stable DC supply voltage, it is recommended to decouple the VCC line with a suitable capacitor (usually of the order of 10 *nF* to 100 *nF*) close to the VCC/VSS package pins. This voltage must remain stable and valid until the end of the transmission of the instruction and, for a Write instruction, until the completion of the internal write cycle.

5.1.2 Power-up Conditions

When the power supply is turned on, VCC rises continuously from VSS to VCC. During this time, the Chip Select (/CS) line is not allowed to float but should follow the VCC voltage, it is therefore recommended to connect the /CS line to VCC via a suitable pull-up resistor.

In addition, the Chip Select (/CS) input offers a built-in safety feature, as the /CS input is edge sensitive as well as level sensitive: after power-up, the device does not become selected until a falling edge has first been detected on Chip Select (/CS). This ensures that Chip Select (/CS) must have been High, prior to going Low to start the first operation.

5.1.3 Device Reset

In order to prevent inadvertent Write operations during power-up (continuous rise of VCC), a power on reset (POR) circuit is included. At Power-up, the device does not respond to any instruction until VCC has reached the power on reset threshold voltage (this threshold is lower than the minimum VCC operating voltage defined in *Power-up Timing*).

When VCC is lower than V_{WI}, the device is reset.

5.1.4 Power-down

At Power-down (continuous decrease in VCC), as soon as VCC drops from the normal operating voltage to below the power on reset threshold voltage (VWI), the device stops responding to any instruction sent to it. During Power-down, the device must be deselected (Chip Select (/CS) should be allowed to follow the voltage applied on VCC) and in Standby Power mode (that is there should be no internal Write cycle in progress).

5.2 Active Power and Standby Power Modes

When Chip Select (/CS) is Low, the device is selected, and in the Active Power mode. The device consumes ICC. When Chip Select (/CS) is High, the device is deselected. If a Write cycle is not currently in progress, the device then goes in to the Standby Power mode, and the device consumption drops to ICC1.

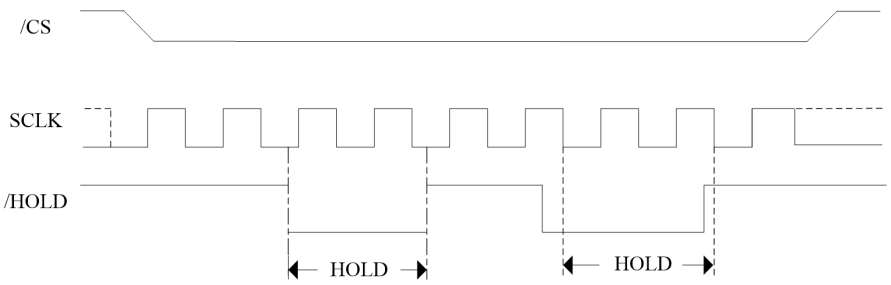
5.3 Hold Condition

When QE=0, HOLD/RST=0, the Hold (/HOLD) signal is used to pause any serial communications with the device without resetting the clocking sequence, but doesn't stop the operation of write status register, programming, or erasing in progress. During the Hold condition, the Serial Data Output (SO) is high impedance, and Serial Data Input (SI) and Serial Clock (SCLK) are Don't Care. To enter the Hold condition, the device must be selected, with Chip Select (/CS) Low. Normally, the device is kept selected, for the whole duration of the Hold condition. Deselecting the device while it is in the Hold condition, has the effect of resetting the state of the device, and this mechanism can be used if it is required to reset any processes that had been in progress.

The Hold condition starts when the Hold (/HOLD) signal is driven Low at the same time as Serial Clock (SCLK) already being Low (as shown in *Figure 5.1*).The Hold condition ends when the Hold (HOLD) signal is driven High at the same time as Serial Clock (C) already being Low. *Figure 5.1* also shows what happens if the rising and falling edges are not timed to coincide with Serial Clock (SCLK) being Low.

Hold condition is not available for 6-pin package.

Figure 5.1. Hold condition activation



5.4 Software Reset & Hardware RESET

5.4.1 Software Reset

The BY25Q20BL can be reset to the initial power-on state by a software reset sequence. This sequence must include two consecutive instructions: Enable Reset (66h) & Reset (99h). If the instruction sequence is successfully accepted, the device will take approximately 300uS (tRST) to reset. No instruction will be accepted during the reset period.

5.4.2 Hardware Reset (/HOLD pin)

The BY25Q20BL can also be configured to utilize hardware /RESET pin. The HOLD/RST bit in the Status Register-3 is the configuration bit for /HOLD pin function or /RESET pin function. When HOLD/RST=0 (factory default), the pin acts as a /HOLD pin as described above; when HOLD/RST=1, the pin acts as a /RESET pin. Drive the /RESET pin low for a minimum period of ~1us (tRESET(1)) will reset the device to its initial power-on state. Any on-going Program/Erase operation will be interrupted and data corruption may happen. While /RESET is low, the device will not accept any instruction input. If QE bit is set to 1, the /HOLD or /RESET function will be disabled, the pin will become one of the four data I/O pin.

Notes:

1. While a faster /RESET pulse (as short as a few hundred nanoseconds) will often reset the device, a 1us minimum pulse is recommended to ensure reliable operation.
2. Hardware Reset function is not available for 6-pin package.

5.5 Status Register

5.5.1 The Status and Control Bits

	SR3							
	S23	S22	S21	S20	S19	S18	S17	S16
	HOLD/ RST	NOP	NOP	NOP	NOP	NOP	NOP	NOP
Default value Note1	0	n/a	n/a	n/a	n/a	n/a	n/a	n/a

	SR2							
	S15	S14	S13	S12	S11	S10	S9	S8
	SUS	CMP	LB3	LB2	LB1	NOP	QE	SRP1
Default value Note1	n/a	0	0	0	0	n/a	0	0

	SR1							
	S7	S6	S5	S4	S3	S2	S1	S0
	SRP0	BP4	BP3	BP2	BP1	BP0	WEL	WIP
Default value Note1	0	0	0	0	0	0	n/a	n/a

Notes:

2. The default value is set by Manufacturer during wafer sort, Marked as Default in following text

The status and control bits of the Status Register are as follows:

5.5.1.1 WIP bit

The Write in Progress (WIP) bit indicates whether the memory is busy in program / erase / write status register progress. When WIP bit is set to 1, means that the device is busy in program / erase / write status register progress, when WIP bit is cleared to 0, means that the device is not in program / erase / write status register progress.

5.5.1.2 WEL bit

The Write Enable Latch bit indicates the status of the internal Write Enable Latch. When WEL bit is set to 1 the internal Write Enable Latch is set, when WEL bit is cleared to 0 the internal Write Enable Latch is reset and no Write Status Register, Program or Erase instruction is accepted.

5.5.1.3 BP4, BP3, BP2, BP1, BP0 bits

The Block Protect (BP4, BP3, BP2, BP1, BP0) bits are non-volatile. They define the size of the area to be software protected against Program and Erase instructions. These bits are written with the Write Status Register instruction. When the Block Protect (BP4, BP3, BP2, BP1, BP0) bits are set to 1, the relevant memory (as defined in *Table 4* and *Table 5*) are became protected against Page Program, Page Erase, Sector Erase and Block Erase instructions. The Block Protect (BP4, BP3, BP2, BP1, BP0) bits can be written provided that the Hardware Protected mode has not been set. The Chip Erase instruction is executed. If the Block Protect (BP2, BP1, and BP0) bits are 0 and CMP=0 or the Block Protect (BP2, BP1 and BP0) bits are 1and CMP=1.

5.5.1.4 SRP1, SRP0 bits

The Status Register Protect (SRP1 and SRP0) bits are non-volatile Read/Write bits in the status register. The SRP bits control the method of write protection: software protection, hardware protection, power supply lock-down or one time programmable protection.

Table 3. Status Register protect table

SRP1	SRP0	/WP	Status Register	Description
0	0	X	Software Protected	The Status Register can be written to after a Write Enable instruction, WEL=1.(Default)
0	1	0	Hardware Protected	/WP=0, the Status Register locked and cannot be written.
0	1	1	Hardware Unprotected	/WP=1, the Status Register is unlocked and can be written to after a Write Enable instruction, WEL=1.
1	0	X	Power Supply Lock-Down(1)	Status Register is protected and cannot be written to again until the next Power-Down, Power-Up cycle.
1	1	X	One Time Program(2)	Status Register is permanently protected and cannot be written to.

Notes:
1. When SRP1, SRP0= (1, 0), a Power-Down, Power-Up cycle will change SRP1, SRP0 to (0, 0) state.
2. The One time Program feature is available upon special order. Please contact BY Technology for details.
3. For 6-pin package, Hardware Protected and Hardware Unprotected function is not available.

5.5.1.5 QE bit

The Quad Enable (QE) bit is a non-volatile Read/Write bit in the Status Register that allows Quad SPI operation. When the QE bit is set to 0 (Default) the /WP pin and /HOLD pin are enable. When the QE bit is set to 1, the Quad IO2 and IO3 pins are enabled. (The QE bit should never be set to 1 during standard SPI or Dual SPI operation if the /WP or /HOLD pins directly to the power supply or ground).
For 6-pin package, Quad SPI operation is not available.

5.5.1.6 LB3/LB2/LB1 bit

The LB bit is a non-volatile One Time Program (OTP) bit in Status Register (S13-S11) that provide the write protect control and status to the Security Registers. The default state of LB is 0, the security registers are unlocked. LB can be set to 1 individually using the Write Register instruction. LB is One Time Programmable, once it's set to 1, the Security Registers will become read-only permanently (LB3-1 corresponds to S13-11).

5.5.1.7 SUS bit

The SUS bit are read only bits in the status register2 (S15) that are set to 1 after executing a Program/Erase Suspend (75H) instruction. The SUS bit are cleared to 0 by Program/Erase Resume (7AH) instruction. Software reset (66H/99H) instruction or Hardware reset as well as a power-down, power-up cycle.

5.5.1.8 Complement Protect (CMP)

The Complement Protect bit (CMP) is a non-volatile read/write bit in the status register. It is used in conjunction with BP4, BP3, BP2, BP1 and BP0 bits to provide more flexibility for the array

protection. Please refer to the *Status Register Memory Protection table* for details. The default setting is CMP=0.

5.5.1.9 HOLD/RST bit

The /HOLD or /RESET Pin Function (HOLD/RST) bit is used to determine whether /HOLD or /RESET function should be implemented on the hardware pin. When HOLD/RST=0 (factory default), the pin acts as /HOLD; when HOLD/RST=1, the pin acts as /RESET. However, /HOLD or /RESET functions are only available when QE=0. If QE is set to 1, the /HOLD and /RESET functions are disabled, the pin acts as a dedicated data I/O pin.
For 6-pin package, HOLD/RST function is not available.

5.5.2 Status Register Memory Protection

5.5.2.1 Protect Table

Table 4. BY25Q20BL Status Register Memory Protection (CMP = 0)

STATUS REGISTER(1)					BY25Q20BL (2M-BIT) MEMORY PROTECTION(3)			
BP4	BP3	BP2	BP1	BP0	PROTECTED BLOCK(S)	PROTECTED ADDRESSES	PROTECTED DENSITY	PROTECTED PORTION(2)
0	X	X	0	0	NONE	NONE	NONE	NONE
0	0	X	0	1	3	030000h – 03FFFFh	64KB	Upper 1/4
0	0	X	1	0	2 and 3	020000h – 03FFFFh	128KB	Upper 1/2
0	1	X	0	1	0	000000h – 00FFFFh	64KB	Lower 1/4
0	1	X	1	0	0 and 1	000000h – 01FFFFh	128KB	Lower 1/2
0	X	X	1	1	0 to 3	000000h – 03FFFFh	256KB	ALL
1	X	0	0	0	NONE	NONE	NONE	NONE
1	0	0	0	1	3	03F000h – 03FFFFh	4KB	U - 1/64
1	0	0	1	0	3	03E000h – 03FFFFh	8KB	U - 1/32
1	0	0	1	1	3	03C000h – 03FFFFh	16KB	U - 1/16
1	0	1	0	X	3	038000h – 03FFFFh	32KB	U - 1/8
1	0	1	1	0	3	038000h – 03FFFFh	32KB	U - 1/8
1	1	0	0	1	0	000000h – 000FFFh	4KB	L - 1/64
1	1	0	1	0	0	000000h – 001FFFh	8KB	L - 1/32
1	1	0	1	1	0	000000h – 003FFFh	16KB	L - 1/16
1	1	1	0	X	0	000000h – 007FFFh	32KB	L - 1/8
1	1	1	1	0	0	000000h – 007FFFh	32KB	L - 1/8
1	X	1	1	1	0 to 3	000000h – 03FFFFh	256KB	ALL

Notes:
1. X = don't care
2. L = Lower; U = Upper
3. If any Erase or Program instruction specifies a memory region that contains protected data portion, this instruction will be ignored.

Table 5. BY25Q20BL Status Register Memory Protection (CMP = 1)

STATUS REGISTER(1)	BY25Q20BL (2M-BIT) MEMORY PROTECTION(3)

BP4	BP3	BP2	BP1	BP0	PROTECTED BLOCK(S)	PROTECTED ADDRESSES	PROTECTED DENSITY	PROTECTED PORTION(2)
0	X	X	0	0	0 to 3	000000h – 03FFFFh	512KB	All
0	0	X	0	1	0 to 2	000000h – 02FFFFh	448KB	Lower 3/4
0	0	X	1	0	0 and 1	000000h – 01FFFFh	384KB	Lower 1/2
0	1	X	0	1	1 to 3	010000h – 03FFFFh	256KB	Upper 3/4
0	1	X	1	0	2 to 3	020000h – 03FFFFh	448KB	Upper 1/2
0	X	X	1	1	NONE	NONE	NONE	NONE
1	X	0	0	0	0 to 3	000000h – 03FFFFh	256KB	ALL
1	0	0	0	1	0 to 3	000000h – 03EFFFh	252KB	L - 63/64
1	0	0	1	0	0 to 3	000000h – 03DFFFh	248KB	L - 31/32
1	0	0	1	1	0 to 3	000000h – 03BFFFh	240KB	L - 15/16
1	0	1	0	X	0 to 3	000000h – 037FFFh	224KB	L - 7/8
1	0	1	1	0	0 to 3	000000h – 037FFFh	224KB	L - 7/8
1	1	0	0	1	0 to 3	001000h – 03FFFFh	252KB	U - 63/64
1	1	0	1	0	0 to 3	002000h – 03FFFFh	248KB	U - 31/32
1	1	0	1	1	0 to 3	004000h – 03FFFFh	240KB	U - 15/16
1	1	1	0	X	0 to 3	008000h – 03FFFFh	224KB	U - 7/8
1	1	1	1	0	0 to 3	008000h – 03FFFFh	224KB	U - 7/8
1	X	1	1	1	NONE	NONE	NONE	NONE

Notes:

1. X = don’t care
2. L = Lower; U = Upper
3. If any Erase or Program instruction specifies a memory region that contains protected data portion, this instruction will be ignore

6. Device Identification

Three legacy Instructions (9Fh/90h/ABh) and two new Instructions (92h/94h) in Dual/Quad SPI mode are supported to access device identification that can indicate the manufacturer, device type, and capacity (density). The returned data bytes provide the information as shown in the below table.

Table 6. BY25Q20BL ID Definition table

Operation Code	M7-M0	ID15-ID8	ID7-ID0
9Fh	68	10	12
90h / 92h /94h	68		11
ABh			11

7. Instructions Description

All instructions, addresses and data are shifted in and out of the device, beginning with the most significant bit on the first rising edge of SCLK after /CS is driven low. Then, the one byte instruction code must be shifted in to the device, most significant bit first on SI, each bit being latched on the rising edges of SCLK.

See *Table 7*, every instruction sequence starts with a one-byte instruction code. Depending on the instruction, this might be followed by address bytes, or by data bytes, or by both or none.

For the instruction of Read, Fast Read, Read Status Register-1, Read Status Register-2 or Release from Deep Power Down, and Read Device ID, the shifted-in instruction sequence is followed by a data out sequence. /CS can be driven high after any bit of the data-out sequence is being shifted out.

For the instruction of Page Program, Page Erase, Sector Erase, Block Erase, Chip Erase, Write Status Register, Write Enable, Write Disable or Deep Power-Down instruction, /CS must be driven high exactly at a byte boundary, otherwise the instruction is rejected, and is not executed. That is /CS must drive high when the number of clock pulses after /CS being driven low is an exact multiple of eight. For Page Program, if at any time the input byte is not a full byte, nothing will happen and WEL will not be reset.

Table 7. Instruction Set Table 1 (1)

Instruction Name	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	n-Bytes
Read							
Normal Read Data	03h	A23-A16	A15-A8	A7-A0	(D7-D0)	(Next Byte)	(continuous)
Fast Read	0Bh	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)	(continuous)
Dual Output Fast read	3Bh	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)(2)	(continuous)
Quad Output Fast read	6Bh	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)(3)	(continuous)
Dual I/O Fast read	BBh	A23-A8(4)	A7-A0 M7-M0(4)	(D7-D0)			(continuous)
Quad I/O Fast read	EBh	A23-A0 M7-M0(5)	Dummy	(D7-D0)(6)			(continuous)
Set Burst With Wrap	77h	W6-W4					
Program/Erase and Suspend							
Page Program	02h	A23-A16	A15-A8	A7-A0	(D7-D0)(7)	(Next Byte)	
Dual Page Program	A2h	A23-A16	A15-A8	A7-A0	(D7-D0)(7)	(Next Byte)	
Quad Page Program	32h	A23-A16	A15-A8	A7-A0	(D7-D0)(7)	(Next Byte)	
Page Erase	81h/DBh	A23-A16	A15-A8	A7-A0			
Sector Erase (4KB)	20h	A23-A16	A15-A8	A7-A0			
Block Erase (32KB)	52h	A23-A16	A15-A8	A7-A0			
Block Erase (64KB)	D8h	A23-A16	A15-A8	A7-A0			
Chip Erase	C7h/60h						
Program/Erase Suspend	75h						
Program/Erase Resume	7Ah						
Security							
Erase Security Registers	44h	A23-A16(8)	A15-A8(8)	A7-A0(8)			
Program Security Registers	42h	A23-A16(8)	A15-A8(8)	A7-A0(8)	D7-D0	Next Byte	
Read Security Registers	48h	A23-A16(8)	A15-A8(8)	A7-A0(8)	Dummy	D7-D0	
Read Serial Flash Discoverable Parameter	5Ah	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)	(continuous)
Configuration							
Write Enable	06h						
Volatile SR Write Enable	50h						
Write Disable	04h						
Status Register							
Read Status Register-1	05h	(S7-S0)(9)					(continuous)
Write Status Register(10)	01h	S7-S0	S15-S8				
Read Status Register-2	35h	(S15-S8)(9)					(continuous)
Write Status Register-2	31h	S15-S8					
Read Status Register-3	15h	(S23-S16)(9)					(continuous)
Write Status Register-3	11h	S23-S16					
Active Status Interrupt	25h						
ID and Power							
Deep Power-down	B9h						
Release Power-down / ID	ABh	Dummy	Dummy	Dummy	(ID7-ID0)(9)		(continuous)
Release Power-down	ABH						
Manufacturer/Device ID	90h	Dummy	Dummy	00/01h	(MF7-MF0)/ (ID7-ID0)	(ID7-ID0)(9)/ (MF7-MF0)(9)	(continuous)
Mftr./Device ID Dual I/O	92h	A23-A8(4)	A7-A0(4) M7-M0	(M7-M0) (D7-D0)			(continuous)
Mftr./Device ID Quad I/O	94h	A23-A0	(M7-M0)				(continuous)

		M7-M0(5)	(D7-D0)(6)				
Read JEDEC ID	9Fh	(MF7-MF0)	(ID15-ID8)	(ID7-ID0)(9)			(continuous)
Read Unique ID Number	4Bh	Dummy	Dummy	Dummy	Dummy	(ID127-ID0)	
Other Instructions							
Enable Reset	66h						
Reset Device	99h						

Notes:

1. Data bytes are shifted with Most Significant Bit first. Byte fields with data in parenthesis "( )" indicate data output from the device.
2. Dual SPI data output format:
   IO0 = (D6, D4, D2, D0)
   IO1 = (D7, D5, D3, D1)
3. Quad SPI data output format:
   IO0 = (D4, D0, …..)
   IO1 = (D5, D1, …..)
   IO2 = (D6, D2, …..)
   IO3 = (D7, D3, …..)
4. Dual SPI address input format:
   IO0 = A22, A20, A18, A16, A14, A12, A10, A8, A6, A4, A2, A0, M6, M4, M2, M0
   IO1 = A23, A21, A19, A17, A15, A13, A11, A9, A7, A5, A3, A1, M7, M5, M3, M1
5. Quad SPI address input format:
   IO0 = A20, A16, A12, A8, A4, A0, M4, M0
   IO1 = A21, A17, A13, A9, A5, A1, M5, M1
   IO2 = A22, A18, A14, A10, A6, A2, M6, M2
   IO3 = A23, A19, A15, A11, A7, A3, M7, M3
6. Fast Read Quad I/O data output format:
   IO0 = (x, x, x, x, D4, D0, D4, D0)
   IO1 = (x, x, x, x, D5, D1, D5, D1)
   IO2 = (x, x, x, x, D6, D2, D6, D2)
   IO3 = (x, x, x, x, D7, D3, D7, D3)
7. At least one byte of data input is required for Page Program, Dual Page Program, Quad Page Program and Program Security Registers, up to 256 bytes of data input. If more than 256 bytes of data are sent to the device, the addressing will wrap to the beginning of the page and overwrite previously sent data.
8. Security Register Address:

Security Register 1	A23-16 = 00h	A15-9 = 0001000	A8-0 = byte address
Security Register 2	A23-16 = 00h	A15-9 = 0010000	A8-0 = byte address
Security Register 3	A23-16 = 00h	A15-9 = 0011000	A8-0 = byte address

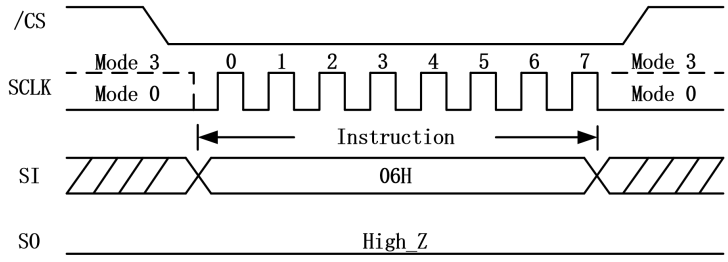
9. The Status Register contents and Device ID will repeat continuously until /CS terminates the instruction.
10. Write Status Register (01h) can also be used to write Status Register-1&2, see *section 7.1.6*.
11. For 6-pin package, Quad SPI instructions are not available.

7.1 Configuration and Status Instructions

7.1.1 Write Enable (06H)

The Write Enable instruction (*Figure 7.1.1*) sets the Write Enable Latch (WEL) bit in the Status Register to a 1. The WEL bit must be set prior to every Page Program, Dual Page Program, Quad Page Program, Page Erase, Sector Erase, Block Erase, Chip Erase, Write Status Register and Erase/Program Security Registers instruction. The Write Enable instruction is entered by driving /CS low, shifting the instruction code “06h” into the Data Input (SI) pin on the rising edge of SCLK, and then driving /CS high.

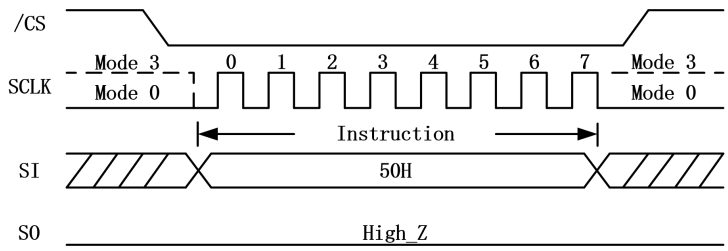
Figure 7.1.1. Write Enable Instruction for SPI Mode



7.1.2 Write Enable for Volatile Status Register (50h)

The non-volatile Status Register bits described in *section 5.4* can also be written to as volatile bits. This gives more flexibility to change the system configuration and memory protection schemes quickly without waiting for the typical non-volatile bit write cycles or affecting the endurance of the Status Register non-volatile bits. To write the volatile values into the Status Register bits, the Write Enable for Volatile Status Register (50h) instruction must be issued prior to a Write Status Register (01h) instruction. Write Enable for Volatile Status Register instruction (*Figure 7.1.2*) will not set the Write Enable Latch (WEL) bit, it is only valid for the Write Status Register instruction to change the volatile Status Register bit values.

Figure 7.1.2. Write Enable for Volatile Status Register Instruction for SPI Mode

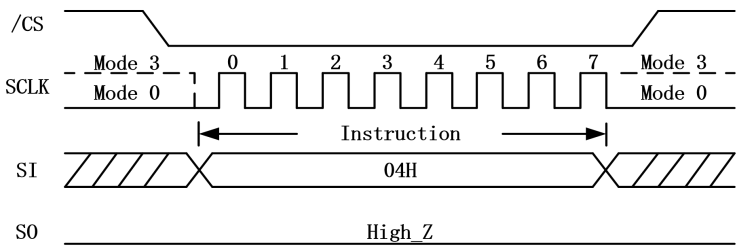


7.1.3 Write Disable (04h)

The Write Disable instruction (*Figure 7.1.3*) resets the Write Enable Latch (WEL) bit in the Status Register to 0. The Write Disable instruction is entered by driving /CS low, shifting the instruction code “04h” into the SI pin and then driving /CS high.

Note that the WEL bit is automatically reset after Power-up and upon completion of the Write Status Register, Erase/Program Security Registers, Page Program, Dual Page Program, Quad Page Program, Page Erase, Sector Erase, Block Erase, Chip Erase and Reset instructions.

Figure 7.1.3. Write Disable Instruction for SPI Mode

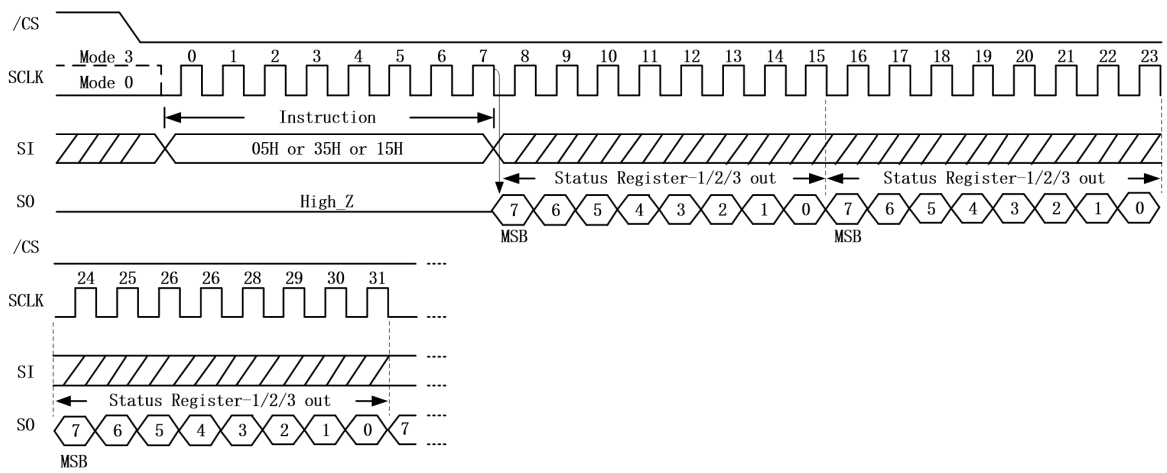


7.1.4 Read Status Register-1 (05h) , Status Register-2 (35h) , Status Register-3(15h)

The Read Status Register instructions allow the 8-bit Status Registers to be read. The instruction is entered by driving /CS low and shifting the instruction code “05h” for Status Register-1, “35h” for Status Register -2, “15h” for Status Register-3 into the SI pin on the rising edge of SCLK. The status register bits are then shifted out on the SO pin at the falling edge of SCLK with most significant bit (MSB) first as shown in Figure *7.1.4*, Refer to *section 5.4* for Status Register descriptions.

The Read Status Register instruction may be used at any time, even while a Program, Erase or Write Status Register cycle is in progress. This allows the WIP status bit to be checked to determine when the cycle is complete and if the device can accept another instruction. The Status Register can be read continuously, as shown in Figure *7.1.4* The instruction is completed by driving /CS high.

Figure 7.1.4. Read Status Register Instruction



7.1.5 Active Status Interrupt (25h)

To simplify the readout of the WIP bit, the Active Status Interrupt Instruction (25h) may be used. It is then not necessary to continuously read the status register, it is sufficient to monitor the value of the SO line. If the SO line is connected to an interrupt line on the host controller, the host controller may be in sleep mode until the SO line indicates that the device is ready for the next Instruction

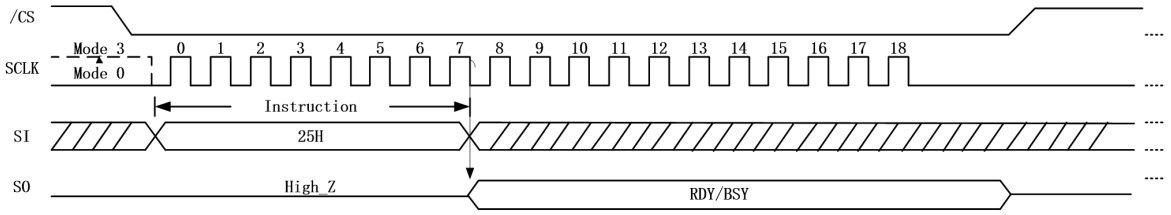
The WIP bit can be read at any time, including during an internally self-timed program or erase operation. To enable the Active Status Interrupt instruction, the /CS pin must first be asserted and the instruction code of 25h must be clocked into the device. The value of the SI line after the instruction code being clocked in is of no significance to the operation.

The value of WIP is then output on the SO line, and is continuously updated by the device for as long as the /CS pin remains asserted. Additional clocks on the SCK pin are not required. That is, whether the additional clock on the SCK pin exists is independent of the correct output of the value of WIP. (Figure *7.1.5* shows a case where additional clocks exist). If the WIP bit changes from 1 to 0 while the /CS pin is asserted, the SO line will change from 1 to 0. (The WIP bit cannot change from 0 to 1 during an operation, so if the SO line already is 0, it will not change.)

Deasserting the /CS pin will terminate the Active Status Interrupt operation and put the SO pin into a high-impedance state.

The sequence of issuing ASI instruction is: /CS goes low→ sending ASI instruction code→ WIP data out on SO

Figure 7.1.5. Active Status Interrupt Instruction



7.1.6 Write Status Register (01h or 31h or 11h)

The Write Status Register instruction allows the Status Registers to be written. The Status Register-1 can be written by the Write Status Register 01h instruction; The Status Register-2 be written by the Write Status Register 01h or 31h instruction; Status Register-3 can be written by the Write Status Register 11h instruction. When the Write Status Register instruction 01h is followed by 1 byte data, the data will be written to Status Register-1. When the Write Status Register instruction 01h is followed by 2 bytes of data, the first byte data will be written to Status Register-1, and the second byte data will be written to Status Register-2; And Write Status Register instruction 31h or 11h can only follow 1 byte data, the data will be written to Status Register-2、Status Register-3 respectively. The writable Status Register bits include: SRP0, BP[4:0] in Status Register-1; CMP, LB[3:1], QE, SRP1 in Status Register- 2; HOLD/RST in Status Register- 3. All other Status Register bit locations are read-only and will not be affected by the Write Status Register instruction. LB[3:1] are non-volatile OTP bits, once it is set to 1, it cannot be cleared to 0.

The Write Status Register (WRSR) instruction allows new values to be written to the Status Register. Before it can be accepted, a Write Enable (WREN) or Write Enable For Volatile SR instruction must previously have been executed After the Write Enable (WREN) instruction has been decoded and executed, the device sets the Write Enable Latch (WEL).

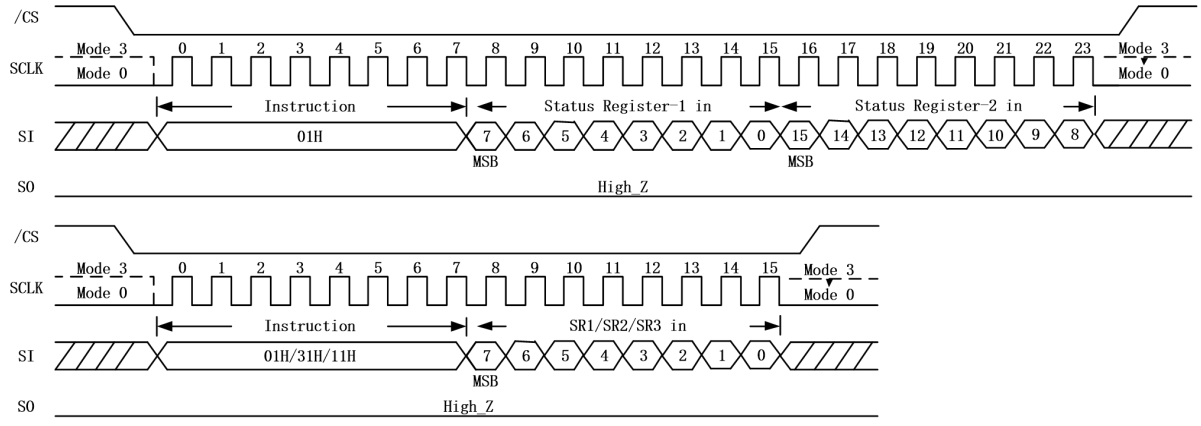
The Write Status Register instruction has no effect on S15 (SUS), S1 (WEL) and S0 (WIP) of the Status Register. /CS must be driven high after the 8 or 16 bit of the data byte has been latched in. If not, the Write Status Register (WRSR) command is not executed. As soon as /CS is driven high, the self-timed Write Status Register cycle (whose duration is tW) is initiated. While the Write Status Register cycle is in progress, the Status Register may still be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Write Status Register cycle, and is 0 when it is completed. When the cycle is completed, the Write Enable Latch (WEL) is reset.

The Write Status Register instruction allows the user to change the values of the Block Protect (BP4, BP3, BP2, BP1, and BP0) bits, to define the size of the area that is to be treated as read-only, as defined in Table4 and Table5.The Write Status Register (WRSR) instruction also allows the user to set or reset the Status Register Protect (SRP1 and SRP0) bits in accordance with the Write Protect (/WP) signal. The Status Register Protect (SRP1 and SRP0) bits and Write Protect (/WP) signal allow the device to be put in the Hardware Protected Mode. The Write Status Register instruction is not executed once the Hardware Protected Mode is entered.

The sequence of issuing WRSR instruction is: /CS goes low→ sending WRSR instruction code→ Status Register data on SI→/CS goes high.

The /CS must go high exactly at the 8 bits or 16 bits data boundary; otherwise, the instruction will be rejected and not executed. The self-timed Write Status Register cycle time (tW) is initiated as soon as Chip Select (/CS) goes high. The Write in Progress (WIP) bit still can be checked during the Write Status Register cycle is in progress. The WIP is set 1 during the tW timing, and is set 0 when Write Status Register Cycle is completed, and the Write Enable Latch (WEL) bit is reset.

Figure 7.1.6. Write Status Register Instruction



7.2 Read Instructions

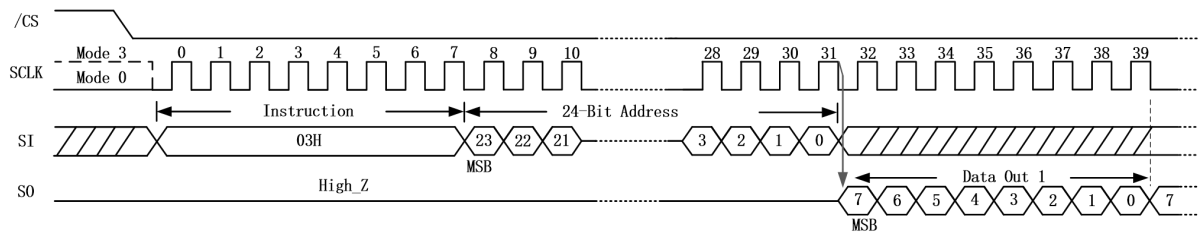
7.2.1 Normal Read Data (03H)

The Read Data instruction allows one or more data bytes to be sequentially read from the memory. The instruction is initiated by driving the /CS pin low and then shifting the instruction code “03h” followed by a 24-bit address (A23-A0) into the SI pin. The code and address bits are latched on the rising edge of the SCLK pin. After the address is received, the data byte of the addressed memory location will be shifted out on the SO pin at the falling edge of SCLK with most significant bit (MSB) first. The address is automatically incremented to the next higher address after each byte of data is shifted out allowing for a continuous stream of data. This means that the entire memory can be accessed with a single instruction as long as the clock continues. The instruction is completed by driving /CS high.

The Read Data instruction sequence is shown in *Figure 7.2.1*. If a Read Data instruction is issued while an Erase, Program or other Write cycle is in progress (WIP=1) the instruction is ignored and will not have any effects on the current cycle. The Read Data instruction allows clock frequency up to to a maximum of fR (see *AC Electrical Characteristics*).

The Normal Read Data (03h) instruction is only supported in Standard SPI mode.

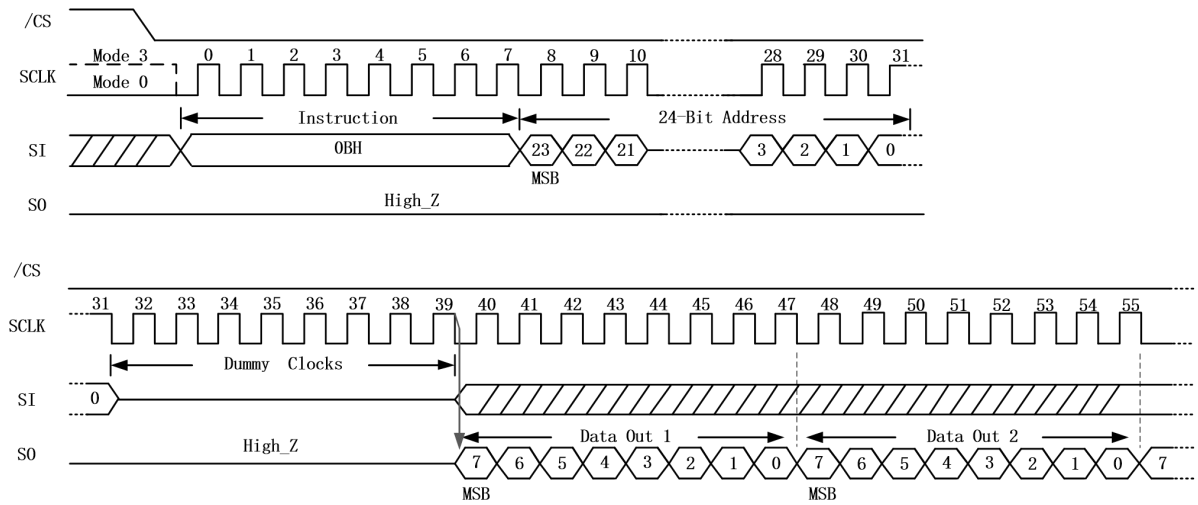
Figure 7.2.1**.** Read Data Instruction



7.2.2 Fast Read (0BH)

The Fast Read instruction is similar to the Read Data instruction except that it can operate at the highest possible frequency of fC (see *AC Electrical Characteristics*). In standard SPI mode, this is accomplished by adding eight “dummy” clocks after the 24-bit address as shown in *Figure 7.2.2*. The dummy clocks allow the devices internal circuits additional time for setting up the initial address. During the dummy clocks the data value on the SO pin is a “don’t care”.

Figure 7.2.2. Fast Read Instruction

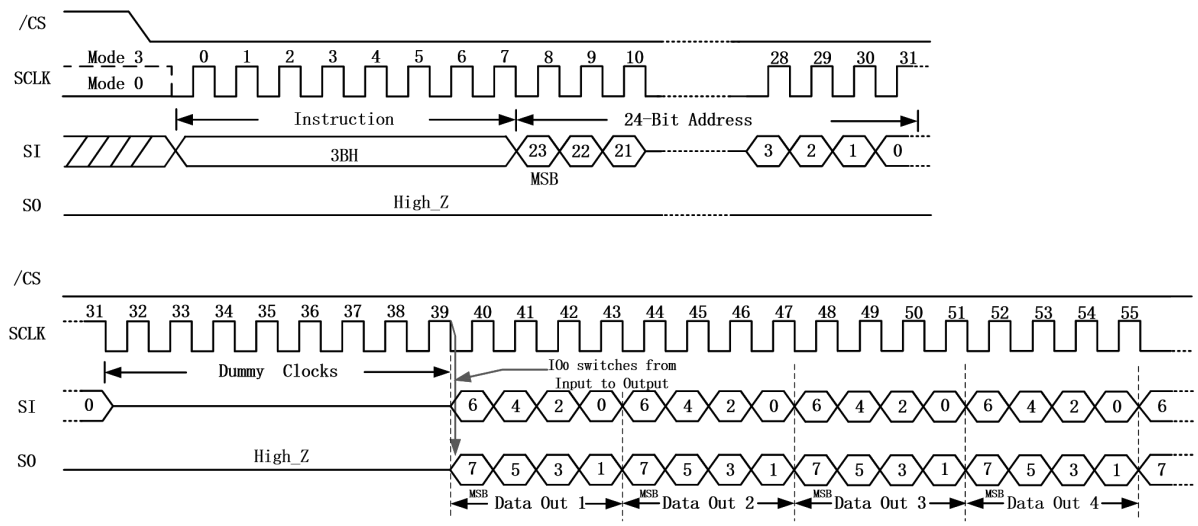


7.2.3 Fast Read Dual Output (3Bh)

The Fast Read Dual Output (3Bh) instruction is similar to the standard *Fast Read (0Bh)* instruction except that data is output on two pins; SI and SO. This allows data to be transferred at twice the rate of standard SPI devices. The Fast Read Dual Output instruction is ideal for quickly downloading code from Flash to RAM upon power-up or for applications that cache code-segments to RAM for execution.

Similar to the Fast Read instruction, the Fast Read Dual Output instruction can operate at the highest possible frequency of fC (see *AC Electrical Characteristics*). This is accomplished by adding eight “dummy” clocks after the 24-bit address as shown in *Figure 7.2.3*. The dummy clocks allow the device's internal circuits additional time for setting up the initial address. The input data during the dummy clocks is “don’t care”. However, the SI pin should be high-impedance prior to the falling edge of the first data out clock.

Figure 7.2.3. Fast Read Dual Output Instruction



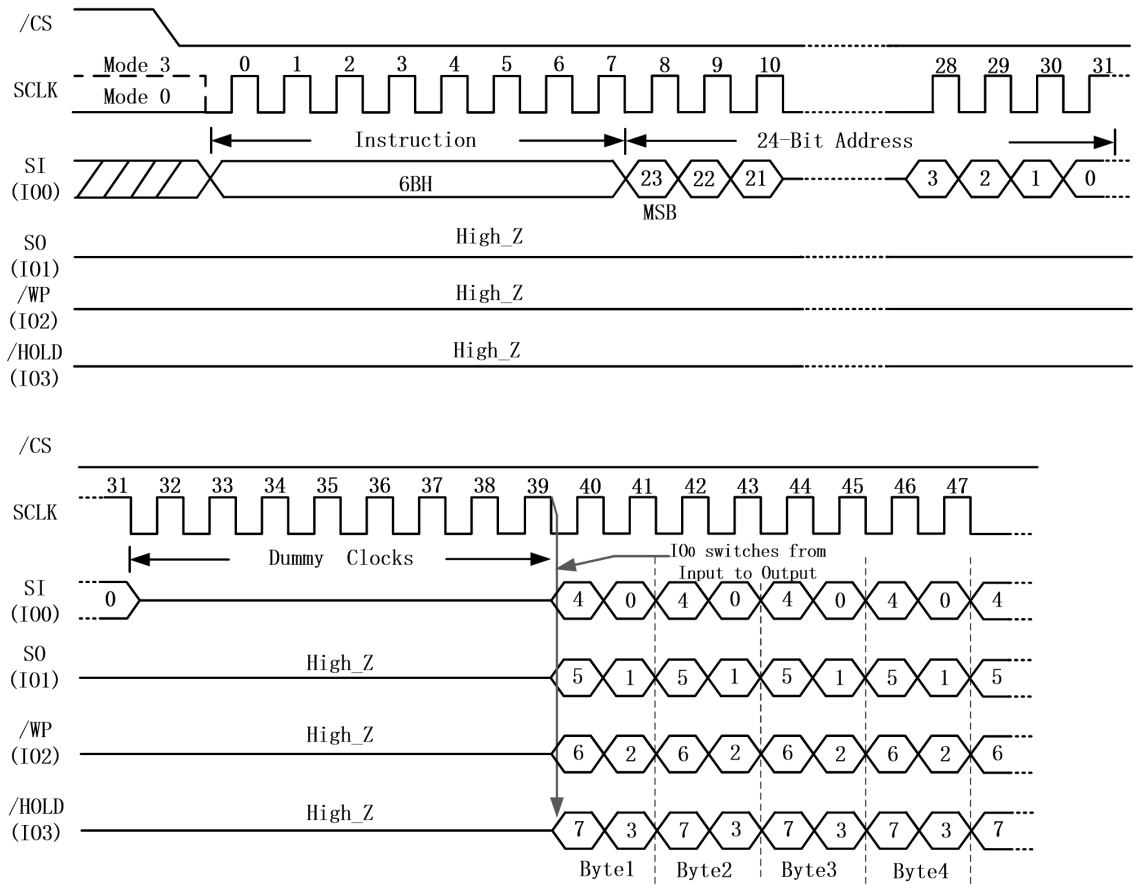
7.2.4 Fast Read Quad Output (6Bh)

The Fast Read Quad Output (6Bh) instruction is similar to the *Fast Read Dual Output (3Bh)* instruction except that data is output on two pins, SI, SO, /WP, and /HOLD. The Quad Enable (QE) bit in Status Register-2 must be set to 1 before the device will accept the Fast Read Quad Output Instruction. The Fast Read Quad Output Instruction allows data to be transferred at four times the rate of standard SPI devices.

The Fast Read Quad Output instruction can operate at the highest possible frequency of fC (see *AC Electrical Characteristics*). This is accomplished by adding eight “dummy” clocks after the 24-bit address as shown in *Figure 7.2.4*. The dummy clocks allow the device's internal circuits additional time for setting up the initial address. The input data during the dummy clocks is “don’t care”. However, the IO pins should be high-impedance prior to the falling edge of the first data out clock.

For 6-pin package, Quad SPI function is not available.

Figure 7.2.4. Fast Read Quad Output Instruction



7.2.5 Fast Read Dual I/O (BBh)

The Fast Read Dual I/O (BBh) instruction allows for improved random access while maintaining two IO pins, SI and SO. It is similar to the *Fast Read Dual Output (3Bh)* instruction but with the capability to input the Address bits (A23-0) two bits per clock. This reduced instruction overhead may allow for code execution (XIP) directly from the Dual SPI in some applications.

Fast Read Dual I/O with "Continuous Read Mode"

The Fast Read Dual I/O instruction can operate at the highest possible frequency of fC (see *AC Electrical Characteristics*). The Fast Read Dual I/O instruction can further reduce instruction overhead through setting the "Continuous Read Mode" bits (M7-0) after the input Address bits (A23- 0), as shown in *Figure 7.2.5a*. The upper nibble of the (M7-4) controls the length of the next Fast Read Dual I/O instruction through the inclusion or exclusion of the first byte instruction code. The lower nibble bits of the (M3-0) are don't care ("x"). However, the IO pins should be high-impedance prior to the falling edge of the first data out clock.

If the "Continuous Read Mode" bits M5-4 = (1,0), then the next Fast Read Dual I/O instruction (after /CS is raised and then lowered) does not require the BBh instruction code, as shown in *Figure 7.2.5b*. This reduces the instruction sequence by eight clocks and allows the Read address to be immediately entered after /CS is asserted low. If the "Continuous Read Mode" bits M5-4 do not equal to (1,0), the next instruction (after /CS is raised and then lowered) requires the first byte instruction code, thus returning to normal operation. It is recommended to input FFh on SI for the next instruction (16 clocks), to ensure M4 = 1 and return the device to normal operation.

Figure 7.2.5a. Fast Read Dual I/O Instruction (Initial instruction or previous M5-4≠10)

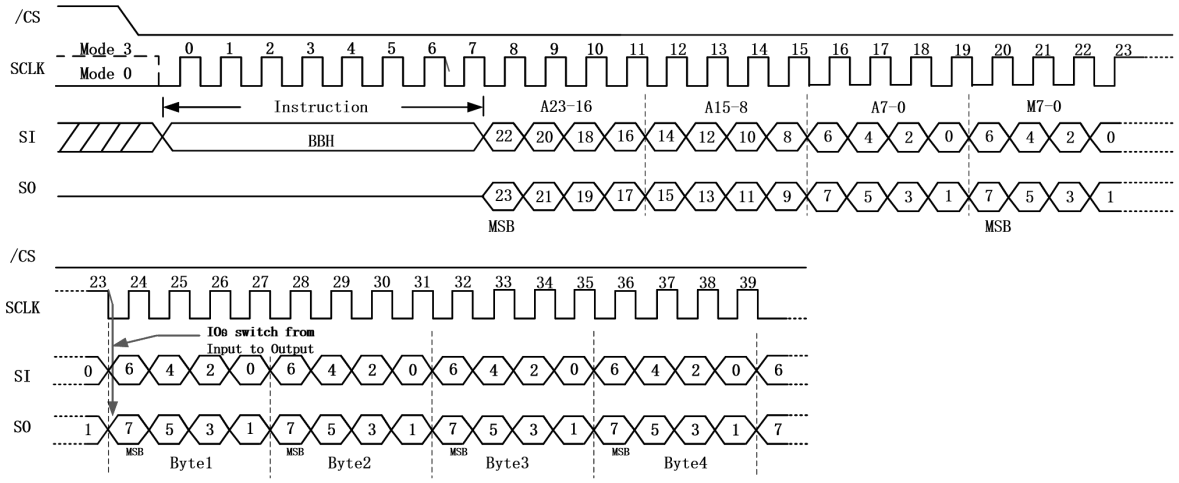
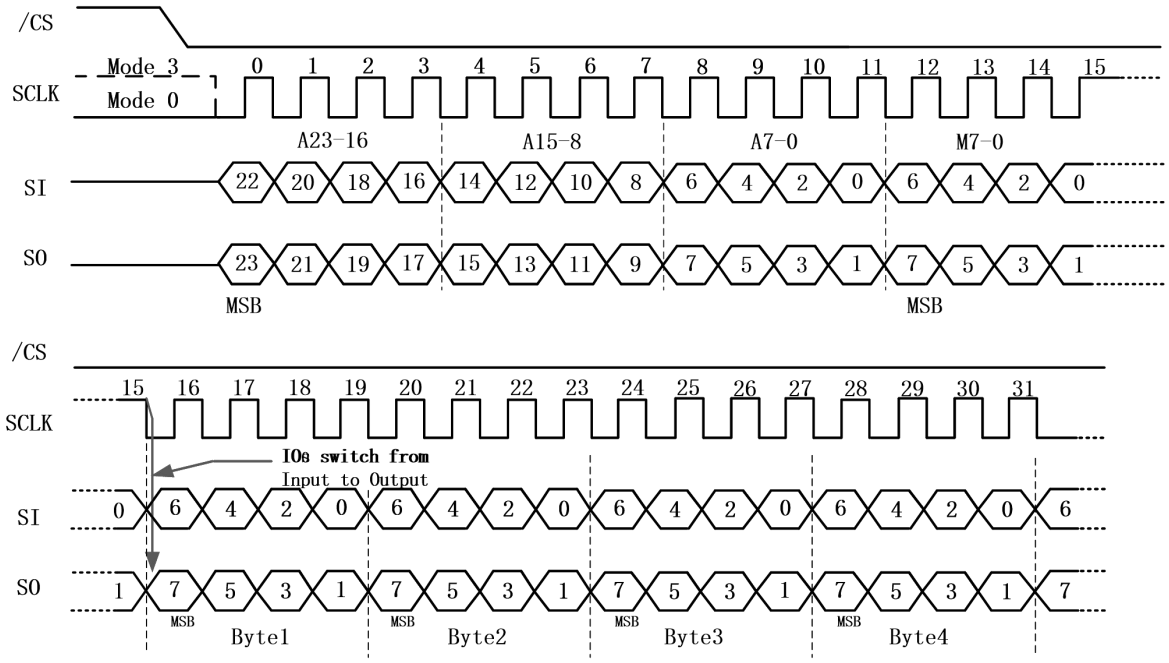


Figure 7.2.5b. Fast Read Dual I/O Instruction (Previous instruction set M5-4 = 10)



7.2.6 Fast Read Quad I/O (EBh)

The Fast Read Quad I/O (EBh) instruction is similar to the *Fast Read Dual I/O (BBh)* instruction except that address and data bits are input and output through two pins SI, SO, /WP and /HOLD and four Dummy clocks are required in SPI mode prior to the data output. The Quad I/O dramatically reduces instruction overhead allowing faster random access for code execution (XIP) directly from the Quad SPI. The Quad Enable bit (QE) of Status Register-2 must be set to enable the Fast Read Quad I/O Instruction.

For 6-pin package, Quad SPI function is not available.

Fast Read Quad I/O with "Continuous Read Mode"

The Fast Read Quad I/O instruction can operate at the highest possible frequency of fC (see *AC Electrical Characteristics*). The Fast Read Quad I/O instruction can further reduce instruction overhead through setting the "Continuous Read Mode" bits (M7-0) after the input Address bits (A23-0), as shown in *Figure 7.2.6a*. The upper nibble of the (M7-4) controls the length of the next Fast Read Quad I/O instruction through the inclusion or exclusion of the first byte instruction code. The lower nibble bits of the (M3-0) are don't care ("x"). However, the IO pins should be high-impedance prior to the falling edge of the first data out clock.

If the "Continuous Read Mode" bits M5-4 = (1,0), then the next Fast Read Quad I/O instruction (after /CS is raised and then lowered) does not require the EBh instruction code, as shown in *Figure 7.2.6b*. This reduces the instruction sequence by eight clocks and allows the Read address to be immediately entered after /CS is asserted low. If the "Continuous Read Mode" bits M5-4 do not equal to (1,0), the next instruction (after /CS is raised and then lowered) requires the first byte instruction code, thus returning to normal operation. It is recommended to input FFh on SI for the next instruction (8 clocks), to ensure M4 = 1 and return the device to normal operation.

Figure 7.2.6a. Fast Read Quad I/O Instruction (Initial instruction or previous M5-4≠10)

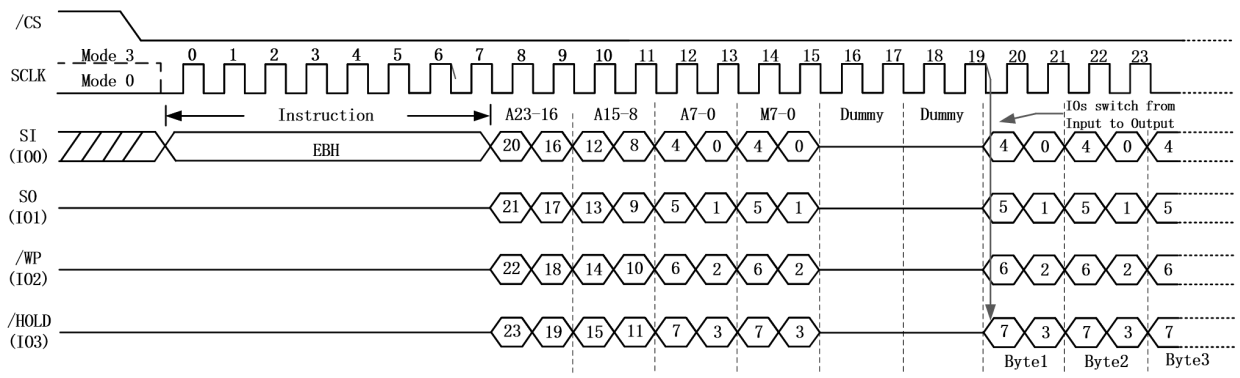
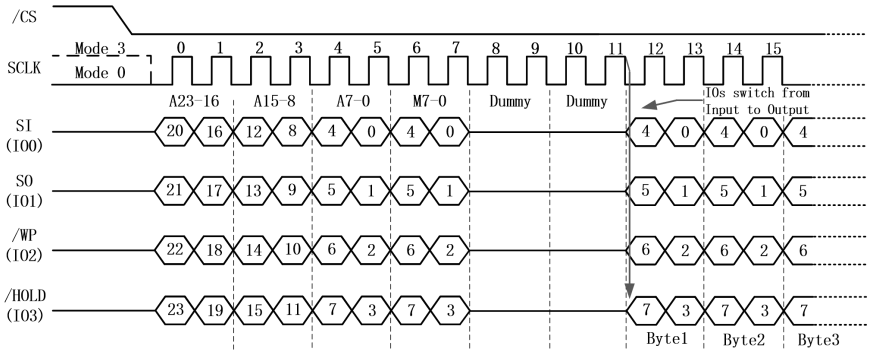


Figure 7.2.6b. Fast Read Quad I/O Instruction (Previous instruction set M5-4 = 10)



Fast Read Quad I/O with "8/16/32/64-Byte Wrap Around" in Standard SPI mode

The Fast Read Quad I/O instruction can also be used to access a specific portion within a page by issuing a "*Set Burst with Wrap*" (77h) instruction prior to EBh. The "Set Burst with Wrap" (77h) instruction can either enable or disable the "Wrap Around" feature for the following EBh instructions. When "Wrap Around" is enabled, the data being accessed can be limited to an 8, 16, 32 or 64-byte section of a 256-byte page. The output data starts at the initial address specified in the instruction, once it reaches the ending boundary of the 8/16/32/64- byte section, the output will wrap around to the beginning boundary automatically until /CS is pulled high to terminate the instruction.

The Burst with Wrap feature allows applications that use cache to quickly fetch a critical address and then fill the cache afterwards within a fixed length (8/16/32/64-byte) of data without issuing multiple read instructions.

The "Set Burst with Wrap" instruction allows three "Wrap Bits", W6-4 to be set. The W4 bit is used to enable or disable the "Wrap Around" operation while W6-5 are used to specify the length of the wrap around section within a page. Refer to section 7.2.7 for detail descriptions.

7.2.7 Set Burst with Wrap (77h)

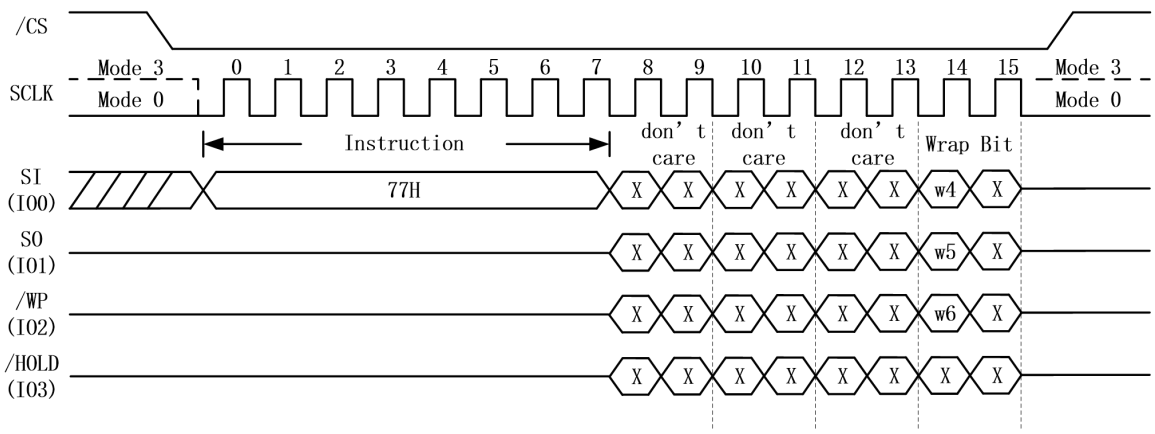
The Set Burst with Wrap (77h) instruction is used in conjunction with "*Fast Read Quad I/O (EBh)",* "instructions to access a fixed length of 8/16/32/64-byte section within a 256-byte page. Certain applications can benefit from this feature and improve the overall system code execution performance.

Similar to a Quad I/O instruction, the Set Burst with Wrap instruction is initiated by driving the /CS pin low and then shifting the instruction code "77h" followed by 24 dummy bits and 8 "Wrap Bits", W7-0. The instruction sequence is shown in *Figure 7.2.8*. Wrap bit W7 and the lower nibble W3-0 are not used.

W6, W5	W4 = 0		W4 =1 (DEFAULT)	
	Wrap Around	Wrap Length	Wrap Around	Wrap Length
0 0	Yes	8-byte	No	N/A
0 1	Yes	16-byte	No	N/A
1 0	Yes	32-byte	No	N/A
1 1	Yes	64-byte	No	N/A

Once W6-4 is set by a Set Burst with Wrap instruction, all the following "*Fast Read Quad I/O (EBh)*", instructions will use the W6-4 setting to access the 8/16/32/64-byte section within any page. To exit the "Wrap Around" function and return to normal read operation, another Set Burst with Wrap instruction should be issued to set W4 = 1. The default value of W4 upon power on or after software reset or hardware rese is 1.

Figure 7.2.8. Set Burst with Wrap Instruction



7.3 ID and Power Instructions

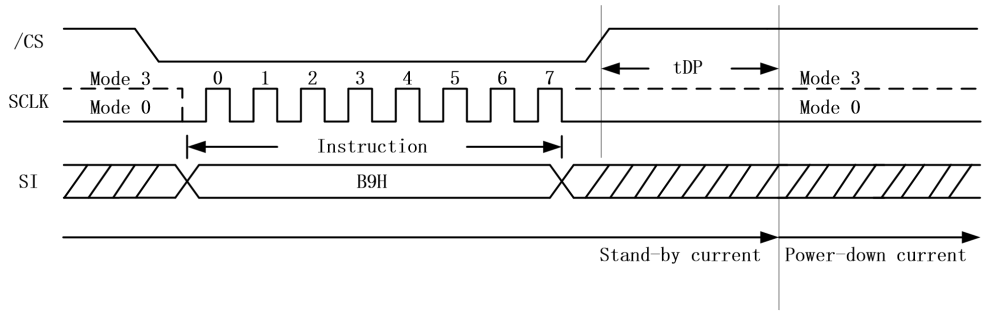
7.3.1 Deep Power-down (B9h)

Although the standby current during normal operation is relatively low, standby current can be further reduced with the Power-down instruction. The lower power consumption makes the Power-down instruction especially useful for battery powered applications (See ICC1 and ICC2 in *DC Characteristics*.)The instruction is initiated by driving the /CS pin low and shifting the instruction code “B9h” as shown in *Figure 7.3.1*

The /CS pin must be driven high after the eighth bit has been latched. If this is not done the Power-down instruction will not be executed. After /CS is driven high, the power- down state will entered within the time duration of tDP (See *AC Characteristics*). While in the power-down state only the *Release Power-down / Device ID (ABh)* instruction, which restores the device to normal operation, will be recognized. All other instructions are ignored. This includes the Read Status Register instruction, which is always available during normal operation. Ignoring all but one instruction makes the Power Down state a useful condition for securing maximum write protection.

The device always powers-up in the normal operation with the standby current of ICC1

Figure 7.3.1. Deep Power-down Instruction



7.3.2 Release Power-down / Device ID (ABh)

The Release from Power-down / Device ID instruction is a multi-purpose instruction. It can be used to release the device from the power-down state, or obtain the devices electronic identification (ID) number.

To release the device from the power- down state, the instruction is issued by driving the /CS pin low, shifting the instruction code “ABh” and driving /CS high as shown in *Figure 7.3.2a*.Release from power-down will take the time duration of tRES1 (See *AC Characteristics*) before the device will resume normal operation and other instructions are accepted. The /CS pin must remain high during the tRES1 time duration.

When used only to obtain the Device ID while not in the power-down state, the instruction is initiated by driving the /CS pin low and shifting the instruction code “ABh” followed by 3-dummy bytes. The Device ID bits are then shifted out on the falling edge of SCLK with most significant bit (MSB) first. The Device ID value for the BY25Q20BL is listed in *Manufacturer and Device Identification table*. The Device ID can be read continuously. The instruction is completed by driving /CS high.

When used to release the device from the power-down state and obtain the Device ID, the instruction is the same as previously described, and shown in *Figure 7.3.2b*, except that after /CS is driven high it must remain high for a time duration of tRES2 (See *AC Characteristics*) . After this time duration the device will resume normal operation and other instructions will be accepted. If the Release from Power- down / Device ID instruction is issued while an Erase, Program or Write cycle is in process (when WIP equals 1) the instruction is ignored and will not have any effects on the current cycle.

Figure 7.3.2a. Release Power-down Instruction

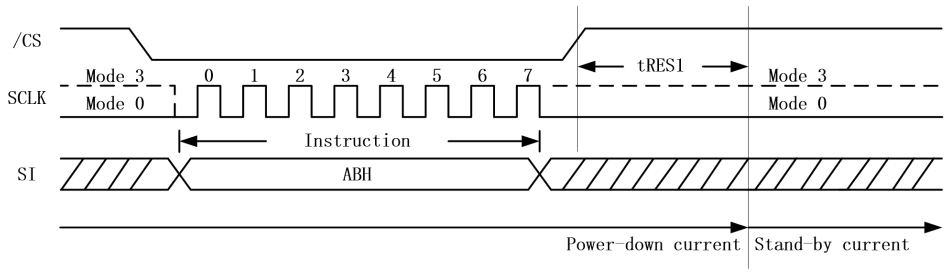
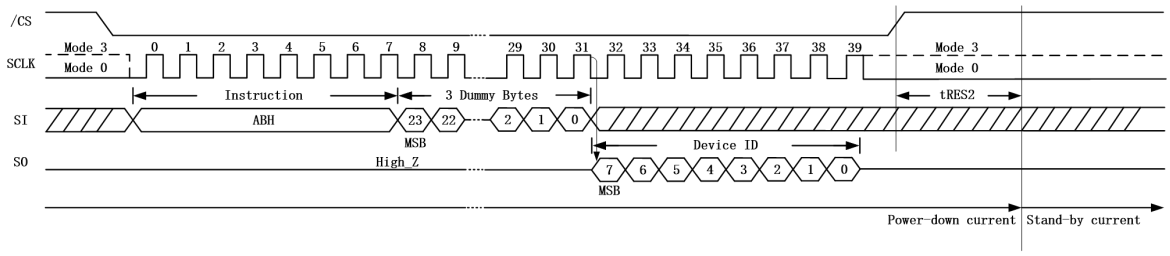


Figure 7.3.2b. Release Power-down / Device ID Instruction

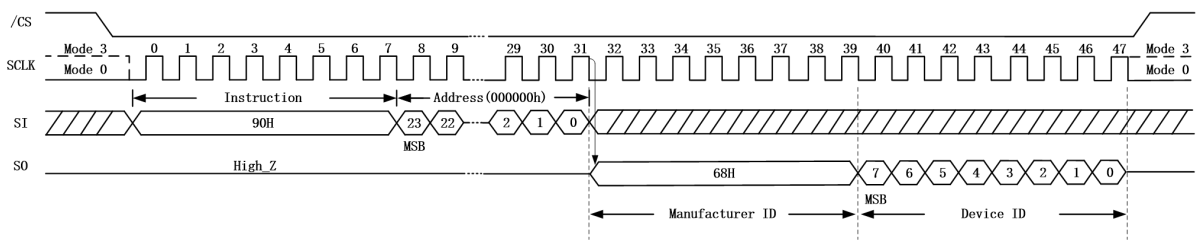


7.3.3 Read Manufacturer / Device ID (90h)

The Read Manufacturer/Device ID instruction is an alternative to the *Release from Power-down / Device ID* instruction that provides both the JEDEC assigned manufacturer ID and the specific device ID.

The Read Manufacturer / Device ID instruction can operate at the highest possible frequency of fC (see *AC Electrical Characteristics*). The instruction is initiated by driving the /CS pin low and shifting the instruction code “90h” followed by a 24-bit address (A23-A0). After which, the Manufacturer ID for BY Technology (68h) and the Device ID are shifted out on the falling edge of SCLK with most significant bit (MSB) first as shown in *Figure 7.3.3*. The Device ID values for the BY25Q20BL are listed in *Manufacturer and Device Identification table*. The address A23-A1 is an unrelated item and has no effect on the result of the instruction. At the same time, if the A0 is initially set to 1 the Device ID will be read first and then followed by the Manufacturer ID. If the A0 is initially set to 0 the Manufacturer ID will be read first and then followed by the Device ID. The Manufacturer and Device IDs can be read continuously, alternating from one to the other. The instruction is completed by driving /CS high.

Figure 7.3.3. Read Manufacturer / Device ID Instruction

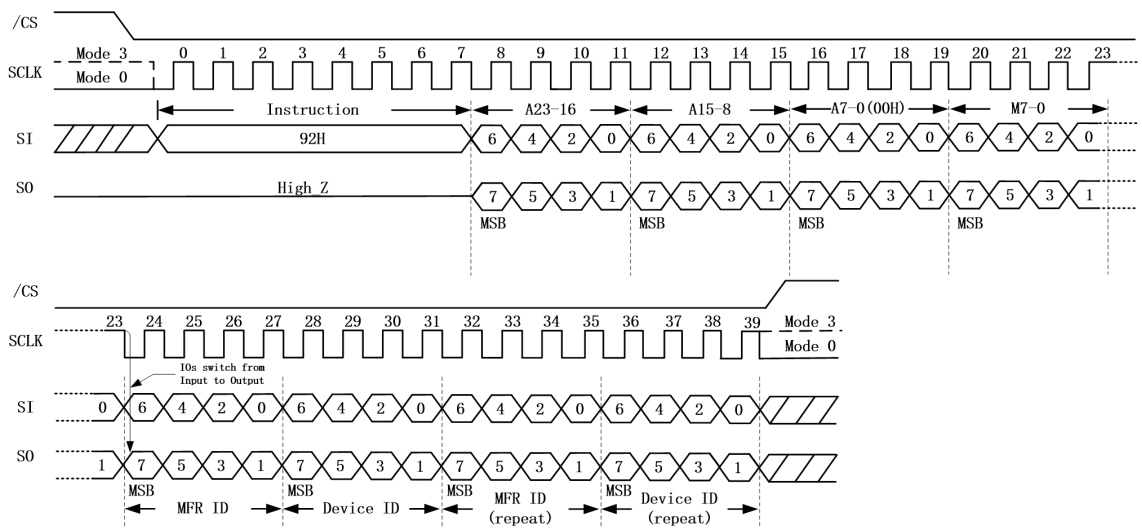


7.3.4 Read Manufacturer / Device ID Dual I/O (92h)

The Read Manufacturer / Device ID Dual I/O instruction is an alternative to the *Read Manufacturer / Device ID* instruction that provides both the JEDEC assigned manufacturer ID and the specific device ID at 2x speed.

The Read Manufacturer / Device ID Dual I/O instruction can operate at the highest possible frequency of fC (see *AC Electrical Characteristics*). The instruction is initiated by driving the /CS pin low and shifting the instruction code “92h” followed by a 24-bit address (A23-A0) and four clock dummy cycles, but with the capability to input the Address bits two bits per clock. After which, the Manufacturer ID for BY Technology (68h) and the Device ID are shifted out 2 bits per clock on the falling edge of SCLK with most significant bits (MSB) first as shown in *Figure 7.3.4*. The Device ID values for the BY25Q20BL are listed in *Manufacturer and Device Identification table*. The address A23-A1 and M7-M0 is an unrelated item and has no effect on the result of the instruction. At the same time, if the A0 is initially set to 1 the Device ID will be read first and then followed by the Manufacturer ID. If the A0 is initially set to 0 the Manufacturer ID will be read first and then followed by the Device ID. The Manufacturer and Device IDs can be read continuously, alternating from one to the other. The instruction is completed by driving /CS high.

Figure 7.3.4. Read Manufacturer / Device ID Dual I/O Instruction



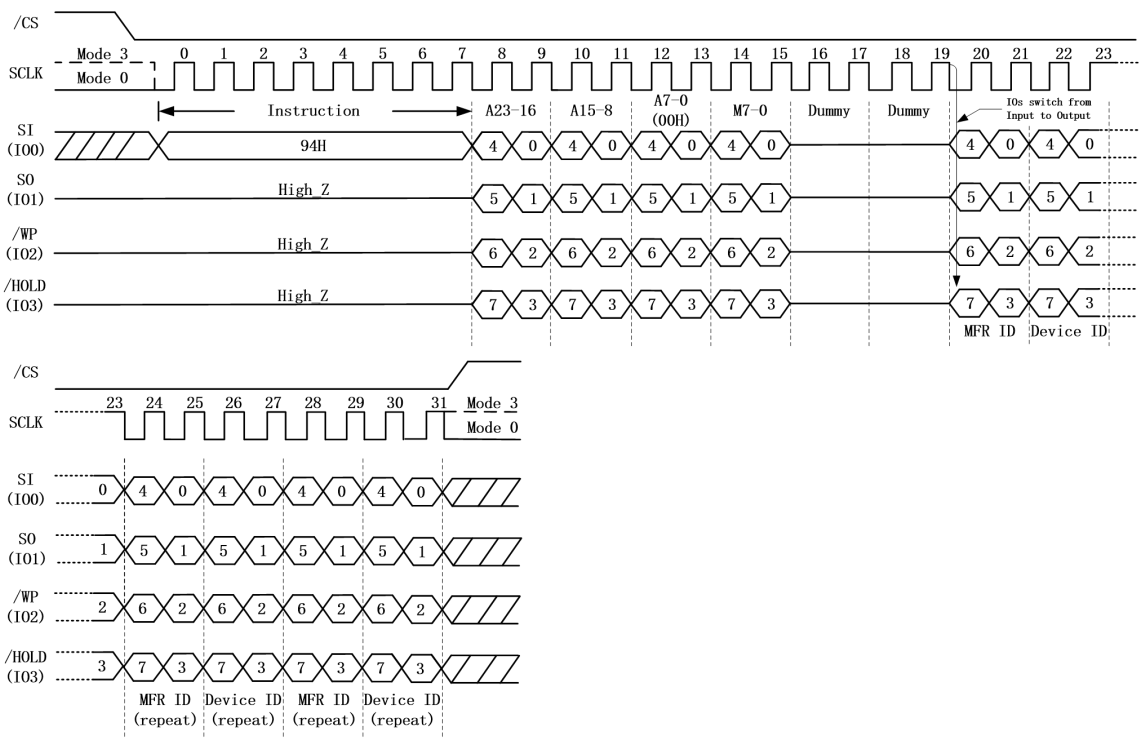
7.3.5 Read Manufacturer / Device ID Quad I/O (94h)

The Read Manufacturer / Device ID Quad I/O instruction is an alternative to the *Read Manufacturer / Device ID* instruction that provides both the JEDEC assigned manufacturer ID and the specific device ID at 4x speed.

The Read Manufacturer / Device ID Quad I/O instruction can operate at the highest possible frequency of fC (see *AC Electrical Characteristics*). The instruction is initiated by driving the /CS pin low and shifting the instruction code “94h” followed by a 24-bit address (A23-A0) and six clock dummy cycles, but with the capability to input the Address bits four bits per clock. After which, the Manufacturer ID for BY Technology (68h) and the Device ID are shifted out four bits per clock on the falling edge of SCLK with most significant bit (MSB) first as shown in *Figure 7.3.5*. The Device ID values for the BY25Q20BL are listed in *Manufacturer and Device Identification table*. The address A23-A1 and M7-M0 is an unrelated item and has no effect on the result of the instruction. At the same time, if the A0 is initially set to 1 the Device ID will be read first and then followed by the Manufacturer ID. If the A0 is initially set to 0 the Manufacturer ID will be read first and then followed by the Device ID. The Manufacturer and Device IDs can be read continuously, alternating from one to the other. The instruction is completed by driving /CS high.

For 6-pin package, Quad SPI function is not available.

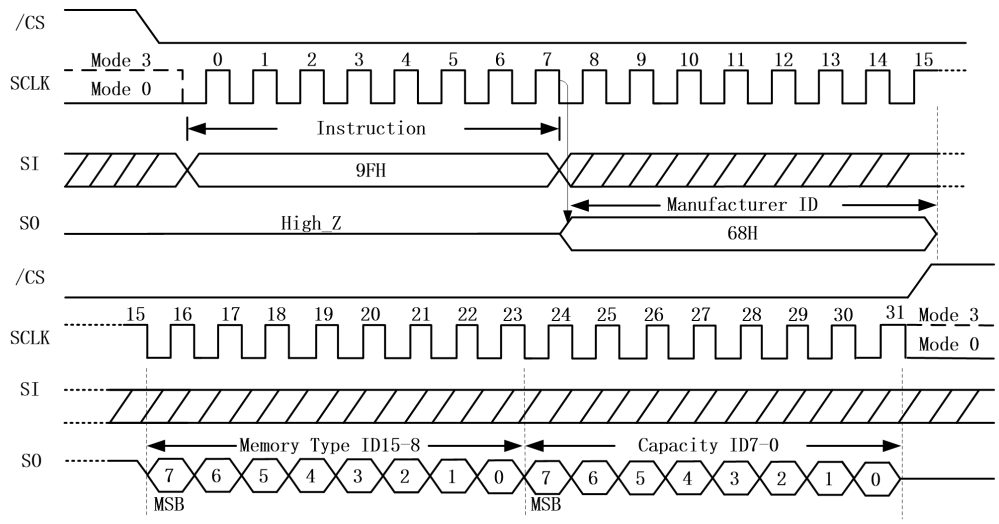
Figure 7.3.5. Read Manufacturer / Device ID Quad I/O Instruction



7.3.6 Read JEDEC ID (9Fh)

The Read JEDEC ID instruction can operate at the highest possible frequency of fC (see *AC Electrical Characteristics*). For compatibility reasons, the BY25Q20BL provides several instructions to electronically determine the identity of the device. The Read JEDEC ID instruction is compatible with the JEDEC standard for SPI compatible serial memories that was adopted in 2003. The instruction is initiated by driving the /CS pin low and shifting the instruction code “9Fh”. The JEDEC assigned Manufacturer ID byte for BY Technology (68h) and two Device ID bytes, Memory Type (ID15-ID8) and Capacity (ID7-ID0) are then shifted out on the falling edge of SCLK with most significant bit (MSB) first as shown in *Figure 7.3.6*. For memory type and capacity values refer to *Manufacturer and Device Identification table*.

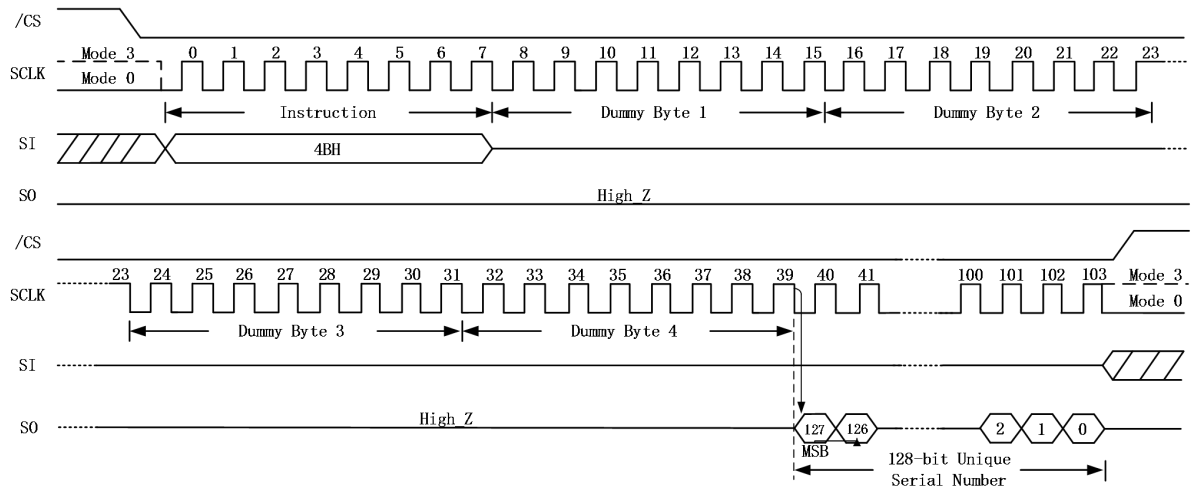
Figure 7.3.6. Read JEDEC ID Instruction



7.3.7 Read Unique ID Number (4Bh)

The Read Unique ID Number instruction can operate at the highest possible frequency of fC (see *AC Electrical Characteristics*).The Read Unique ID Number instruction accesses a factory-set read-only 128-bit number that is unique to each BY25Q20BL device. The ID number can be used in conjunction with user software methods to help prevent copying or cloning of a system. The Read Unique ID instruction is initiated by driving the /CS pin low and shifting the instruction code "4Bh" followed by a four bytes of dummy clocks. After which, the 128-bit ID is shifted out on the falling edge of SCLK as shown in *Figure 7.3.7.*

Figure 7.3.7. Read Unique ID Sequence Diagram



7.4 Program / Erase and Security Instructions

7.4.1 Page Program (02h)

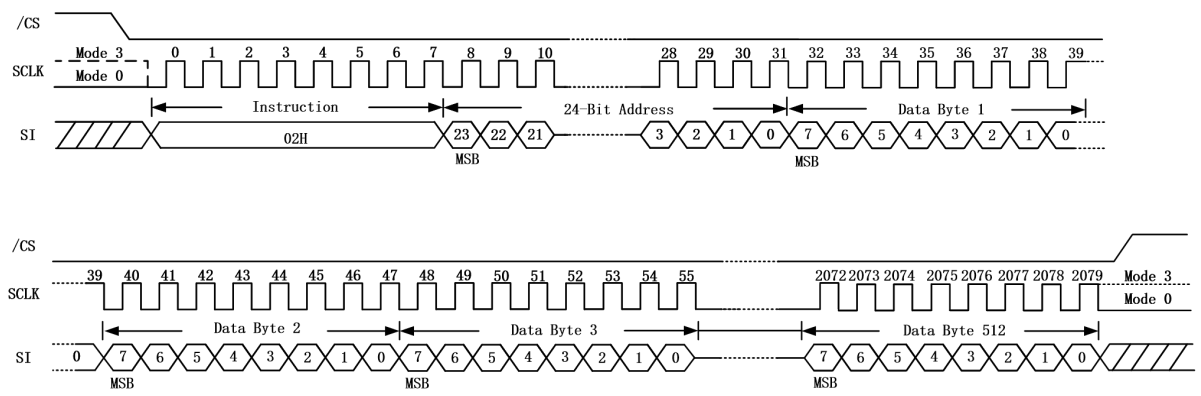
The Page Program instruction allows from one byte to 256 bytes (a page) of data to be programmed at previously erased (FFh) memory locations. A Write Enable instruction must be

executed before the device will accept the Page Program Instruction (Status Register bit WEL= 1). The instruction is initiated by driving the /CS pin low then shifting the instruction code “02h” followed by a 24-bit address (A23-A0) and at least one data byte, into the SI pin. The /CS pin must be held low for the entire length of the instruction while data is being sent to the device. The Page Program instruction sequence is shown in *Figure 7.4.1*.

If more than 256 bytes are sent to the device, previously latched data are discarded and the last 256 data bytes are guaranteed to be programmed correctly within the same page. If less than 256 data bytes are sent to device, they are correctly programmed at the requested addresses without having any effects on the other bytes of the same page. /CS must be driven high after the eighth bit of the last data byte has been latched in; otherwise the Page Program instruction is not executed.

As with the write and erase instructions, the /CS pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Page Program instruction will not be executed. After /CS is driven high, the self-timed Page Program instruction will commence for a time duration of tPP (See *AC Characteristics*). While the Page Program cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the WIP bit. The WIP bit is a 1 during the Page Program cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Page Program cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Page Program instruction will not be executed if the addressed page is protected by the Block Protect (BP4, BP3, BP2, BP1, and BP0) bits

Figure 7.4.1. Page Program Instruction

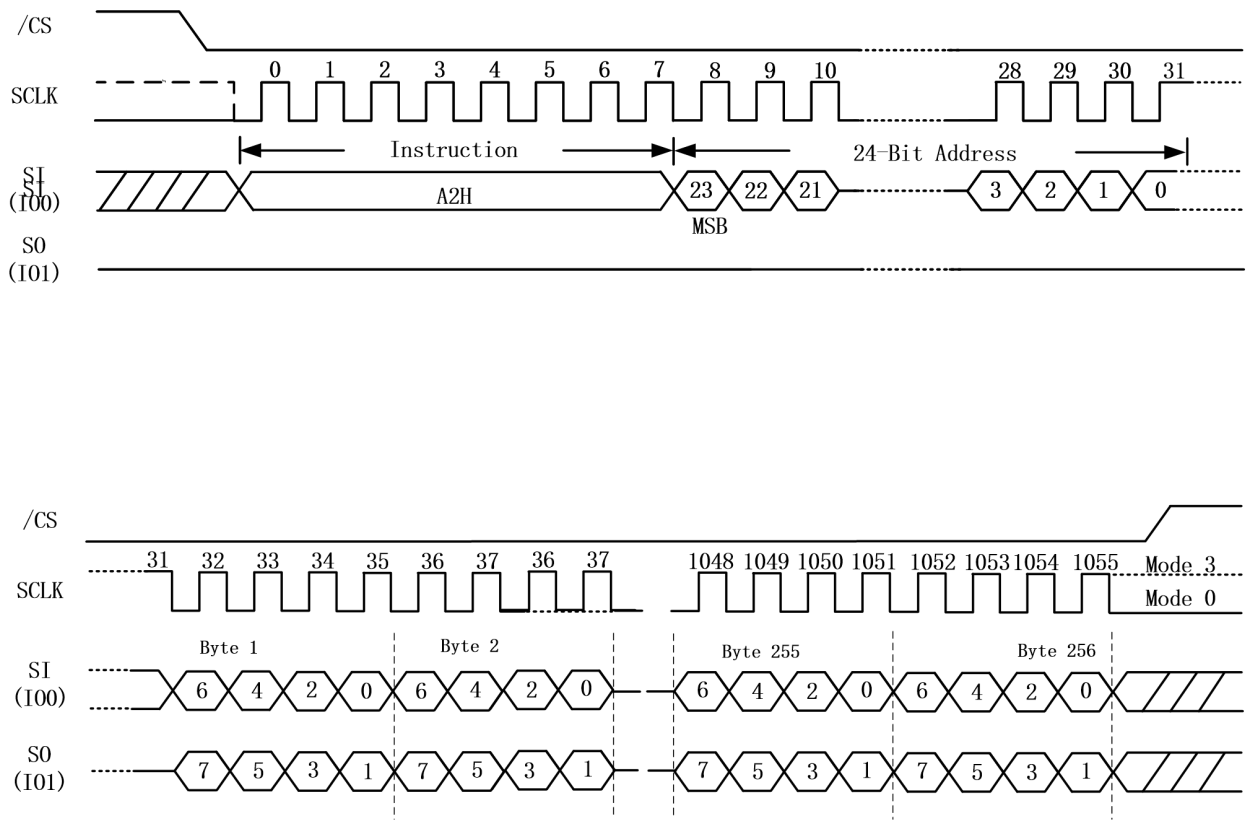


7.4.2 Dual Page Program (A2h)

The Dual Page Program instruction allows up to 256 bytes of data to be programmed at previously erased (FFh) memory locations using two pins: SI, SO. The Dual Page Program can improve performance for PROM Programmer and applications that have slow clock speeds <5MHz. Systems with faster clock speed will not realize much benefit for the Dual Page Program instruction since the inherent page program time is much longer than the time it take to clock-in the data.

A Write Enable instruction must be executed before the device will accept the Dual Page Program instruction (Status Register-1, WEL=1). The instruction is initiated by driving the /CS pin low then shifting the instruction code “A2h” followed by a 24-bit address (A23-A0) and at least one data byte, into the IO pins. The /CS pin must be held low for the entire length of the instruction while data is being sent to the device. All other functions of Dual input Page Program are identical to standard Page Program. The Dual Page Program instruction sequence is shown in *Figure 7.4.2*.

Figure 7.4.2. Dual Page Program Instruction



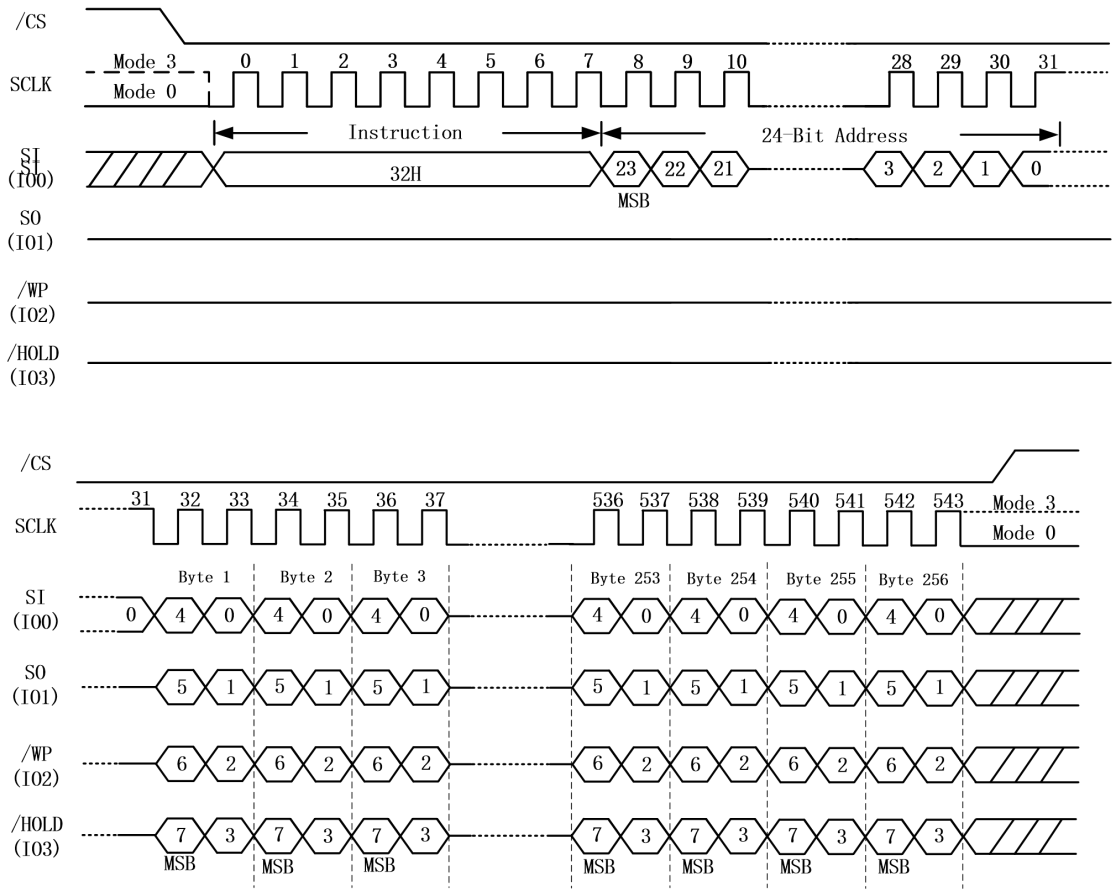
7.4.3 Quad Page Program (32h)

The Quad Page Program instruction allows up to 256 bytes of data to be programmed at previously erased (FFh) memory locations using two pins: SI, SO, /WP, and /HOLD. The Quad Page Program can improve performance for PROM Programmer and applications that have slow clock speeds <5MHz. Systems with faster clock speed will not realize much benefit for the Quad Page Program instruction since the inherent page program time is much longer than the time it take to clock-in the data.

To use Quad Page Program the Quad Enable (QE) bit in Status Register-2 must be set to 1. A Write Enable instruction must be executed before the device will accept the Quad Page Program instruction (Status Register-1, WEL=1). The instruction is initiated by driving the /CS pin low then shifting the instruction code “32h” followed by a 24-bit address (A23-A0) and at least one data byte, into the IO pins. The /CS pin must be held low for the entire length of the instruction while data is being sent to the device. All other functions of Quad Page Program are identical to standard Page Program. The Quad Page Program instruction sequence is shown in *Figure 7.4.3*.

For 6-pin package, Quad SPI function is not available.

Figure 7.4.3. Quad Input Page Program Instruction



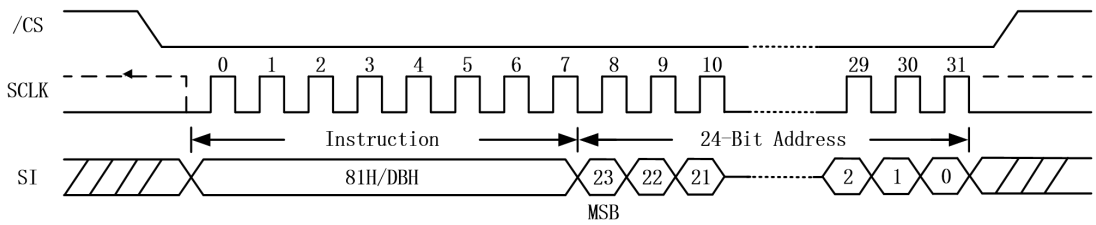
7.4.4 Page Erase (81h/DBh)

The Page Erase (PE) instruction is for erasing the data of the chosen Page to be "1". A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit before sending the Page Erase (PE).

To perform a Page Erase with the standard page size (256 bytes), an instruction code of 81h or DBh must be clocked into the device followed by three address bytes comprised of 2 page address bytes that specify the page in the main memory to be erased. And A7-A0 is an unrelated item.

The sequence of issuing PE instruction is: /CS goes low → sending PE instruction code→ 3-byte address on SI → /CS goes high.

Figure 7.4.4. Page Erase Instruction

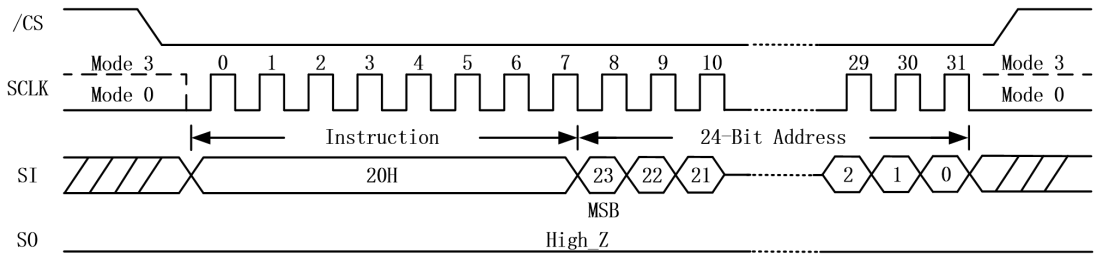


7.4.5 Sector Erase (20h)

The Sector Erase instruction sets all memory within a specified sector (4K-bytes) to the erased state of all 1s (FFh). A *Write Enable* instruction must be executed before the device will accept the Sector Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the /CS pin low and shifting the instruction code “20h” followed a 24-bit sector address. And the address A11-A0 is an unrelated item and has no effect on the result of the instruction. The Sector Erase instruction sequence is shown in *Figure 7.4.5*.

The /CS pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Sector Erase instruction will not be executed. After /CS is driven high, the self-timed Sector Erase instruction will commence for a time duration of tSE (See *AC Characteristics*). While the Sector Erase cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the WIP bit. The WIP bit is a 1 during the Sector Erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Sector Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Sector Erase instruction will not be executed if the addressed page is protected by the Block Protect (BP4, BP3, BP2, BP1, and BP0) bits.

Figure 7.4.5. Sector Erase Instruction

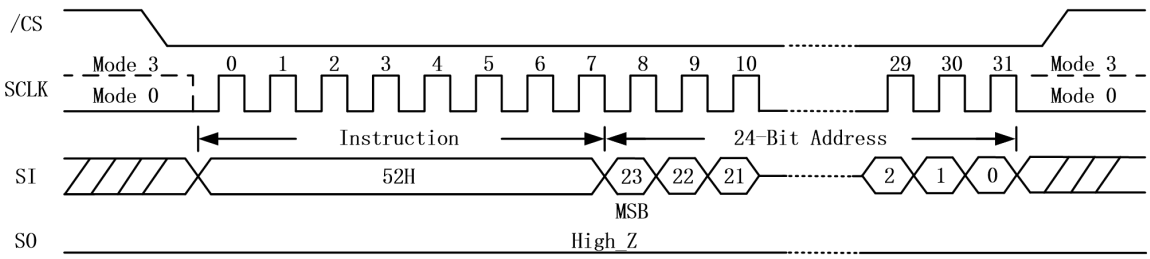


7.4.6 32KB Block Erase (52h)

The 32KB Block Erase instruction sets all memory within a specified block (32K-bytes) to the erased state of all 1s (FFh). A *Write Enable* instruction must be executed before the device will accept the 32KB Block Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the /CS pin low and shifting the instruction code “52h” followed a 24-bit block address (A23-A0). And the address A14-A0 is an unrelated item and has no effect on the result of the instruction. The Block Erase instruction sequence is shown in *Figure 7.4.6*.

The /CS pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the 32KB Block Erase instruction will not be executed. After /CS is driven high, the self-timed 32KB Block Erase instruction will commence for a time duration of tBE1 (See *AC Characteristics*). While the 32KB Block Erase cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the WIP bit. The WIP bit is a 1 during the 32KB Block Erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the 32KB Block Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The 32KB Block Erase instruction will not be executed if the addressed page is protected by the Block Protect (BP4, BP3, BP2, BP1, and BP0) bits.

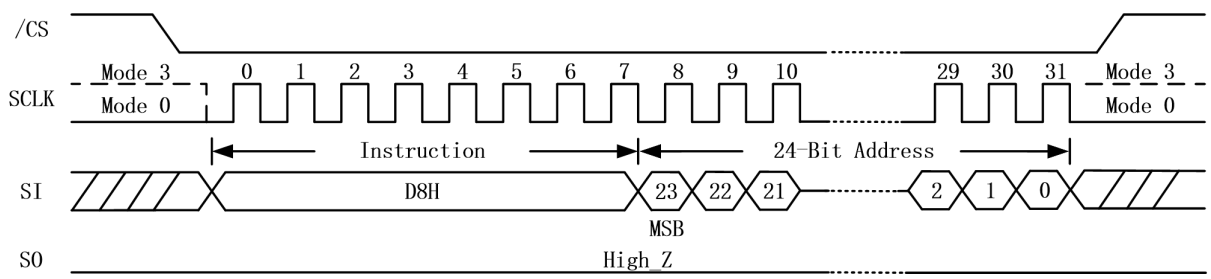
Figure 7.4.6. 32KB Block Erase Instruction



7.4.7 64KB Block Erase (D8h)

The 64KB Block Erase instruction sets all memory within a specified block (64K-bytes) to the erased state of all 1s (FFh). A *Write Enable* instruction must be executed before the device will accept the 64KB Block Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the /CS pin low and shifting the instruction code “D8h” followed a 24-bit block address (A23-A0). And the address A15-A0 is an unrelated item and has no effect on the result of the instruction. The 64KB Block Erase instruction sequence is shown in *Figure 7.4.7*.
The /CS pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the 64KB Block Erase instruction will not be executed. After /CS is driven high, the self-timed 64KB Block Erase instruction will commence for a time duration of tBE2 (See *AC Characteristics*) . While the 64KB Block Erase cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the WIP bit. The WIP bit is a 1 during the 64KB Block Erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the 64KB Block Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The 64KB Block Erase instruction will not be executed if the addressed page is protected by the Block Protect (BP4, BP3, BP2, BP1, and BP0) bits.

Figure 7.4.7. 64KB Block Erase Instruction

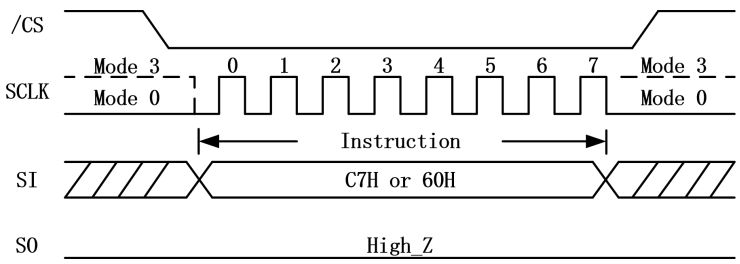


7.4.8 Chip Erase (C7h / 60h)

The Chip Erase instruction sets all memory within the device to the erased state of all 1s (FFh). A *Write Enable* instruction must be executed before the device will accept the Chip Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the /CS pin low and shifting the instruction code “C7h” or “60h”. The Chip Erase instruction sequence is shown in Figure 7.4.8.

The /CS pin must be driven high after the eighth bit has been latched. If this is not done the Chip Erase instruction will not be executed. After /CS is driven high, the self-timed Chip Erase instruction will commence for a time duration of tCE (See *AC Characteristics*). While the Chip Erase cycle is in progress, the Read Status Register instruction may still be accessed to check the status of the WIP bit. The WIP bit is a 1 during the Chip Erase cycle and becomes a 0 when finished and the device is ready to accept other instructions again. After the Chip Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Chip Erase instruction will not be executed if any memory region is protected by the Block Protect (BP4, BP3, BP2, BP1, and BP0) bits.

Figure 7.4.8. Chip Erase Instruction for SPI Mode



7.4.9 Program/Erase Suspend (75h)

The Program/Erase Suspend instruction “75h”, allows the system to interrupt a Page Program or a Page/Sector/32K/64K Block Erase operation and then read data from any other sector or block. After the program or erase operation has entered the suspended state, the memory array can be read except for the page being programmed or the page/sector/block being erased. And after the erase operation has entered the suspended state, the memory array can be programed except for the page/sector/block being erased. Write status register operation can't be suspended. Erase/Program security registers operation can't be suspended. The Program/Erase Suspend instruction sequence is shown in *Figure 7.4.9*.

Readable Area of Memory While a Program or Erase Operation is Suspended

Suspended operation	Readable Region Of Memory Array
Page Program	All but the Page being programmed
Dual Page Program	All but the Page being programmed
Quad Page Program	All but the Page being programmed
Page Erase	All but the Page being Erased
Sector Erase(4KB)	All but the 4KB Sector being Erased
Block Erase(32KB)	All but the 32KB Block being Erased
Block Erase(64KB)	All but the 64KB Block being Erased

When the Serial NOR Flash receives the Suspend instruction, there is a latency of tPSL or tESL before the Write Enable Latch (WEL) bit clears to “0” and the SUS sets to “1”, after which the device is ready to accept one of the commands listed in "Table Acceptable Commands During Program/Erase Suspend after tPSL/tESL" (e.g. FAST READ). Refer to " AC Characteristics" for tPSL and tESL timings. "Table Acceptable instructions During Suspend (tPSL/tESL not required)" lists the Instructions for which the tPSL and tESL latencies do not apply. For example, “05h”, “48h”, “66h” and “99h” can be issued at any time after the Suspend instruction.
Status Register bit 15 (SUS) can be read to check the suspend status. The SUS sets to “1” when a program or erase instruction is suspended. The SUS clears to “0” when the program or erase instruction is resumed.

Acceptable instructions During Program/Erase Suspend after tPSL/tESL

Instruction Name	Instruction code	Suspend Type	
		Program Suspend	Erase Suspend
Read Data	03H	*	*
Fast Read	0BH	*	*
Dual Output Fast Read	3BH	*	*
Dual I/O Fast Read	BBH	*	*
Quad Output Fast Read	6BH	*	*
Quad I/O Fast Read	EBH	*	*
Read SFDP	5AH	*	*
Read JEDEC ID	9FH	*	*
Mftr./Device ID	90H	*	*
Mftr./Device ID Dual IO	92H	*	*
Mftr./Device ID Quad IO	94H	*	*

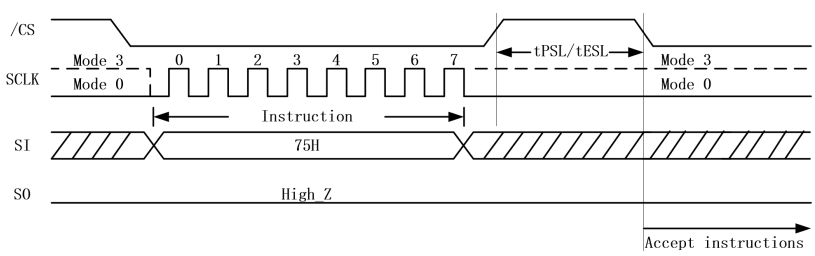
Instruction Name	Instruction code	Suspend Type	
		Program Suspend	Erase Suspend
Read Securty Registers	48H	*	*
Set Burst with Wrap	77H	*	*
Write Enable	06H		*
Write Disable	04H	*	*
Program/Erase Resume	7AH	*	*
Page Program	02H		*
Dual Page Program	A2H		*
Quad Page Program	32H		*
Release Powen-down/Device ID	ABH	*	*

Acceptable Commands During Suspend（tPSL/tESL not required）

Instruction Name	Instruction code	Suspend Type	
		Program Suspend	Erase Suspend
Read Status Register-1	05H	*	*
Read Status Register-2	35H	*	*
Active Status Interrupt	25H	*	*
Enable Reset	66H	*	*
Reset Device	99H	*	*

tPSL: Program Suspend Latency; tESL: Erase Suspend Latency.

Figure 7.4.9. Program/Erase Suspend Instruction

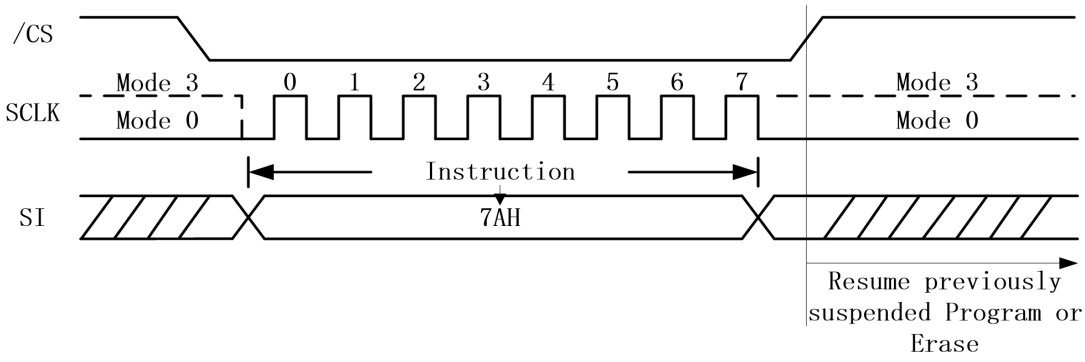


7.4.10 Program/Erase Resume (7Ah)

The Program/Erase Resume instruction “7Ah” must be written to resume the Program or Page / Sector /Block Erase operation after the Program/Erase Suspend. The Program/Erase Resume instruction “7Ah” will be accepted by the device only if the SUS bit in the Status Register equals to 1 and the WIP bit equals to 0. After issued the SUS bit will be cleared from 1 to 0 immediately, the WIP bit will be set from 0 to 1 within 200ns and the Page, Sector or 32/64KBlock will complete the program/erase operation. If the SUS bit equals to 0 or the WIP bit equals to 1, the Program/Erase Resume instruction “7Ah” will be ignored by the device. The Program/Erase Resume instruction sequence is shown in *Figure 7.4.10*.

Program/Erase Resume instruction is ignored if the previous Program/Erase Suspend operation was interrupted by unexpected power off. It is also required that a subsequent Program/Erase Suspend instruction not to be issued within a minimum of time of “tSUS” following a previous Resume instruction.

Figure 7.4.10. Program/Erase Resume Instruction



7.4.11 Erase Security Registers (44h)

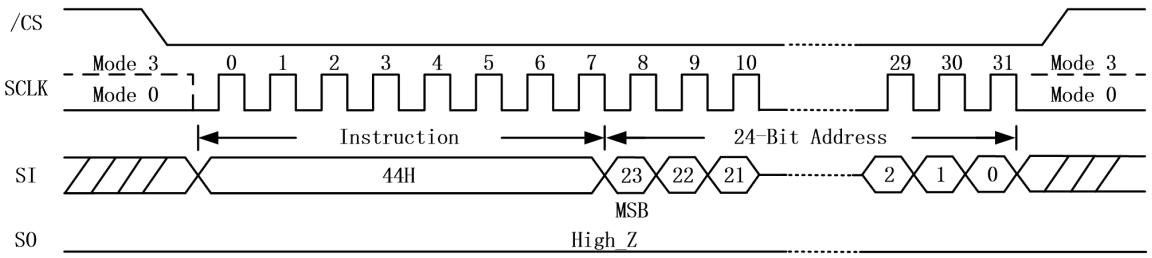
The BY25Q20BL offers three 512-byte Security Registers which can be erased and programmed individually. These registers may be used by the system manufacturers to store security and other important information separately from the main memory array.

The Erase Security Register instruction is similar to the Sector Erase instruction. A Write Enable instruction must be executed before the device will accept the Erase Security Register Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the /CS pin low and shifting the instruction code “44h” followed by a 24-bit address (A23-A0) to erase one of the three security registers.

ADDRESS	A23-16	A15-12	A11-9	A8-0
Security Register #1	00h	0 0 0 1	0 0 0	Don’t Care
Security Register #2	00h	0 0 1 0	0 0 0	Don’t Care
Security Register #3	00h	0 0 1 1	0 0 0	Don’t Care

The Erase Security Register instruction sequence is shown in *Figure 7.4.11*. The /CS pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the instruction will not be executed. After /CS is driven high, the self-timed Erase Security Register operation will commence for a time duration of tSE (See *AC Characteristics*). While the Erase Security Register cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the WIP bit. The WIP bit is a 1 during the erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Erase Security Register cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Security Register Lock Bits (LB3-1) in the Status Register-2 can be used to OTP protect the security registers. Once a lock bit is set to 1, the corresponding security register (LB3-1 corresponds to S13-11) will be permanently locked, Erase Security Register instruction to that register will be ignored (Refer to *section 5.4.1.6* for detail descriptions).

Figure 7.4.11. Erase Security Registers Instruction



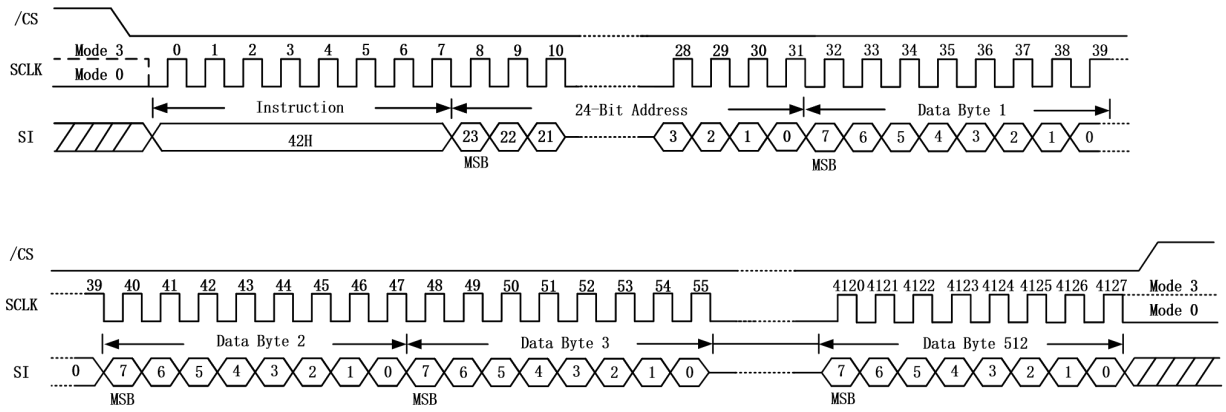
7.4.12 Program Security Registers (42h)

The Program Security Register instruction is similar to the *Page Program* instruction. It allows from one byte to 512 bytes of security register data to be programmed by two times (one time program 256 bytes) at previously erased (FFh) memory locations. A Write Enable instruction must be executed before the device will accept the Program Security Register Instruction (Status Register bit WEL= 1). The instruction is initiated by driving the /CS pin low then shifting the instruction code "42h" followed by a 24- bit address (A23-A0) and at least one data byte, into the SI pin. The /CS pin must be held low for the entire length of the instruction while data is being sent to the device.

ADDRESS	A23-16	A15-12	A11-9	A8-0
Security Register #1	00h	0 0 0 1	0 0 0	Byte Address
Security Register #2	00h	0 0 1 0	0 0 0	Byte Address
Security Register #3	00h	0 0 1 1	0 0 0	Byte Address

The Program Security Register instruction sequence is shown in *Figure 7.4.12*. The Security Register Lock Bits (LB3-1) in the Status Register-2 can be used to OTP protect the security registers. Once a lock bit is set to 1, the corresponding security register will be permanently locked, Program Security Register instruction to that register will be ignored.

Figure 7.4.12. Program Security Registers Instruction

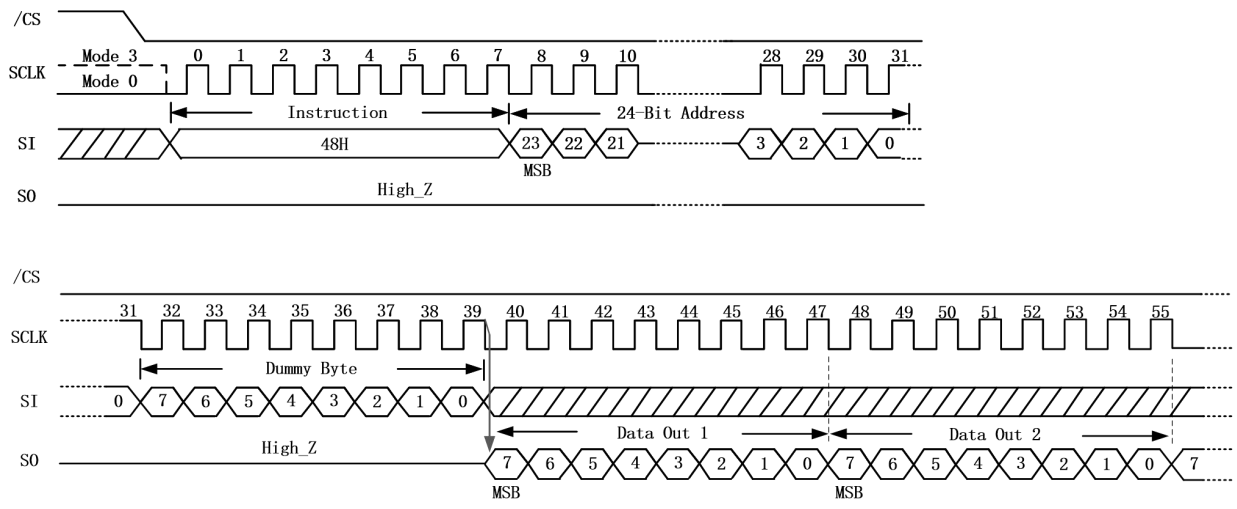


7.4.13 Read Security Registers (48h)

The Read Security Register instruction is similar to the *Fast Read* instruction and allows one or more data bytes to be sequentially read from one of the three security registers. The instruction is initiated by driving the /CS pin low and then shifting the instruction code “48h” followed by a 24-bit address (A23-A0) and eight “dummy” clocks into the SI pin. The code and address bits are latched on the rising edge of the SCLK pin. After the address is received, the data byte of the addressed memory location will be shifted out on the SO pin at the falling edge of SCLK with most significant bit (MSB) first. The byte address is automatically incremented to the next byte address after each byte of data is shifted out. Once the byte address reaches the last byte of the register (byte address FFh), it will reset to address 00h, the first byte of the register, and continue to increment. The instruction is completed by driving /CS high. The Read Security Register instruction sequence is shown in *Figure 7.4.13*. If a Read Security Register instruction is issued while an Erase, Program or Write cycle is in progress (WIP=1) the instruction is ignored and will not have any effects on the current cycle. The Read Security Register instruction allows clock frequency up to to a maximum of fC (see *AC Electrical Characteristics*).

ADDRESS	A23-16	A15-12	A11-9	A8-0
Security Register #1	00h	0 0 0 1	0 0 0	Byte Address
Security Register #2	00h	0 0 1 0	0 0 0	Byte Address
Security Register #3	00h	0 0 1 1	0 0 0	Byte Address

Figure 7.4.13. Read Security Registers Instruction



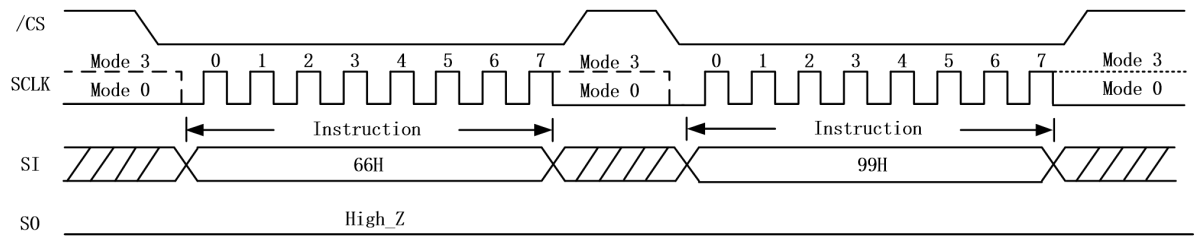
7.4.14 Enable Reset (66h) and Reset Device (99h)

The BY25Q20BL provide a software Reset instruction. Once the Reset instruction is accepted, any on-going internal operations will be terminated and the device will return to its default power-on state and lose all the current volatile settings, such as Volatile Status Register bits, Write Enable Latch (WEL) status, Program/Erase Suspend status, Continuous Read Mode bit setting (M7-M0) , Wrap Bit setting (W6-W4).

To avoid accidental reset, both instructions must be issued in sequence. Any other instructions other than “Reset (99h)” after the “Enable Reset (66h)” instruction will disable the “Reset Enable” state. A new sequence of “Enable Reset (66h)” and “Reset (99h)” is needed to reset the device. Once the Reset instruction is accepted by the device, the device will take tRST to reset. During this period, no instruction will be accepted.

Data corruption may happen if there is an on-going or suspended internal Erase or Program operation when Reset instruction sequence is accepted by the device. It is recommended to check the WIP bit and the SUS bit in Status Register before issuing the Reset instruction sequence.

Figure 7.4.14. Enable Reset and Reset Instruction Sequence



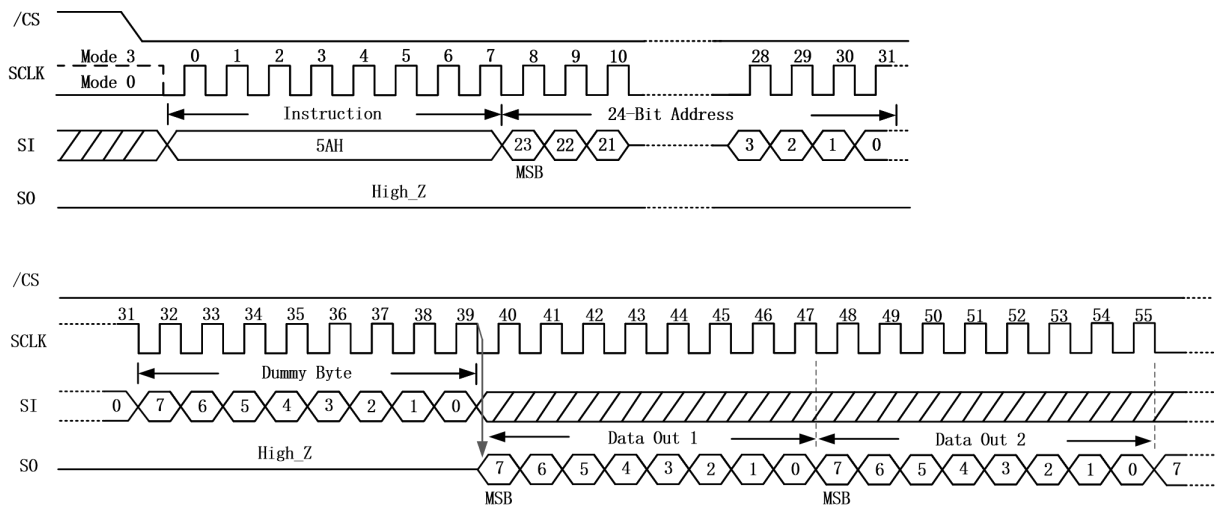
7.4.15 Read Serial Flash Discoverable Parameter (5AH)

The Serial Flash Discoverable Parameter (SFDP) standard provides a consistent method of describing the functional and feature capabilities of serial flash devices in a standard set of internal parameter tables. These parameter tables can be interrogated by host system software to enable adjustments needed to accommodate divergent features from multiple vendors. The concept is similar to the one found in the Introduction of JEDEC Standard, JESD68 on CFI.

SFDP is a JEDEC Standard, JESD216B.

SFDP is a special order. If you need anything, please contact BY Technology

Figure 7.4.15. Read Serial Flash Discoverable Parameter instruction Sequence Diagram



8. Electrical Characteristics

8.1 Absolute Maximum Ratings

PARAMETERS	SYMBOL	CONDITIONS	RANGE	UNIT
Supply Voltage	VCC		–0.6 to VCC+0.6	V
Voltage Applied to Any Pin	VIO	Relative to Ground	–0.6 to VCC+0.6	V
Transient Voltage on any Pin	VIOT	<20nS Transient Relative to Ground	–1.0V to VCC+1.0V	V
Storage Temperature	TSTG		–65 to +150	°C
Lead Temperature	TLEAD		See Note (2)	°C
Electrostatic Discharge Voltage	VESD	Human Body Model(3)	–2000 to +2000	V

Notes:

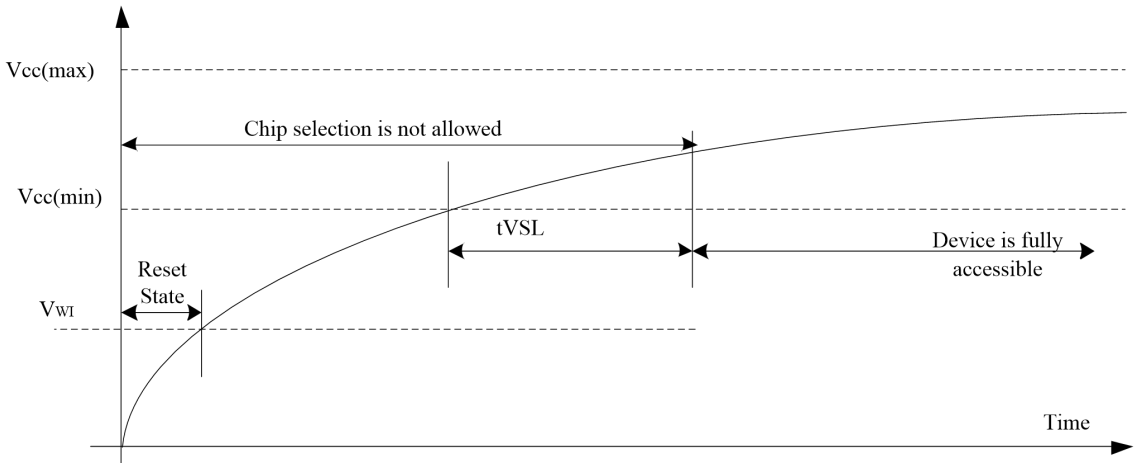
1. This device has been designed and tested for the specified operation ranges. Proper operation outside of these levels is not guaranteed. Exposure to absolute maximum ratings may affect device reliability. Exposure beyond absolute maximum ratings may cause permanent damage.
2. Compliant with JEDEC Standard J-STD-20C for small body Sn-Pb or Pb-free (Green) assembly and the European directive on restrictions on hazardous substances (RoHS) 2002/95/EU.
3. JEDEC Std JESD22-A114A (C1=100pF, R1=1500 ohms, R2=500 ohms)

8.2 Operating Ranges

PARAMETER	SYMBOL	CONDITIONS	SPEC		UNIT
			MIN	MAX	
Supply Voltage(1)	VCC	FR = 108MHz, fR = 50MHz	1.65	2.0	V
Ambient Temperature (Operating)	TA	Industrial	–40	+85	°C

8.3 Power-up Timing and Write Inhibit Threshold

Symbol	Parameter	Min	Max	Unit.
tVSL	VCC(min) To /CS Low	300		us
V_{WI}	Write Inhibit Threshold Voltage V_{WI}	1.0	1.4	V



8.4 DC Electrical Characteristics

(T= -40℃~85℃, VCC=2.7~3.6V)

PARAMETER	SYMBOL	CONDITIONS	SPEC			UNIT
			MIN	TYP	MAX	
Input Capacitance	CIN(1)	VIN = 0V(1)			6	pF
Output Capacitance	Cout(1)	VOUT = 0V(1)			8	pF
Input Leakage	ILI	All inputs at CMOS level			±2	μA
Output Leakage	ILO	All inputs at CMOS level			±2	μA
Standby Current	ICC1	/CS = VCC, VIN = GND or VCC		9		μA
Power-down Current	ICC2	/CS = VCC, VIN = GND or VCC		0.1	0.6	μA
Normal read current (03h)	ICC3	F=1MHz;IOUT=0mA		0.3	0.4	mA
		F=33MHz;IOUT=0mA		0.5	0.8	mA
Read Current(0Bh)	ICC4	F=50MHz;IOUT=0mA		0.8	1.0	mA
		F=85MHz;IOUT=0mA		1.2	1.5	mA
Program Current	ICC5	/CS = VCC WIP=1		1.5	3.0	mA
Erase Current	ICC6	/CS = VCC WIP=1		1.5	3.0	mA
Input Low Voltage	VIL				VCC x 0.2	V
Input High Voltage	VIH		VCC x 0.8			V
Output Low Voltage	VOL	IOL = 100 μA			0.2	V
Output High Voltage	VOH	IOH = –100 μA	VCC – 0.2			V

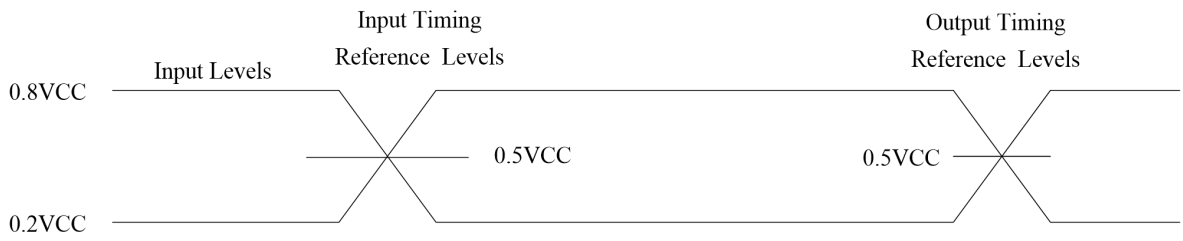
Notes:

1. Tested on sample basis and specified through design and characterization data. TA = 25° C, VCC = 1.8V.

8.5 AC Measurement Conditions

PARAMETER	SYMBOL	SPEC		UNIT
		MIN	MAX	
Input Capacitance	Cin		6	pF
Output Capacitance	Cout		6	pF
Load Capacitance	CL		30	pF
Input Rise and Fall Times	TR, TF		5	ns
Input Pulse Voltages	VIN	0.2 VCC-0.8 VCC		V
Input Timing Reference Voltages	IN	0.5 VCC-0.5 VCC		V
Output Timing Reference Voltages	OUT	0.5 VCC-0.5 VCC		V

AC Measurement I/O Waveform



8.6 AC Electrical Characteristics

(T= -40℃~85℃, VCC=2.7~3.6V)

DESCRIPTION	SYMBOL	ALT	SPEC			UNIT
			MIN	TYP	MAX	
Clock frequency for Normal Read Data instruction	fR				33	MHz
Clock frequency for Read instruction except Normal Read Data instruction (05h,35h,0Bh,3Bh, 6Bh,BBh, EBh,90h,92h,94h,9Fh,4Bh,48h,5Ah)	fC	fC1			85	MHz
Clock High, Low Time	tCLH, tCLL(1)		5.5			ns
Clock Rise Time peak to peak	tCLCH(2)		0.1			V/ns
Clock Fall Time peak to peak	tCHCL(2)		0.1			V/ns
/CS Active Setup Time relative to CLK	tSLCH	tCSS	5			ns
/CS Not Active Hold Time relative to CLK	tCHSL		5			ns
Data In Setup Time	tDVCH	tDSU	2			ns
Data In Hold Time	tCHDX	tDH	3			ns
Output Disable Time	tSHQZ(2)	tDIS			6	ns
/CS Active Hold Time relative to CLK	tCHSH	tCSS	5			ns
/CS Not Active Setup Time relative to CLK	tSHCH		5			ns
/CS Deselect Time from read to next Read	tSHSL	tCSH	15			ns
/CS Deselect Time from Write,Erase,Program TO Read status Register			30			ns
Clock Low to Output Valid loading 30pF	tCLQV	tV			7	ns
Clock Low to Output Valid loading 15pF					6	ns
Output Hold Time	tCLQX	tHO	0			ns
/HOLD Active Setup Time relative to CLK	tHLCH		5			ns
/HOLD Active Hold Time relative to CLK	tCHHH		5			ns
/HOLD Not Active Setup Time relative to CLK	tHHCH		5			ns
/HOLD Not Active Hold Time relative to CLK	tCHHL		5			ns

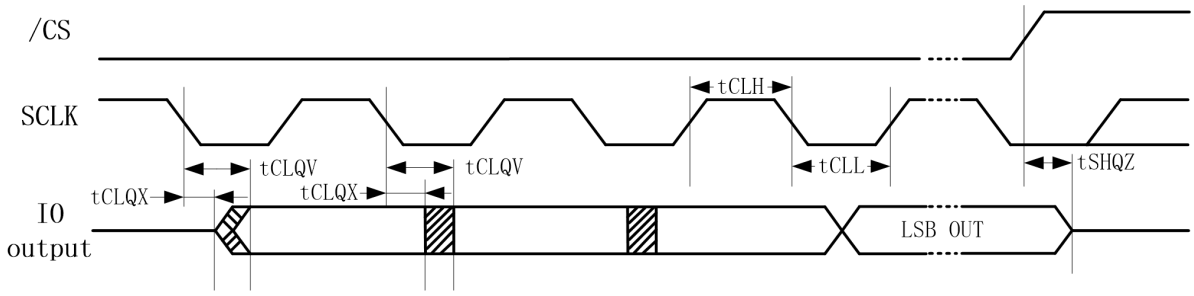
8.7 AC Electrical Characteristics (cont'd)

DESCRIPTION	SYMBOL	ALT	SPEC			UNIT
			MIN	TYP	MAX	
/HOLD to Output Low-Z	tHHQX(2)	tLZ			6	ns
/HOLD to Output High-Z	tHLQZ(2)	tHZ			6	ns
Write Protect Setup Time Before /CS Low	tWHSL(3)		20			ns
Write Protect Hold Time After /CS High	tSHWL(3)		100			ns
/CS High to Deep Power-down Mode	tDP(2)				3	µs
/CS High to Standby Mode without ID Read	tRES1(2)				8	µs
/CS High to Standby Mode with ID Read	tRES2(2)				8	µs
/CS High to next Instruction after Suspend	tSUS(2)				20	µs
/CS High to next Instruction after Reset	tRST(2)		300			µs
Write Status Register Cycle Time	tW			6.5	12	ms
Byte Program Time	tBP1			1	3	ms
Erase Suspend Latency	tESL				30	µs
Program Suspend Latency	tPSL				30	µs
Latency between Program Resume and next Suspend	tPRS		20			µs
Latency between Erase Resume and next Suspend	tERS		20			µs
Page Program Time	tPP			2	3	ms
Page Erase Time	tPE			8	12	ms
Sector Erase Time (4KB)	tSE			8	12	ms
Block Erase Time (32KB)	tBE1			8	12	ms
Block Erase Time (64KB)	tBE2			8	12	ms
Chip Erase Time	tCE			8	12	ms

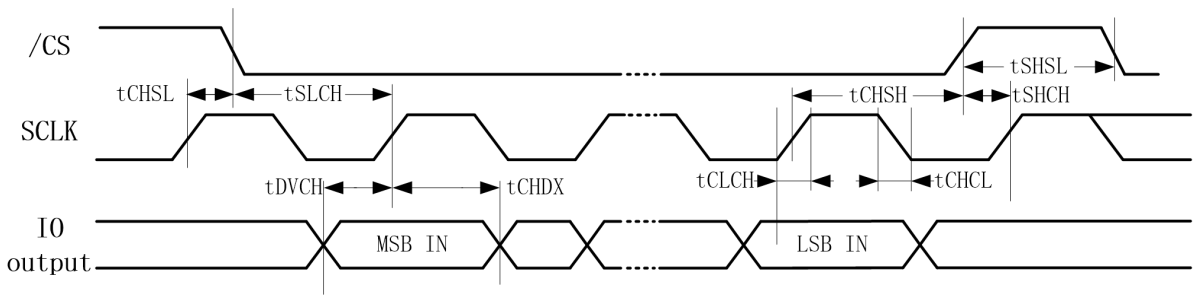
Notes:

1. Clock high + Clock low must be less than or equal to 1/fC.
2. Value guaranteed by design and/or characterization, not 100% tested in production.
3. Only applicable as a constraint for a Write Status Register instruction when SRP[1:0]=(0,1).
4. Tested on sample basis and specified through design and characterization data. TA = 25° C, VCC = 1.8V, 100% driver strength.
5. For 6-pin package, /WP and /HOLD timing is not available.

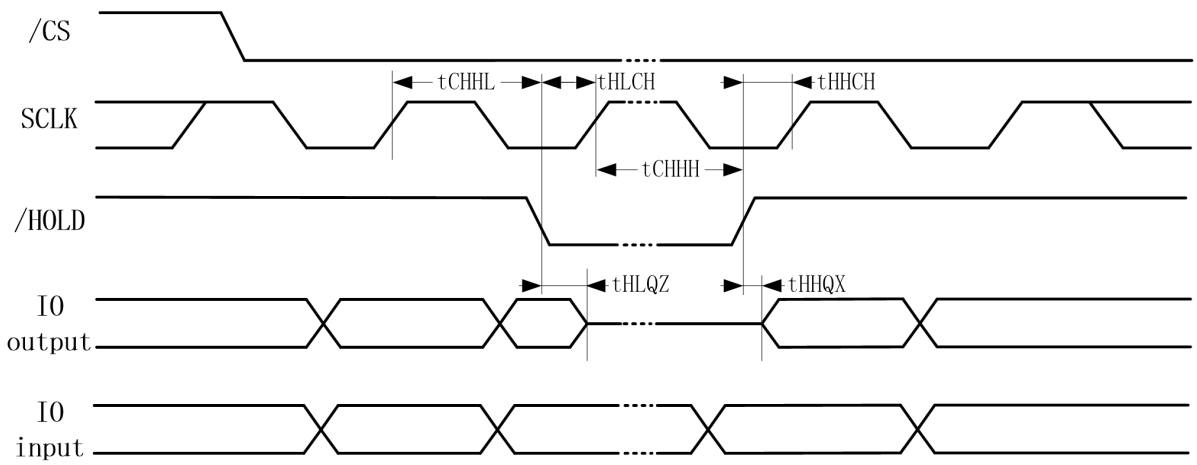
8.8 Serial Output Timing



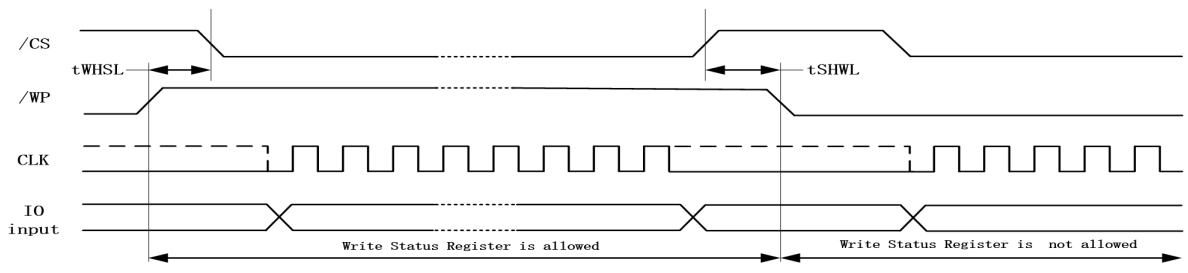
8.9 Serial Input Timing



8.10 /HOLD Timing

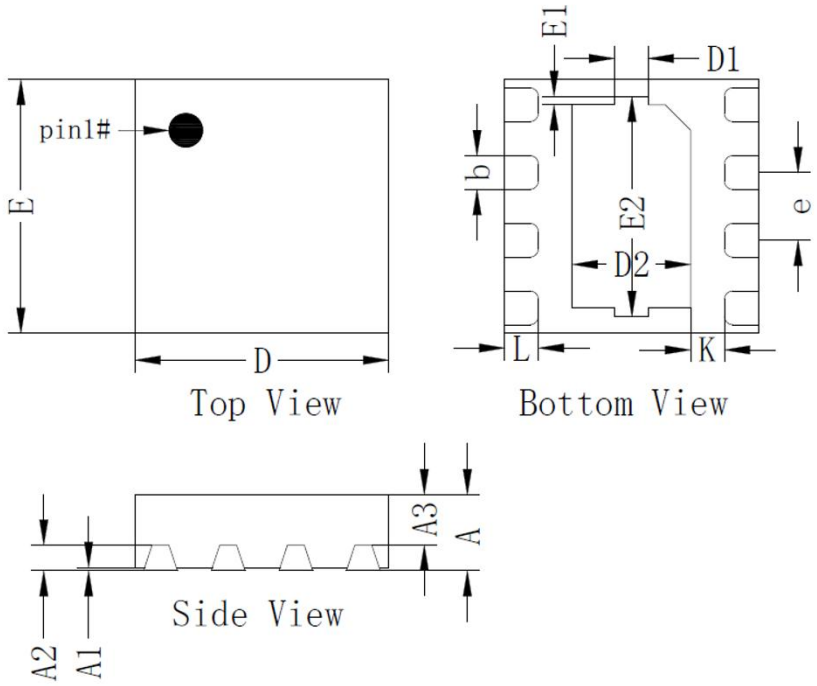


8.11 /WP Timing



9. Package Information

9.1 Package USON8 (1.5*1.5*0.45mm)



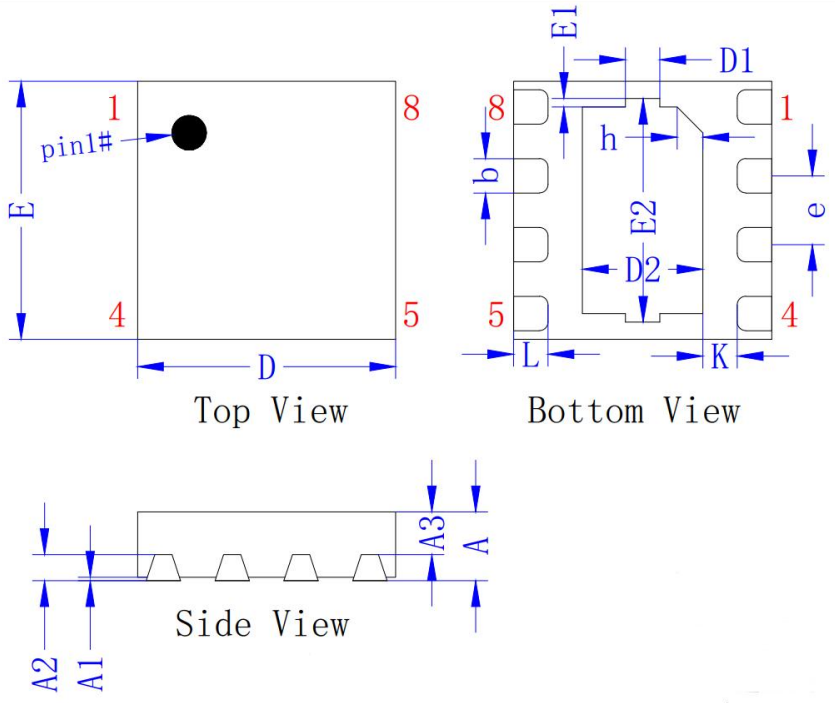
COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETERS)

SYMBOL	MILLMETERS		
	MIN	NOM	MAX
A	0.40	0.45	0.50
A1	0.00	0.02	0.05
A2		0.152REF	
A3	---	0.30	---
D	1.45	1.50	1.55
E	1.45	1.50	1.55
D1		0.20REF	
E1		0.05REF	
D2	0.60	0.70	0.80
E2	1.20	1.30	1.40
e		0.40BSC	
L	0.15	0.20	0.25
b	0.15	0.20	0.25
K		0.20REF	

Note:

1. The exposed metal pad area on the bottom of the package is floating.

9.2 Package USON8 (1.5*1.5*0.40mm)



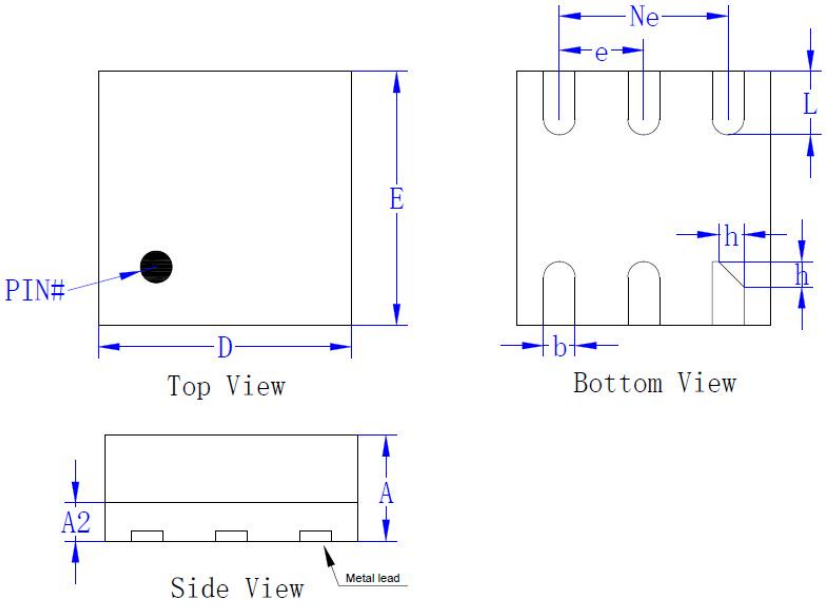
COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETERS)

SYMBOL	MILLMETERS		
	MIN	NOM	MAX
A	0.37	0.40	0.43
A1	0.00	0.02	0.05
A2		0.152 REF	
A3	---	0.25	---
D	1.45	1.50	1.55
E	1.45	1.50	1.55
D1		0.20 REF	
E1		0.05 REF	
D2	0.60	0.70	0.80
E2	1.20	1.30	1.40
e		0.40 BSC	
L	0.10	0.20	0.25
b	0.15	0.20	0.25
K		0.20 REF	
h		0.15 REF	

Note:

1. The exposed metal pad area on the bottom of the package is floating.

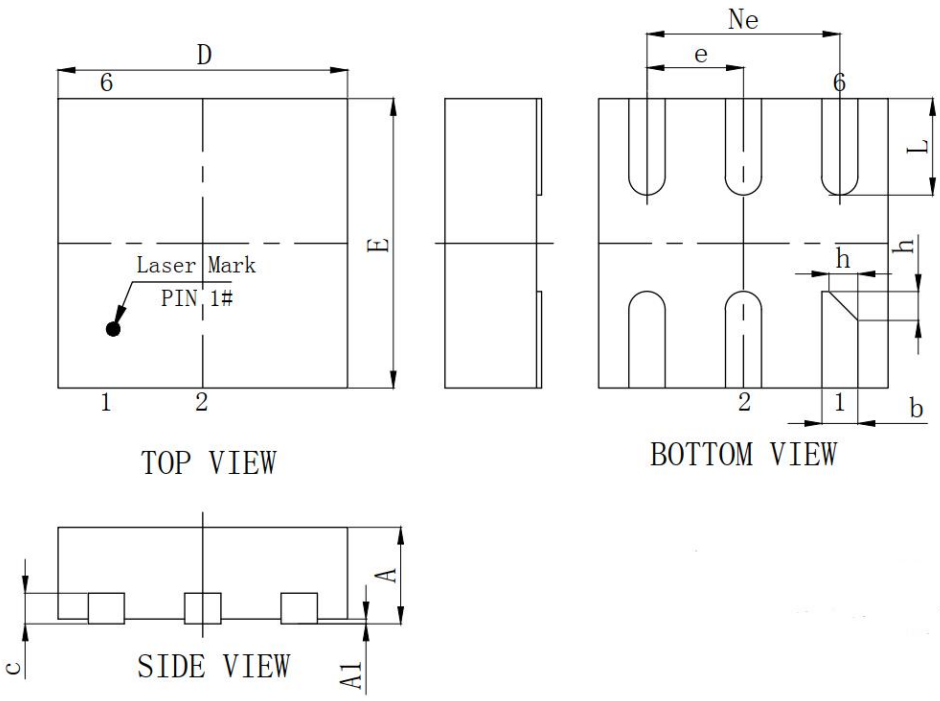
9.3 Package USON6 (1.2*1.2*0.5mm)



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETERS)

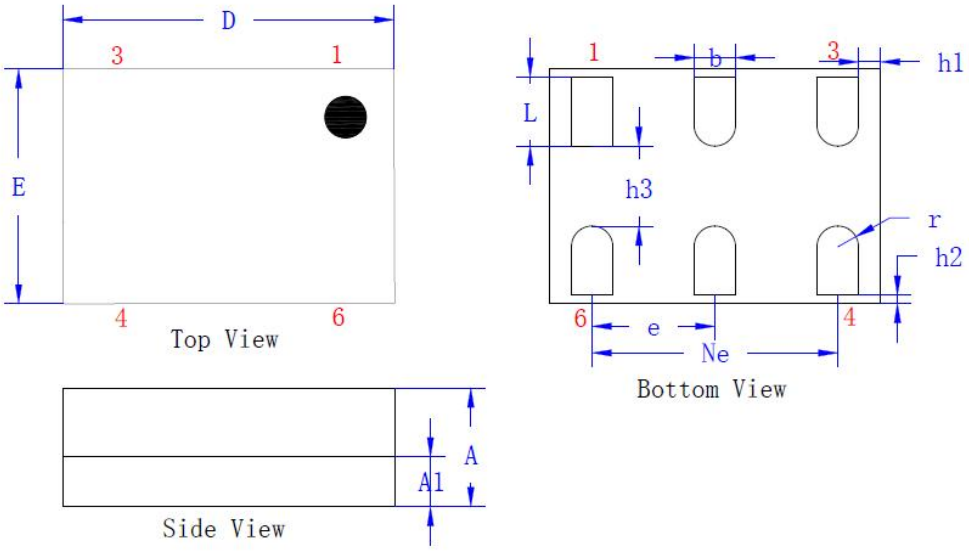
SYMBOL	MILLMETERS		
	MIN	NOM	MAX
A	0.45	0.50	0.55
A2	0.18 REF		
D	1.15	1.20	1.25
E	1.15	1.20	1.25
b	0.10	0.15	0.20
L	0.25	0.30	0.35
e	0.40 BSC		
Ne	0.80 BSC		
h	0.12 REF		

9.4 Package USON6 (1.2*1.2*0.4mm)



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.35	-	0.40
A1	0.00	0.02	0.05
b	0.10	0.15	0.20
c	0.127REF		
D	1.15	1.20	1.25
e	0.40BSC		
Ne	0.80BSC		
E	1.15	1.20	1.25
L	0.35	0.40	0.45
h	0.12REF		

9.5 Package USON6 (0.85*1.2*0.45mm)



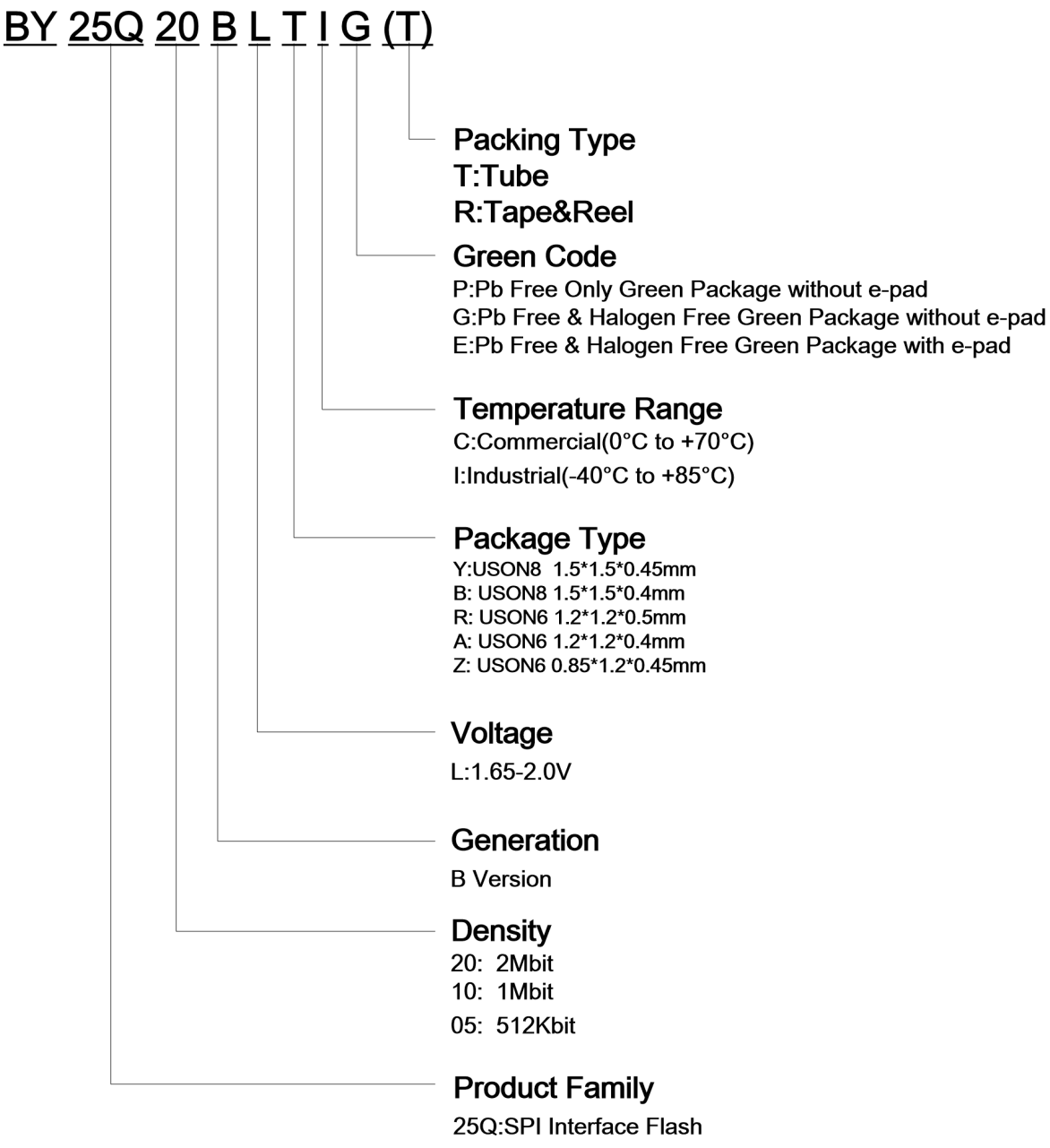
COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETERS)

SYMBOL	MILLMETERS		
	MIN	NOM	MAX
A	0.40	0.45	0.50
A1	0.18 REF		
D	1.15	1.20	1.25
E	0.80	0.85	0.90
b	0.10	0.15	0.20
L	0.20	0.25	0.30
e	0.445 BSC		
Ne	0.89 BSC		
r	0.075 REF		
h1	---	0.08	---
h2	---	0.03	---
h3	---	0.29	---

Note:

1. “USON60.85*1.2*0.45mm” package has not been in mass production, just for engineering samples with no quality assurance.

10. Order Information



Note: “USON60.85*1.2*0.45mm” package has not been in mass production, just for engineering samples with no quality assurance.

10.1 Valid part Numbers and Top Side Marking

The following table provides the valid part numbers for BY25Q20BL SPI Flash Memory. Pls contact BY Technology for specific availability by density and package type.

Package Type	Density	Product Number	Top Side Marking
Y USON8 1.5*1.5*0.45mm	2M-bit	BY25Q20BLYIG	Q20L YYWW
B USON8 1.5*1.5*0.4mm	2M-bit	BY25Q20BLBIG	Q20B YYWW
R USON6 1.2*1.2*0.5mm	2M-bit	BY25Q20BLRIG	BY2L
A USON6 1.2*1.2*0.4mm	2M-bit	BY25Q20BLAIG	BY2A
Z USON6 0.85*1.2*0.45mm	2M-bit	BY25Q20BLZIG	Q20Z

Note:BY25Q20BLZIG has not been in mass production, just for engineering samples with no quality assurance.

10.2 Minimum Packing Quantity (MPQ)

Package Type	Packing Type	Qty for 1 Tube or Reel	Vacuum bag/ Inner Box	MPQ
USON8 1.5*1.5*0.45mm	Tape&Reel	5000ea/Reel	1Reel/Bag 10Bags/InnerBox	50,000
USON8 1.5*1.5*0.4mm	Tape&Reel	5000ea/Reel	1Reel/Bag 10Bags/InnerBox	50,000
USON6 1.2*1.2*0.5mm	Tape&Reel	5000ea/Reel	1Reel/Bag 10Bags/InnerBox	50,000
USON6 1.2*1.2*0.4mm	Tape&Reel	5000ea/Reel	1Reel/Bag 10Bags/InnerBox	50,000
USON6 0.85*1.2*0.45mm	Tape&Reel	5000ea/Reel	1Reel/Bag 10Bags/InnerBox	50,000

Note: “USON60.85*1.2*0.45mm” package has not been in mass production, just for engineering samples with no quality assurance.

11. Document Change History

REVISION	CHANGE DESCRIPTION	CLAUSE	ORIGINATOR DATE
1.0	Initiate;	/	Marketing/Designer 2019-01-25
1.1	Modify the description in 8.3 Power-up Timing and Write Inhibit Threshold; Add hardware reset function;	/	Zuohuan Yu 2020-01-03
1.2	Modify the description in 5.5 Status Register;	/	Zuohuan Yu 2020-06-09
1.3	Modify table7 Status Register on page22	/	Zuohuan Yu 2020-12-08
1.4	Update sop8-150mil MPQ	/	Zuohuan Yu 2021-4-7
1.5	Add WSON8 1.5*1.5*0.45mm package	/	Zuohuan Yu 2021-11-12
1.6	Add USON6 1.2*1.2*0.5mm package	/	Zuohuan Yu 2022-5-11
1.7	Add WSON8 1.5*1.5*0.4mm package Add USON6 1.2*1.2*0.4mm package	/	Zuohuan Yu 2022-9-17
1.8	Update top Marking of BY25Q20BLYIG and BY25Q20BLBIG	/	Zuohuan Yu 2022-9-17
1.9	Add WLCSP package	/	Zuohuan Yu 2022-9-19
2.0	1, Update DFN6 1.2*1.2*0.4 MPQ 2, Update ICC3/ICC4	/	Zuohuan Yu 2022-11-25
2.1	Update WLCSP POD	/	Zuohuan Yu 2022-12-07
2.2	Add USON6 0.85*1.2*0.45mm package	/	Zuohuan Yu 2023-03-07
2.3	Update the logo and abbreviation	/	Zuohuan Yu 2023-04-06
2.4	Delete the tCLQV1	/	Zuohuan Yu 2023-04-17
2.5	Modify the USON6 1.2x1.2x0.4mm MPQ	/	Zuohuan Yu 2023-05-05
2.6	Add the note of the DFN package	/	Zuohuan Yu 2023-07-19

2.7	Updata package information and low power information	/	Zuohuan Yu 2024-4-26