DATASHEET

FOR

128M BIT SPI NOR FLASH

BY25Q128FS

Features

- **Serial Peripheral Interface**
  - Standard SPI: SCLK, /CS, SI, SO, /WP, /HOLD
  - Dual SPI: SCLK, /CS, IO0, IO1, /WP, /HOLD
  - Quad SPI: SCLK, /CS, IO0, IO1, IO2, IO3
- **Read**
  - Normal Read (Serial): 100MHz clock rate
  - Fast Read (Serial): 120MHz clock rate with 30PF load
  - Dual I/O data transfer up to 240Mbits/S
  - Quad I/O data transfer up to 480Mbits/S
  - Allows XIP (execute in place) Operation: Continuous Read with 8/16/32/64-byte Wrap
- **Program**
  - Serial-input Page Program up to 256bytes
- **Erase**
  - Block Erase (64/32 KB)
  - Sector Erase (4 KB)
  - Chip Erase
  - Erase Suspend and Resume
- **Program/Erase Speed**
  - Page Program time: 0.7ms typical
  - Sector Erase time: 70ms typical
  - Block Erase time: 0.25/0.4s typical
  - Chip Erase time: 100s typical
- **Flexible Architecture**
  - Sector of 4K-byte
  - Block of 32/64K-byte
- **Low Power Consumption**
  - 10mA maximum active current
  - 2uA maximum power down current
- **Software/Hardware Write Protection**
  - 3x1024-Byte Security Registers with OTP Locks
  - Discoverable Parameters (SFDP) register
  - Enable/Disable protection with WP Pin
  - Write protect all/portion of memory via software
  - Top or Bottom, Sector or Block selection
- **Single Supply Voltage**
  - Full voltage range: 2.7~3.6V
- **Temperature Range**
  - Commercial (-40℃ to +85℃)
  - Industrial (-40℃ to +85℃)
- **Cycling Endurance/Data Retention**
  - Typical 100k Program-Erase cycles on any sector
  - Typical 20-year data retention

Contents

1. Description 5
2. Signal Description 7
2.1 Input/Output Summary 7
2.2 Chip Select (/CS) 7
2.3 Serial Clock (SCLK) 7
2.4 Serial Input (SI)/IO0 7
2.5 Serial Data Output (SO)/IO1 8
2.6 Write Protect (/WP)/IO2 8
2.7 HOLD (/HOLD) /RESET /IO3 8
2.8 VCC Power Supply 8
2.9 VSS Ground 8
3. Block/Sector Addresses 9
4. SPI Operation 10
4.1 Standard SPI Instructions 10
4.2 Dual SPI Instructions 10
4.3 Quad SPI Instructions 10
5. Operation Features 11
5.1 Supply Voltage 11
5.1.1 Operating Supply Voltage 11
5.1.2 Power-up Conditions 11
5.1.3 Device Reset 11
5.1.4 Power-down 11
5.2 Active Power and Standby Power Modes 11
5.3 Hold Condition 11
5.4 Software Reset & Hardware RESET 13
5.4.1 Software Reset 13
5.4.2 Hardware Reset (/HOLD pin) 13
5.5 Write Protect Features 14
5.6 Status Register 15
5.6.1 Status Register Table 15
5.6.2 The Status and Control Bits 16
5.7 Array Memory Protection 18
5.7.1 Block Protect Table 18
6. Device Identification 20
7. Instructions Description 21
7.1 Configuration and Status Instructions 26
7.1.1 Write Enable (06H) 26
7.1.2 Write Enable for Volatile Status Register (50H) 27
7.1.3 Write Disable (04H) 28
7.1.4 Read Status Register (05H or 35H or 15H) 29
7.1.5 Write Status Register (01H or 31H or 11H) 30
7.1.6 Enable Reset (66H) and Reset Device (99H) 31
7.2 Read Instructions 32
7.2.1 Read Data (03H) 32
7.2.2 Fast Read (0BH) 32
7.2.3 Dual Output Fast Read (3BH) 33
7.2.4 Quad Output Fast Read (6BH) 34
7.2.5 Dual I/O Fast Read (BBH) 35
7.2.6 Quad I/O Fast Read (EBH) 37
7.2.7 Quad I/O Word Fast Read (E7H) 39
7.2.8 Set Burst with Wrap (77H) 41
7.3 ID and Security Instructions 42
7.3.1 Read Manufacture ID/ Device ID (90H) 42
7.3.2 Dual I/O Read Manufacture ID/ Device ID (92H) 43
7.3.3 Quad I/O Read Manufacture ID/ Device ID (94H) 44

7.3.4 Read JEDEC ID (9FH) 45
7.3.5 Read Unique ID Number (4Bh) 46
7.3.6 Deep Power-Down (B9H) 47
7.3.7 Release from Deep Power-Down/Read Device ID (ABH) 48
7.3.8 Read Security Registers (48H) 49
7.3.9 Erase Security Registers (44H) 50
7.3.10 Program Security Registers (42H) 51
7.3.11 Read Serial Flash Discoverable Parameter (5AH) 52
7.4 Program and Erase Instructions 57
7.4.1 Page Program (02H) 57
7.4.2 Quad Page Program (32H) 58
7.4.3 Sector Erase (20H) 59
7.4.4 32KB Block Erase (52H) 60
7.4.5 64KB Block Erase (D8H) 61
7.4.6 Chip Erase (60/C7H) 62
7.4.7 Erase Suspend (75H) 63
7.4.8 Erase Resume (7AH) 65
8. Electrical Characteristics 66
8.1 Absolute Maximum Ratings 66
8.2 Operating Ranges 66
8.3 Latch Up Characteristics 67
8.4 Power-up Timing 67
8.5 DC Electrical Characteristics 68
8.6 AC Measurement Conditions 69
8.7 AC Electrical Characteristics 69
9. Package Information 72
9.1 Package 8-Pin SOP 208-mil 72
9.2 Package 8-Pad WSON (5x6mm) 73
10. Order Information 74
10.1 Valid part Numbers and Top Side Marking 75
10.2 Minimum Packing Quantity (MPQ) 75
11. Document Change History 76

1. Description

The BY25Q128FS is 128M-bit Serial Peripheral Interface (SPI) Flash memory, and supports the Dual/Quad SPI: Serial Clock, Chip Select, Serial Data I/O0 (SI), I/O1 (SO), I/O2 (/WP), and I/O3 (/HOLD). The Dual I/O data is transferred with speed of 216Mbits/s and the Quad I/O & Quad output data is transferred with speed of 432Mbits/s. The device uses a single low voltage power supply, ranging from 2.7 Volt to 3.6 Volt.

Additionally, the device supports JEDEC standard manufacturer and device ID and three 1024bytes Security Registers.

In order to meet environmental requirements, BY Technology offers 8-pin SOP 208mil, 8-pad WSON 6x5-mm, and other special order packages, please contacts BY Technology for ordering information.

Figure 1. Logic diagram

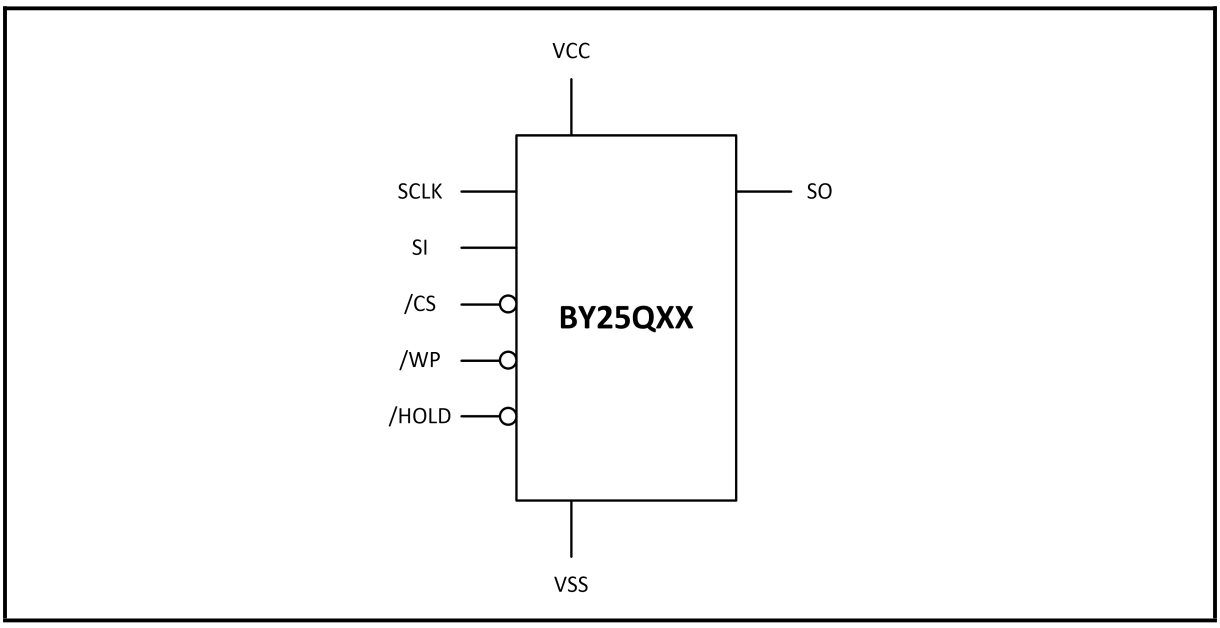


Figure 2. Pin Configuration SOP 208 mil

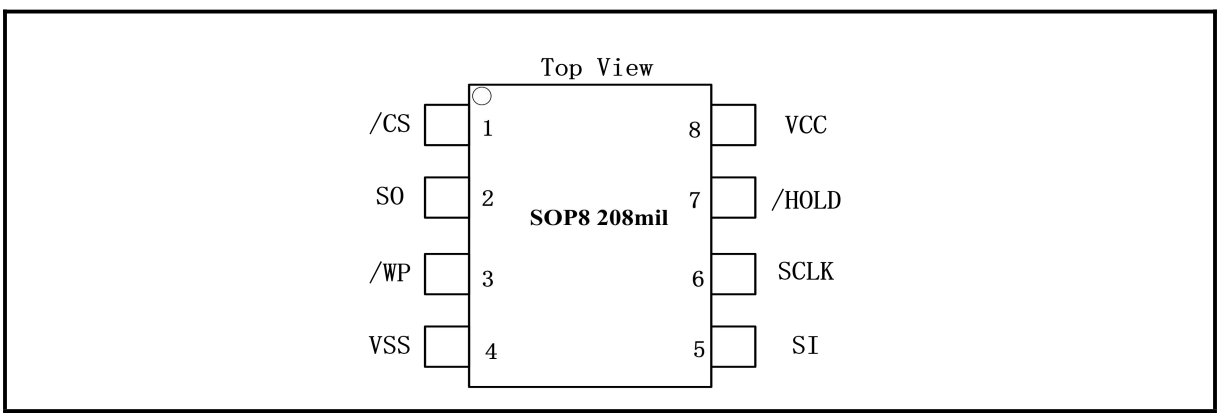
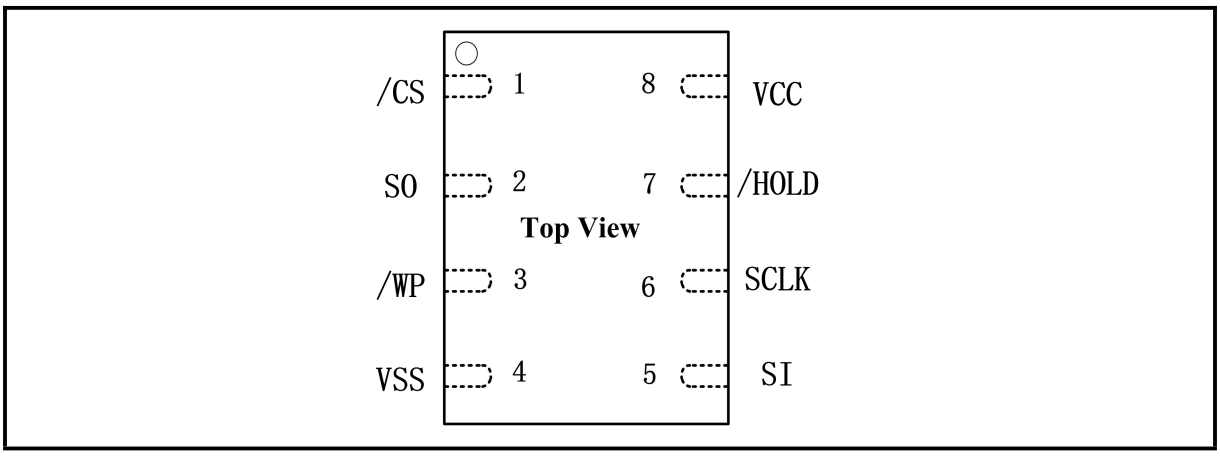


Figure 3. Pin Configuration WSON 5x6-mm



2. Signal Description

During all operations, VCC must be held stable and within the specified valid range: VCC (min) to VCC (max).

All of the input and output signals must be held High or Low (according to voltages of VIH, VOH, VIL or VOL, see ***DC Electrical Characteristics***). These signals are described next.

2.1 Input/Output Summary

Table 1. Signal Names

Pin Name	I/O	Description
/CS	I	Chip Select
SO (IO1)	I/O	Serial Output for single bit data Instructions. IO1 for Dual or Quad Instructions
/WP (IO2)	I/O	Write Protect in single bit or Dual data Instructions. IO2 in Quad mode. The signal has an internal pull-up resistor and may be left unconnected in the host system if not used for Quad Instructions
VSS		Ground
SI (IO0)	I/O	Serial Input for single bit data Instructions. IO0 for Dual or Quad Instructions
SCLK	I	Serial Clock
/HOLD (IO3)	I/O	Hold (pause) serial transfer in single bit or Dual data Instructions. IO3 in Quad-I/O. The signal has an internal pull-up resistor and may be left unconnected in the host system if not used for Quad Instructions
VCC		Core and I/O Power Supply

2.2 Chip Select (/CS)

The chip select signal indicates when an instruction for the device is in process and the other signals are relevant for the memory device. When the /CS signal is at the logic high state, the device is not selected and all input signals are ignored and all output signals are high impedance. Unless an internal Program, Erase or Write Status Registers embedded operation is in progress, the device will be in the Standby Power mode. Driving the /CS input to logic low state enables the device, placing it in the Active Power mode. After Power Up, a falling edge on /CS is required prior to the start of any instruction.

2.3 Serial Clock (SCLK)

This input signal provides the synchronization reference for the SPI interface. Instructions, addresses, or data input are latched on the rising edge of the SCLK signal. Data output changes after the falling edge of SCLK.

2.4 Serial Input (SI)/IO0

This input signal is used to transfer data serially into the device. It receives instructions, addresses, and data to be programmed. Values are latched on the rising edge of serial SCLK clock signal.

SI becomes IO0 an input and output during Dual and Quad Instructions for receiving instructions, addresses, and data to be programmed (values latched on rising edge of serial SCLK clock signal) as well as shifting out data (on the falling edge of SCLK).

2.5 Serial Data Output (SO)/IO1

This output signal is used to transfer data serially out of the device. Data is shifted out on the falling edge of the serial SCLK clock signal.

SO becomes IO1 an input and output during Dual and Quad Instructions for receiving instructions, addresses, and data to be programmed (values latched on rising edge of serial SCLK clock signal) as well as shifting out data (on the falling edge of SCLK).

2.6 Write Protect (/WP)/IO2

When /WP is driven Low (VIL), while the Status Register Protect bits (SRP1 and SRP0) of the Status Registers (SR2[0] and SR1[7]) are set to 0 and 1 respectively, it is not possible to write to the Status Registers. This prevents any alteration of the Status Registers. As a consequence, all the data bytes in the memory area that are protected by the Block Protect, BP4, BP3 bits in the status registers, are also hardware protected against data modification while /WP remains Low. The /WP function is not available when the Quad mode is enabled (QE) in Status Register 2 (SR2[1]=1).

The /WP function is replaced by IO2 for input and output during Quad mode for receiving addresses, and data to be programmed (values are latched on rising edge of the SCLK signal) as well as shifting out data (on the falling edge of SCLK). /WP has an internal pull-up resistance; when unconnected; /WP is at VIH and may be left unconnected in the host system if not used for Quad mode.

2.7 HOLD (/HOLD) /RESET /IO3

The /HOLD function is only available when QE=0, which can be configured either as a /HOLD pin or as a /RESET pin depending on Status Register setting. If QE=1, the /HOLD function is disabled, the pin acts as dedicated data I/O pin, and the /HOLD or /RESET function is not available.

When QE=0 and HOLD/RES= 0, the /HOLD signal goes low to stop any serial communications with the device, but doesn't stop the operation of write status register, programming, or erasing in progress.

The operation of HOLD, need /CS keep low, and starts on falling edge of the /HOLD signal, with SCLK signal being low (if SCLK is not being low, HOLD operation will not start until SCLK being low). The HOLD condition ends on rising edge of /HOLD signal with SCLK being low (If SCLK is not being low, HOLD operation will not end until SCLK being low).

2.8 VCC Power Supply

VCC is the supply voltage. It is the single voltage used for all device functions including read, program, and erase.

2.9 VSS Ground

VSS is the reference for the VCC supply voltage.

3. Block/Sector Addresses

Table 2. Block/Sector Addresses of BY25Q128FS

Memory Density	Big Block (8M bit)	Block (64k byte)	Block (32k byte)	Sector No.	Sector Size(KB)	Address range
128Mbit	Big Block 0	Block 0	Half block 0	Sector 0	4	000000h-000FFFh
				:	:	:
				Sector 7	4	007000h-007FFFh
			Half block 1	Sector 8	4	008000h-008FFFh
				:	4	:
				Sector 15	4	00F000h-00FFFFh
		:	:	:	:	:
		Block 15	Half block 30	Sector 240	4	0F0000h-0F0FFFh
				:	:	:
				Sector 247	4	0F7000h-0F7FFFh
			Half block 31	Sector 248	4	0F8000h-0F8FFFh
				:	:	:
				Sector 255	4	0FF000h-0FFFFFh
		:	:	:	:	:
	Big Block 15	Block 240	Half block 480	Sector 3840	4	F00000h-F00FFFh
				:	:	:
				Sector 3847	4	F07000h-F07FFFh
			Half block 481	Sector 3848	4	F08000h-F08FFFh
				:	:	:
				Sector 3855	4	F0F000h-F0FFFFh
		:	:	:	:	:
		Block 255	Half block 510	Sector 4080	4	FF0000h-FF0FFFh
				:	:	:
				Sector 4087	4	FF7000h-FF7FFFh
			Half block 511	Sector 4088	4	FF8000h-FF8FFFh
				:	:	:
				Sector 4095	4	FFF000h-FFFFFFh

Notes:

1. Big Block = Uniform Big Block, and the size is 8M bits.
2. Block = Uniform Block, and the size is 64K bytes.
3. Half block = Half Uniform Block, and the size is 32k bytes.
4. Sector = Uniform Sector, and the size is 4K bytes.

4. SPI Operation

4.1 Standard SPI Instructions

The BY25Q128FS features a serial peripheral interface on 4 signals bus: Serial Clock (SCLK), Chip Select (/CS), Serial Data Input (SI) and Serial Data Output (SO). Both SPI bus mode 0 and 3 are supported. Input data is latched on the rising edge of SCLK and data shifts out on the falling edge of SCLK.

4.2 Dual SPI Instructions

The BY25Q128FS supports Dual SPI operation when using the “Dual Output Fast Read” (3BH), “Dual I/O Fast Read” (BBH) and “Read Manufacture ID/Device ID Dual I/O” (92H) instructions. These instructions allow data to be transferred to or from the device at two times the rate of the standard SPI. When using the Dual SPI instruction the SI and SO pins become bidirectional I/O pins: IO0 and IO1.

4.3 Quad SPI Instructions

The BY25Q128FS supports Quad SPI operation when using the “Quad Output Fast Read”(6BH), “Quad I/O Fast Read” (EBH) ,”Quad I/O word Fast Read”(E7H),”Read Manufacture ID/Device ID Quad I/O”(94H) and “Quad Page Program”(32H) instructions. These instructions allow data to be transferred to or from the device at four times the rate of the standard SPI. When using the Quad SPI instruction the SI and SO pins become bidirectional I/O pins: IO0 and IO1, and /WP and /HOLD pins become IO2 and IO3. Quad SPI instructions require the non-volatile Quad Enable bit (QE) in Status Register to be set.

5. Operation Features

5.1 Supply Voltage

5.1.1 Operating Supply Voltage

Prior to selecting the memory and issuing instructions to it, a valid and stable VCC voltage within the specified [VCC(min), VCC(max)] range must be applied (see ***Electrical Characteristics***). In order to secure a stable DC supply voltage, it is recommended to decouple the VCC line with a suitable capacitor (usually of the order of 10*nF* to 100*nF*) close to the VCC/VSS package pins. This voltage must remain stable and valid until the end of the transmission of the instruction and, for a Write instruction, until the completion of the internal write cycle (tW).

5.1.2 Power-up Conditions

When the power supply is turned on, VCC rises continuously from VSS to VCC. During this time, the Chip Select (/CS) line is not allowed to float but should follow the VCC voltage, it is therefore recommended to connect the /CS line to VCC via a suitable pull-up resistor.

In addition, the Chip Select (/CS) input offers a built-in safety feature, as the /CS input is edge sensitive as well as level sensitive: after power-up, the device does not become selected until a falling edge has first been detected on Chip Select (/CS). This ensures that Chip Select (/CS) must have been High, prior to going Low to start the first operation.

5.1.3 Device Reset

In order to prevent inadvertent Write operations during power-up (continuous rise of VCC), a power on reset (POR) circuit is included. At Power-up, the device does not respond to any instruction until VCC has reached the power on reset threshold voltage (this threshold is lower than the minimum VCC operating voltage defined in ***Power-up Timing***).

When VCC is lower than V_{WI}, the device is reset.

5.1.4 Power-down

At Power-down (continuous decrease in VCC), as soon as VCC drops from the normal operating voltage to below the power on reset threshold voltage(V_{WI}), the device stops responding to any instruction sent to it. During Power-down, the device must be deselected (Chip Select (/CS) should be allowed to follow the voltage applied on VCC) and in Standby Power mode (that is there should be no internal Write cycle in progress).

5.2 Active Power and Standby Power Modes

When Chip Select (/CS) is Low, the device is selected, and in the Active Power mode. The device consumes ICC.

When Chip Select (/CS) is High, the device is deselected. If a Write cycle is not currently in progress, the device then goes in to the Standby Power mode, and the device consumption drops to ICC1.

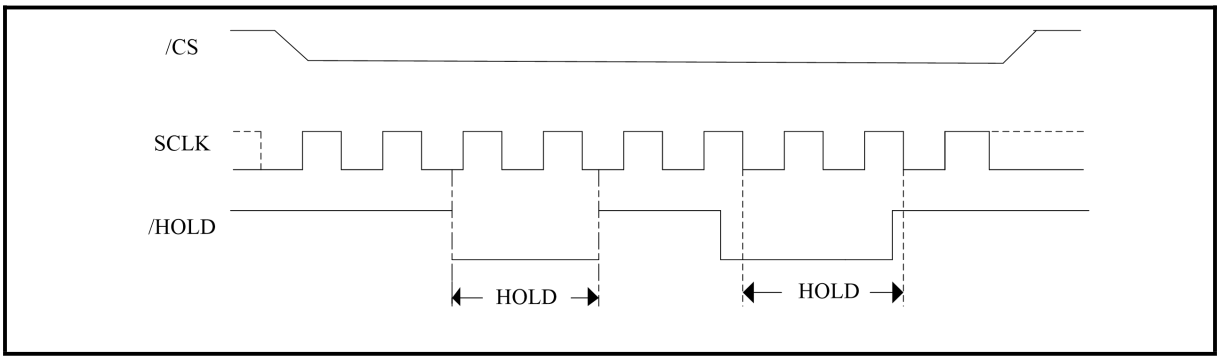
5.3 Hold Condition

When QE=0, HOLD/RST=0, the Hold (/HOLD) signal is used to pause any serial communications with the device without resetting the clocking sequence. During the Hold condition, the Serial Data Output (SO) is high impedance, and Serial Data Input (SI) and Serial Clock (SCLK) are Don't Care. To enter the Hold condition, the device must be selected, with Chip Select (/CS) Low. Normally, the device is kept selected, for the whole duration of the Hold condition. Deselecting the device while it

is in the Hold condition, has the effect of resetting the state of the device, and this mechanism can be used if it is required to reset any processes that had been in progress.

The Hold condition starts when the Hold (/HOLD) signal is driven Low at the same time as Serial Clock (SCLK) already being Low (as shown in ***Figure 4***).The Hold condition ends when the Hold (HOLD) signal is driven High at the same time as Serial Clock (C) already being Low. ***Figure 4*** also shows what happens if the rising and falling edges are not timed to coincide with Serial Clock (SCLK) being Low.

Figure 4. Hold condition activation



5.4 Software Reset & Hardware RESET

5.4.1 Software Reset

The BY25Q128FS can be reset to the initial power-on state by a software reset sequence. This sequence must include two consecutive instructions: Enable Reset (66h) & Reset (99h). If the instruction sequence is successfully accepted, the device will take approximately 300uS (tRST) to reset. No instruction will be accepted during the reset period.

5.4.2 Hardware Reset (/HOLD pin)

The BY25Q128FS can also be configured to utilize hardware /RESET pin. The HOLD/RST bit in the Status Register-3 is the configuration bit for /HOLD pin function or /RESET pin function. When HOLD/RST=0 (factory default), the pin acts as a /HOLD pin as described above; when HOLD/RST=1, the pin acts as a /RESET pin. Drive the /RESET pin low for a minimum period of ~1us (tRESET(1)) will reset the device to its initial power-on state. Any on-going Program/Erase operation will be interrupted and data corruption may happen. While /RESET is low, the device will not accept any instruction input.

If QE bit is set to 1, the /HOLD or /RESET function will be disabled, the pin will become one of the four data I/O pin.

Hardware /RESET pin has the highest priority among all the input signals. Drive /RESET low for a minimum period of ~1us (tRESET(1)) will interrupt any on-going external/internal operations, regardless the status of other SPI signals (/CS, CLK, IOs, /WP and /HOLD).

Notes:

1. While a faster /RESET pulse (as short as a few hundred nanoseconds) will often reset the device, a 1us minimum pulse is recommended to ensure reliable operation.

5.5 Write Protect Features

1. Software Protection (Memory array):

   - The Block Protect (BP4, BP3, BP2, BP1, BP0) bits define the section of the memory array that can be read but not change.

2. Hardware Protection (Status register): /WP going low to protected the writable bits of Status Register.

3. Deep Power-Down: In Deep Power-Down Mode, all instructions are ignored except the Release from deep Power-Down Mode instruction.

4. Device resets when VCC is below threshold: Upon power-up or at power-down, the BY25Q128FS will maintain a reset condition while VCC is below the threshold value of V_{WI}. While reset, all operations are disabled and no instructions are recognized.

5. Time delay write disable after Power-up: During power-up and after the VCC voltage exceeds $VCC_{(min)}$, all program and erase related instructions are further disabled for a time delay of tVSL. This includes the Write Enable, Page Program, Sector Erase, Block Erase, Chip Erase and the Write Status Register instructions.

6. Write Enable: The Write Enable instruction is set the Write Enable Latch bit. The WEL bit will return to reset by following situation:

   -Power –up
   -Write Disable
   -Write Status Register (Whether the SR is protected, WEL will return to reset)
   -Page Program (Whether the program area is protected, WEL will return to reset)
   -Sector Erase/Block Erase/Chip Erase (Whether the erase area is protected, WEL will return to reset)
   -Software Reset
   -Hardware Reset

7. One Time Program (OTP) write protection for array and Security Registers using Status Register.

5.6 Status Register

5.6.1 Status Register Table

See ***Table 3*** for detail description of the Status Register bits.

Table 3. Status Register

	SR3							
	S23	**S22**	**S21**	**S20**	**S19**	**S18**	**S17**	**S16**
	HOLD/RST	**DRV1**	**DRV0**	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**Reserved**
Default (1)	0	1	0	×	×	×	×	×

	SR2							
	S15	**S14**	**S13**	**S12**	**S11**	**S10**	**S9**	**S8**
	SUS	**CMP**	**LB3**	**LB2**	**LB1**	**Reserved**	**QE**	**SRP1**
Default (1)	0	0	0	0	0	0	0	0
	Read Only		OTP	OTP	OTP	Read Only		

	SR1							
	S7	**S6**	**S5**	**S4**	**S3**	**S2**	**S1**	**S0**
	SRP0	**BP4**	**BP3**	**BP2**	**BP1**	**BP0**	**WEL**	**WIP**
Default (1)	0	0	0	0	0	0	0	0
							Read Only	Read Only

Notes:

1. The default value is set by Manufacturer during wafer sort, Marked as Default in following text

5.6.2 The Status and Control Bits

5.6.2.1 WIP bit

The Write in Progress (WIP) bit indicates whether the memory is busy in program/erase/write status register progress. When WIP bit sets to 1, means the device is busy in program/erase/write status register progress, when WIP bit sets 0, means the device is not in program/erase/write status register progress.

5.6.2.2 WEL bit

The Write Enable Latch (WEL) bit indicates the status of the internal Write Enable Latch. When set to 1 the internal Write Enable Latch is set, when set to 0 the internal Write Enable Latch is reset and no Write Status Register, Program or Erase, etc. instruction is accepted.

5.6.2.3 BP4, BP3, BP2, BP1, BP0 bits

The Block Protect (BP4, BP3, BP2, BP1, BP0) bits are non-volatile. They define the size of the area to be software protected against Program and Erase instructions. These bits are written with the Write Status Register instruction. When WPS=0, and the Block Protect (BP4, BP3, BP2, BP1, BP0) bits are set to 1, the relevant memory area (as defined in ***Table 6-Table 7***).becomes protected against Page Program, Sector Erase and Block Erase instructions. The Block Protect (BP4, BP3, BP2, BP1, BP0) bits can be written provided that the Hardware Protected mode has not been set. The Chip Erase instruction is executed, if the Block Protect (BP2, BP1, BP0) bits are 0 and CMP=0 or The Block Protect (BP2, BP1, BP0) bits are 1 and CMP=1.

5.6.2.4 SRP1, SRP0 bits

The Status Register Protect (SRP1 and SRP0) bits are non-volatile Read/Write bits in the status register. The SRP bits control the method of write protection: software protection, hardware protection, power supply lock-down or one time programmable protection.

Table 4. Status Register protect table

SRP1	SRP0	/WP	Status Register	Description
0	0	X	Software Protected	The Status Register can be written to after a Write Enable instruction, WEL=1.(Factory Default)
0	1	0	Hardware Protected	/WP=0, the Status Register locked and cannot be written.
0	1	1	Hardware Unprotected	/WP=1, the Status Register is unlocked and can be written to after a Write Enable instruction, WEL=1.
1	0	X	Power Supply Lock-Down(1)	Status Register is protected and cannot be written to again until the next Power-Down, Power-Up cycle.
1	1	X	One Time Program(2)	Status Register is permanently protected and cannot be written to.

Notes:

1. When SRP1, SRP0= (1, 0), a Power-Down, Power-Up cycle will change SRP1, SRP0 to (0, 0) state.
2. The One time Program feature is available upon special order. Please contact BY Technology for details.

5.6.2.5 QE bit

The Quad Enable (QE) bit is a non-volatile Read/Write bit in the Status Register that allows Quad operation. When the QE bit is set to 0 (Default) the /WP pin and /HOLD pin are enable. When the QE pin is set to 1, the Quad IO2 and IO3 pins are enabled. (The QE bit should never be set to 1 during standard SPI or Dual SPI operation if the /WP or /HOLD pins directly to the power supply or ground).

5.6.2.6 LB3/LB2/LB1 bits

The Security Register Lock (LB3/LB2/LB1) bits are non-volatile One Time Program (OTP) bits in Status Register (S13–S11) that provide the write protect control and status to the Security Registers. The default state of LB is 0, the security registers are unlocked. LB can be set to 1 individually using the Write Register instruction. LB is One Time Programmable, once they are set to 1, the Security Registers will become read-only permanently.

5.6.2.7 CMP bit

The Complement Protect (CMP) bit is a non-volatile Read/Write bit in the Status Register (S14). It is used in conjunction the BP4-BP0 bits to provide more flexibility for the array protection. Please see the Status registers Memory Protection table for details. The default setting is CMP=0.

5.6.2.8 SUS bit

The Suspend Status (SUS) bit is read only bits in the status register2 (S15) that are set to 1 after executing an Erase Suspend (75H) instruction. The SUS bit is cleared to 0 by Erase Resume (7AH) instruction as well as a power-down, power-up cycle.

5.6.2.9 HOLD/RST bit

The /HOLD or /RESET Pin Function (HOLD/RST) bit is used to determine whether /HOLD or /RESET function should be implemented on the hardware pin. When HOLD/RST=0 (factory default), the pin acts as /HOLD; when HOLD/RST=1, the pin acts as /RESET. However, /HOLD or /RESET functions are only available when QE=0. If QE is set to 1, the /HOLD and /RESET functions are disabled, the pin acts as a dedicated data I/O pin.

5.6.2.10 DRV1/DRV0 bits

The Output Driver Strength (DRV1&DRV0) bits are used to determine the output driver strength for the Read instruction.

Table 5. The Output Driver Strength

DRV1,DRV0	Driver Strength
00	25%
01	50%
10	75% (default)
11	100%

5.7 Array Memory Protection

5.7.1 Block Protect Table

Table 6. BY25Q128FS Block Memory Protection (CMP=0)

Status Register Content					Memory Content			
BP4	BP3	BP2	BP1	BP0	Blocks	Addresses	Density	Portion
X	X	0	0	0	NONE	NONE	NONE	NONE
0	0	0	0	1	252 to 255	FC0000H-FFFFFFH	256KB	Upper 1/64
0	0	0	1	0	248 to 255	F80000H-FFFFFFH	512KB	Upper 1/32
0	0	0	1	1	240 to 255	F00000H-FFFFFFH	1MB	Upper 1/16
0	0	1	0	0	224 to 255	E00000H-FFFFFFH	2MB	Upper 1/8
0	0	1	0	1	192 to 255	C00000H-FFFFFFH	4MB	Upper 1/4
0	0	1	1	0	128 to 255	800000H-FFFFFFH	8MB	Upper 1/2
0	1	0	0	1	0 to 3	000000H-03FFFFH	256KB	Lower 1/64
0	1	0	1	0	0 to 7	000000H-07FFFFH	512KB	Lower 1/32
0	1	0	1	1	0 to 15	000000H-0FFFFFH	1MB	Lower 1/16
0	1	1	0	0	0 to 31	000000H-1FFFFFH	2MB	Lower 1/8
0	1	1	0	1	0 to 63	000000H-3FFFFFH	4MB	Lower 1/4
0	1	1	1	0	0 to 127	000000H-7FFFFFH	8MB	Lower 1/2
X	X	1	1	1	0 to 255	000000H-FFFFFFH	16MB	ALL
1	0	0	0	1	255	FFF000H-FFFFFFH	4KB	Top Block
1	0	0	1	0	255	FFE000H-FFFFFFH	8KB	Top Block
1	0	0	1	1	255	FFC000H-FFFFFFH	16KB	Top Block
1	0	1	0	X	255	FF8000H-FFFFFFH	32KB	Top Block
1	0	1	1	0	255	FF8000H-FFFFFFH	32KB	Top Block
1	1	0	0	1	0	000000H-000FFFH	4KB	Bottom Block
1	1	0	1	0	0	000000H-001FFFH	8KB	Bottom Block
1	1	0	1	1	0	000000H-003FFFH	16KB	Bottom Block
1	1	1	0	X	0	000000H-007FFFH	32KB	Bottom Block
1	1	1	1	0	0	000000H-007FFFH	32KB	Bottom Block

Table 7. BY25Q128FS Block Memory Protection (CMP=1)

Status Register Content					Memory Content			
BP4	BP3	BP2	BP1	BP0	Blocks	Addresses	Density	Portion
X	X	0	0	0	0 to 255	000000H-FFFFFFH	ALL	ALL
0	0	0	0	1	0 to 251	000000H-FBFFFFH	16128KB	Lower 63/64
0	0	0	1	0	0 to 247	000000H-F7FFFFH	15872KB	Lower 31/32
0	0	0	1	1	0 to 239	000000H-EFFFFFH	15KB	Lower 15/16
0	0	1	0	0	0 to 223	000000H-DFFFFFH	14MB	Lower 7/8
0	0	1	0	1	0 to 191	000000H-BFFFFFH	12MB	Lower 3/4
0	0	1	1	0	0 to 127	000000H-7FFFFFH	8MB	Lower 1/2
0	1	0	0	1	4 to 255	040000H-FFFFFFH	16128KB	Upper 63/64
0	1	0	1	0	8 to 255	080000H-FFFFFFH	15872KB	Upper 31/32
0	1	0	1	1	16 to 255	100000H-FFFFFFH	15KB	Upper 15/16
0	1	1	0	0	32 to 255	200000H-FFFFFFH	14MB	Upper 7/8
0	1	1	0	1	64 to 255	400000H-FFFFFFH	12MB	Upper 3/4
0	1	1	1	0	128 to 255	800000H-FFFFFFH	8MB	Upper 1/2
X	X	1	1	1	NONE	NONE	NONE	NONE
1	0	0	0	1	0 to 255	000000H-FFEFFFH	16380KB	L-4095/4096
1	0	0	1	0	0 to 255	000000H-FFDFFFH	16376KB	L-2047/2048
1	0	0	1	1	0 to 255	000000H-FFBFFFH	16368KB	L-1023/1024
1	0	1	0	X	0 to 255	000000H-FF7FFFH	16352KB	L-511/512
1	0	1	1	0	0 to 255	000000H-FF7FFFH	16352KB	L-511/512
1	1	0	0	1	0 to 255	001000H-FFFFFFH	16380KB	U-4095/4096
1	1	0	1	0	0 to 255	002000H-FFFFFFH	16376KB	U-2047/2048
1	1	0	1	1	0 to 255	004000H-FFFFFFH	16368KB	U-1023/1024
1	1	1	0	X	0 to 255	008000H-FFFFFFH	16352KB	U-511/512
1	1	1	1	0	0 to 255	008000H-FFFFFFH	16352KB	U-511/512

6. Device Identification

Three legacy Instructions are supported to access device identification that can indicate the manufacturer, device type, and capacity (density). The returned data bytes provide the information as shown in the below table.

Table 8. BY25Q128FS ID Definition table

Operation Code	M7-M0	ID15-ID8	ID7-ID0
9FH	68	41	18
90H/92H/94H	68		17
ABH			17

7. Instructions Description

All instructions, addresses and data are shifted in and out of the device, beginning with the most significant bit on the first rising edge of SCLK after /CS is driven low. Then, the one byte instruction code must be shifted in to the device, most significant bit first on SI, each bit being latched on the rising edges of SCLK.

See ***Table 9***, every instruction sequence starts with a one-byte instruction code. Depending on the instruction, this might be followed by address bytes, or by data bytes, or by both or none. /CS must be driven high after the last bit of the instruction sequence has been shifted in. For the instruction of Read, Fast Read, Read Status Register or Release from Deep Power Down, and Read Device ID, the shifted-in instruction sequence is followed by a data out sequence. /CS can be driven high after any bit of the data-out sequence is being shifted out.

For the instruction of Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register, Write Enable, Write Disable or Deep Power-Down instruction, etc. /CS must be driven high exactly at a byte boundary, otherwise the instruction is rejected, and is not executed. That is /CS must drive high when the number of clock pulses after /CS being driven low is an exact multiple of eight. For Page Program, if at any time the input byte is not a full byte, nothing will happen and WEL will not be reset.

Table 9. Instruction Set Table

Instruction Name	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	N-Bytes
Configuration and Status Instructions							
Write Enable	06H						
Write Enable for Volatile Status Register	50H						
Write Disable	04H						
Read Status Register-1	05H	(S7-S0)					continuous
Read Status Register-2	35H	(S15-S8)					continuous
Read Status Register-3	15H	(S23-S16)					continuous
Write Status Register -1	01H	(S7-S0)					
Write Status Register-2	31H	(S15-S8)					
Write Status Register-3	11H	(S23-S16)					
Enable Reset	66H						
Reset	99H						
Read Instructions							
Read Data	03H	A23-A16	A15-A8	A7-A0	(D7-D0)	Next byte	continuous
Fast Read	0BH	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)	continuous
Dual Output Fast Read	3BH	A23-A16	A15-A8	A7-A0	dummy	(D7-D0) (1)	continuous
Dual I/O Fast Read	BBH	A23-A8(2)	A7-A0 M7-M0(2)	(D7-D0)(1)	Next byte	Next byte	continuous
Quad Output Fast Read	6BH	A23-A16	A15-A8	A7-A0	dummy	(D7-D0) (3)	continuous
Quad I/O Fast Read	EBH	A23-A0 M7-M0(4)	dummy(5)	(D7-D0)(3)	Next byte	Next byte	continuous
Quad I/O Word Fast Read(7)	E7H	A23-A0 dM7-M0 (4)	dummy(6)	(D7-D0)(3)	Next byte	Next byte	continuous
Set Burst with Wrap	77H	dummy(9) W7-W0					
ID and Security Instructions							
Manufacturer/ Device ID	90H	dummy	dummy	00H	(MID7-MID0)	(ID7-ID0)	continuous
Manufacturer/ Device ID by Dual I/O	92H	A23-A8	A7-A0, dummy	(MID7-MID0) ,(DID7-DID0)			continuous
Manufacturer/ Device ID by Quad I/O	94H	A23-A0, dummy	dummy(8) (MID7-MID0) (DID7-DID0)				continuous
JEDEC ID	9FH	MID7-MID 0	ID15-ID8	ID7-ID0			continuous
Read Unique ID Number	4Bh	Dummy	Dummy	Dummy	Dummy	(ID127-I D0)	
Deep Power-Down	B9H						
Release From Deep Power-Down, And Read Device ID	ABH	dummy	dummy	dummy	(ID7-ID0)		continuous

Release From Deep Power-Down	ABH						
Read Security Registers(10)	48H	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)	continuous
Program Security Registers(10)	42H	A23-A16	A15-A8	A7-A0	(D7-D0)	(D7-D0)	continuous
Erase Security Registers(10)	44H	A23-A16	A15-A8	A7-A0			
Read Serial Flash Discoverable Parameter	5AH	A23-A16	A15-A8	A7-A0	Dummy	D7-D0	continuous
Program and Erase Instructions							
Page Program	02H	A23-A16	A15-A8	A7-A0	(D7-D0)	Next byte	continuous
Quad Page Program	32H	A23-A16	A15-A8	A7-A0	(D7-D0)(3)	Next byte	continuous
Sector Erase	20H	A23-A16	A15-A8	A7-A0			
32K Block Erase	52H	A23-A16	A15-A8	A7-A0			
64K Block Erase	D8H	A23-A16	A15-A8	A7-A0			
Chip Erase	C7/60H						
Erase Suspend	75H						
Erase Resume	7AH						

Notes:

1. Dual Output data
   IO0 = (D6, D4, D2, D0)
   IO1 = (D7, D5, D3, D1)
2. Dual Input Address
   IO0 = A22, A20, A18, A16, A14, A12, A10, A8, A6, A4, A2, A0, M6, M4, M2, M0
   IO1 = A23, A21, A19, A17, A15, A13, A11, A9, A7, A5, A3, A1, M7, M5, M3,M1
3. Quad Output Data
   IO0 = (D4, D0,…..)
   IO1 = (D5, D1,…..)
   IO2 = (D6, D2,…..)
   IO3 = (D7, D3,…..)
4. Quad Input Address
   IO0 = A20, A16, A12, A8, A4, A0, M4, M0
   IO1 = A21, A17, A13, A9, A5, A1, M5, M1
   IO2 = A22, A18, A14, A10, A6, A2, M6, M2
   IO3 = A23, A19, A15, A11, A7, A3, M7, M3
5. Fast Read Quad I/O Data
   IO0 = (x, x, x, x, D4, D0,…)
   IO1 = (x, x, x, x, D5, D1,…)
   IO2 = (x, x, x, x, D6, D2,…)
   IO3 = (x, x, x, x, D7, D3,…)
6. Fast Word Read Quad I/O Data
   IO0 = (x, x, D4, D0,…)
   IO1 = (x, x , D5, D1,…)
   IO2 = (x, x, D6, D2,…)
   IO3 = (x, x, D7, D3,…)
7. Fast Word Read Quad I/O Data: the lowest address bit must be 0.
8. Address, continuous Read Mode bits, Dummy bits, Manufacture ID and Device ID
   IO0 = (A20, A16, A12, A8, A4, A0, M4, M0, x, x, x, x, MID4, MID0, DID4, DID0)
   IO1 = (A21, A17, A13, A9, A5, A1, M5, M1, x, x, x, x, MID5, MID1, DID5, DID1)
   IO2 = (A22, A18, A14, A10, A6, A2, M6, M2, x, x, x, x, MID6, MID2, DID6, DID2)
   IO3 = (A23, A19, A15, A11, A7, A3, M7, M3, x, x, x, x, MID7, MID3, DID7, DID3)

9. Dummy bits and Wraps Bits
   IO0 = (x, x, x, x, x, x, w4, x)
   IO1 = (x, x, x, x, x, x, w5, x)
   IO2 = (x, x, x, x, x, x, w6, x)
   IO3 = (x, x, x, x, x, x, x,x)

10. Security Registers Address:
    Security Register1: A23-A16=00H, A15-A10=000100b, A9-A0= Byte Address;
    Security Register2: A23-A16=00H, A15-A10=001000b, A9-A0= Byte Address;
    Security Register3: A23-A16=00H, A15-A10=001100b, A9-A0= Byte Address;

Security Register 0 can be used to store the Flash Discoverable Parameters,
The feature is upon special order, please contact BY Technology for details.

Table 10. Instructions that need to send the Write Enable/Write Enable for Volatile Status Register instruction

Instruction		Write
Write Status Register	01h/31h/11h	06H/50H
Erase Security Registers	44h	06H
Program Security Registers	42h	06H
Page Program	02h	06H
Quad Page Program	32h	06H
Sector Erase	20h	06H
32KB Block Erase	52h	06H
64KB Block Erase	D8h	06H
Chip Erase	60h/C7h	06H

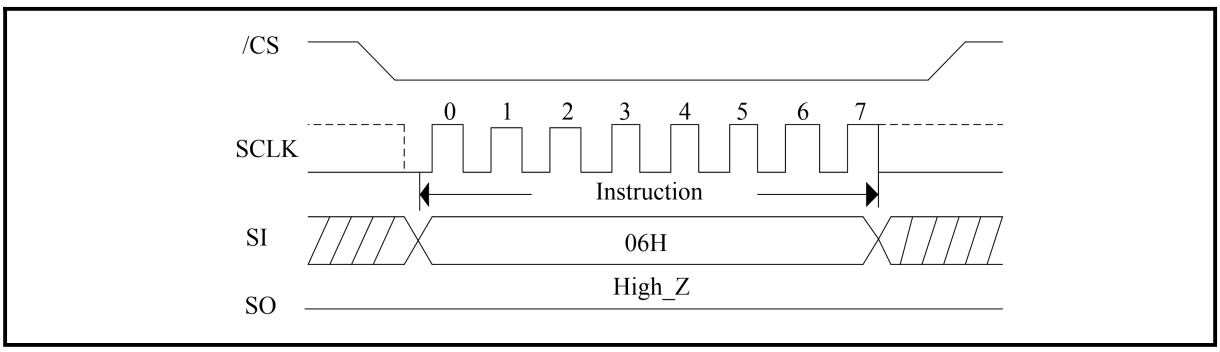
7.1 Configuration and Status Instructions

7.1.1 Write Enable (06H)

See ***Figure 5***, the Write Enable instruction is for setting the Write Enable Latch bit. The Write Enable Latch bit must be set prior to every Write Status Register, Program and Erase. The Write Enable instruction sequence: /CS goes low sending the Write Enable instruction, /CS goes high.

Please note that the Write Enable instruction sent when the Write Enable for Volatile Status Register instruction is valid is not accepted. Therefore, when need to send the Write Enable instruction, but do not know if the Write Enable for Volatile Status Register instruction is valid, please send the Write Disable instruction first.

Figure 5. Write Enable Sequence Diagram

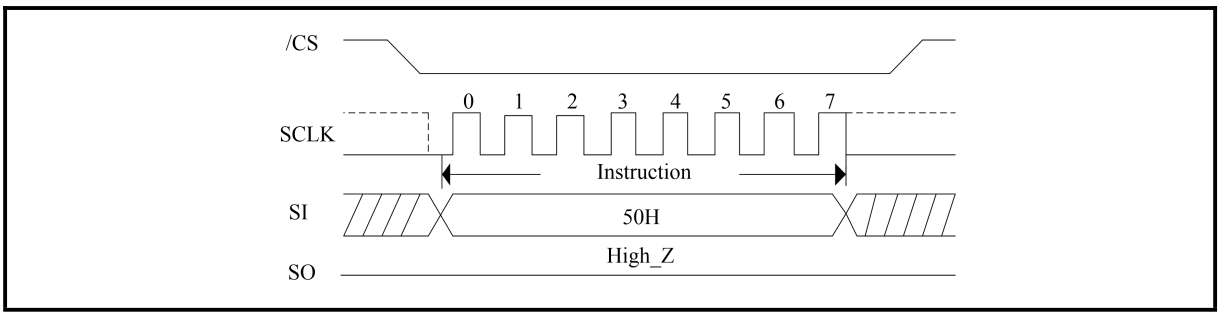


7.1.2 Write Enable for Volatile Status Register (50H)

See ***Figure 6***, the non-volatile Status Register bits can also be written to as volatile bits (HOLD/RST, DRV1, DRV0, CMP, QE, SRP1, SRP0, BP4, BP3, BP2, BP1, BP0). This gives more flexibility to change the system configuration and memory protection schemes quickly without waiting for the typical non-volatile bit write cycles or affecting the endurance of the Status Register non-volatile bits. Write Enable for Volatile Status Register instruction will not set the Write Enable Latch bit, it is only valid for the Write Status Registers instruction to change the volatile Status Register bit values (After the software reset or re-powered, the volatile Status Register bit values will be restored to the default value or the value input by the Write Enable instruction).

Please note that the Write Enable for Volatile Status Register instruction sent when the Write Enable instruction is valid is not accepted. Therefore, when need to send the Write Enable for Volatile Status Register instruction, please first determine whether the Write Enable instruction is not valid.

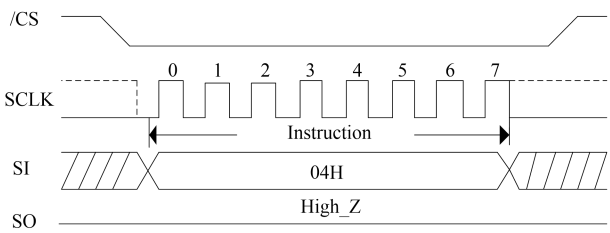
Figure 6. Write Enable for Volatile Status Register



7.1.3 Write Disable (04H)

See ***Figure 7***, the Write Disable instruction is for resetting the Write Enable Latch bit or invalidate the Write Enable for Volatile Status Register instruction. The Write Disable instruction sequence: /CS goes low -> sending the Write Disable instruction -> /CS goes high. The WEL bit is reset by following condition: Power-up and upon completion of the Write Status Register, Page Program, Sector Erase, Block Erase and Chip Erase, Program/Erase Security Registers and Reset instructions.

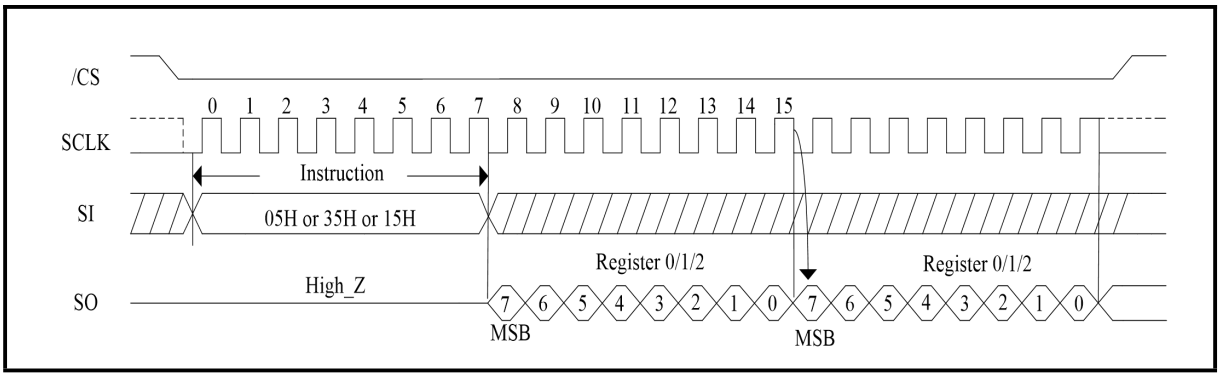
Figure 7. Write Disable Sequence Diagram



7.1.4 Read Status Register (05H or 35H or 15H)

See ***Figure 8***, the Read Status Register (RDSR) instruction is for reading the Status Register. The Status Register may be read at any time, even while a Program, Erase or Write Status Register cycle is in progress. When one of these cycles is in progress, it is recommended to check the Write in Progress (WIP) bit before sending a new instruction to the device. It is also possible to read the Status Register continuously. For instruction code “05H”, the SO will output Status Register bits S7~S0. The instruction code “35H”, the SO will output Status Register bits S15~S8, The instruction code “15H”, the SO will output Status Register bits S23~16.

Figure 8. Read Status Register Sequence Diagram



7.1.5 Write Status Register (01H or 31H or 11H)

The Write Status Register instruction allows the Status Registers to be written. The Status Register-1 can be written by the Write Status Register 01h instruction; The Status Register-2 be written by the Write Status Register 01h or 31h instruction; Status Register-3 can be written by the Write Status Register 11h instruction. When the Write Status Register instruction 01h is followed by 1 byte data, the data will be written to Status Register-1. When the Write Status Register instruction 01h is followed by 2 bytes of data, the first byte data will be written to Status Register-1, and the second byte data will be written to Status Register-2; And Write Status Register instruction 31h or 11h can only follow 1 byte data, the data will be written to Status Register-2、Status Register-3 respectively. The writable Status Register bits include: SRP0, BP[4:0] in Status Register-1; CMP, LB[3:1], QE, SRP1 in Status Register- 2; DRV1, DRV0 in Status Register- 3. All other Status Register bit locations are read-only and will not be affected by the Write Status Register instruction. LB[3:1] are non-volatile OTP bits, once it is set to 1, it cannot be cleared to 0.

The Write Status Register instruction allows new values to be written to the Status Register. Before it can be accepted, a Write Enable or Write Enable For Volatile SR instruction must previously have been executed After the Write Enable instruction has been decoded and executed, the device sets the Write Enable Latch (WEL).

The Write Status Register instruction has no effect on S15 (SUS), S1 (WEL) and S0 (WIP) of the Status Register. /CS must be driven high after the 8 or 16 bit of the data byte has been latched in. If not, the Write Status Register (WRSR) instruction is not executed. As soon as /CS is driven high, the self-timed Write Status Register cycle (whose duration is tW) is initiated. While the Write Status Register cycle is in progress, the Status Register may still be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Write Status Register cycle, and is 0 when it is completed. When the cycle is completed, the Write Enable Latch (WEL) is reset.

The Write Status Register instruction allows the user to change the values of the Block Protect (BP4, BP3, BP2, BP1, and BP0) bits, to define the size of the area that is to be treated as read-only, as defined in ***Table 6*** and ***Table 7***. The Write Status Register (WRSR) instruction also allows the user to set or reset the Status Register Protect (SRP1 and SRP0) bits in accordance with the Write Protect (/WP) signal. The Status Register Protect (SRP1 and SRP0) bits and Write Protect (/WP) signal allow the device to be put in the Hardware Protected Mode. The Write Status Register instruction is not executed once the Hardware Protected Mode is entered.

The sequence of issuing WRSR instruction is: /CS goes low→ sending WRSR instruction code→ Status Register data on SI→/CS goes high.

The /CS must go high exactly at the 8 bits or 16 bits data boundary; otherwise, the instruction will be rejected and not executed. The self-timed Write Status Register cycle time (tW) is initiated as soon as Chip Select (/CS) goes high. The Write in Progress (WIP) bit still can be checked during the Write Status Register cycle is in progress. The WIP is set 1 during the tW timing, and is set 0 when Write Status Register Cycle is completed, and the Write Enable Latch (WEL) bit is reset.

Figure 9. Write Status Register Sequence Diagram-01H 2byte

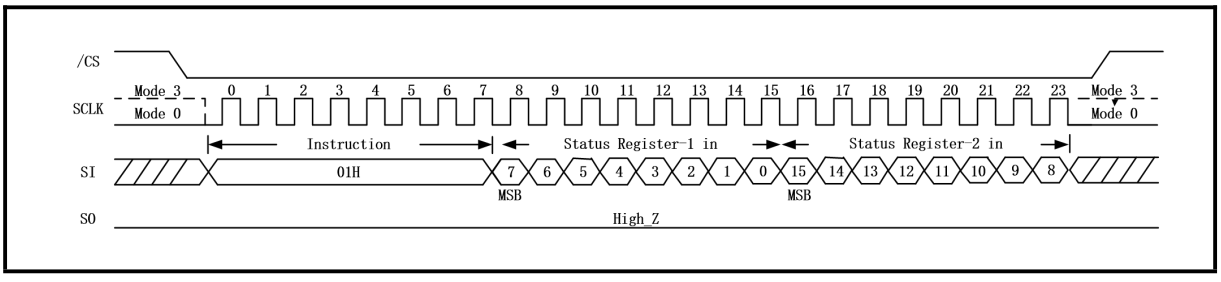
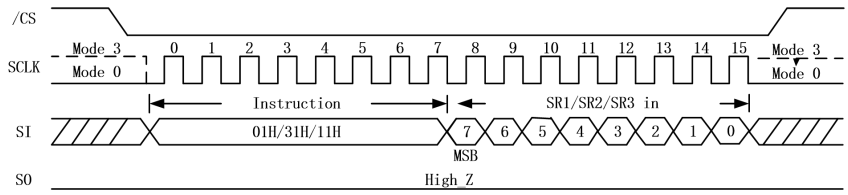


Figure 10. Write Status Register Sequence Diagram-01/31/11H 1byte



7.1.6 Enable Reset (66H) and Reset Device (99H)

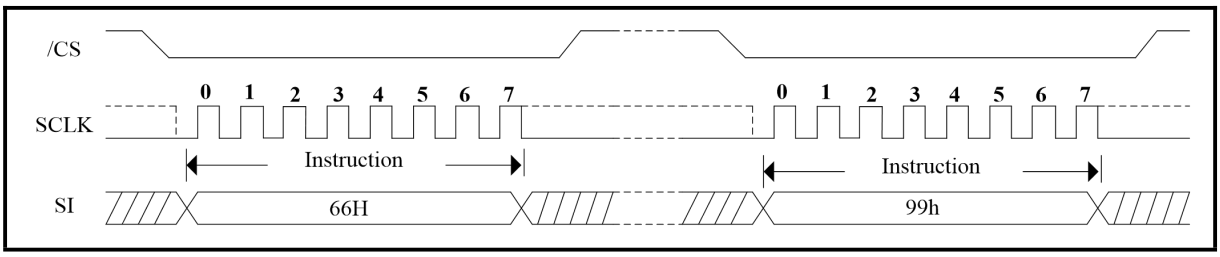
Because of the small package and the limitation on the number of pins, the BY25Q128FS provides a software reset instruction instead of a dedicated RESET pin. Once the software reset instruction is accepted, any on-going internal operations will be terminated and the device will return to its default power-on state and lose all the current volatile settings, such as Volatile Status Register bits, Write Enable Latch (WEL) status, Program/Erase Suspend status, Continuous Read Mode bit setting (M7-M0) and Wrap Bit setting (W6-W4).

To avoid accidental reset, both “Enable Reset (66h)” and “Reset (99h)” instructions must be issued in sequence. Any other instructions other than “Reset (99h)” after the “Enable Reset (66h)” instruction will disable the “Reset Enable” state. A new sequence of “Enable Reset (66h)” and “Reset (99h)” is needed to reset the device. Once the Reset instruction is accepted by the device, the device will take approximately 300us to reset. During this period, no instruction will be accepted.

The Enable Reset (66h) and Reset (99h) instruction sequence is shown in ***Figure 11***.

Data corruption may happen if there is an on-going or suspended internal Erase or Program operation when Reset instruction sequence is accepted by the device. It is recommended to check the BUSY bit and the SUS bit in Status Register before issuing the Reset instruction sequence.

Figure 11. Enable Reset (66h) and Reset (99h) Instruction Sequence

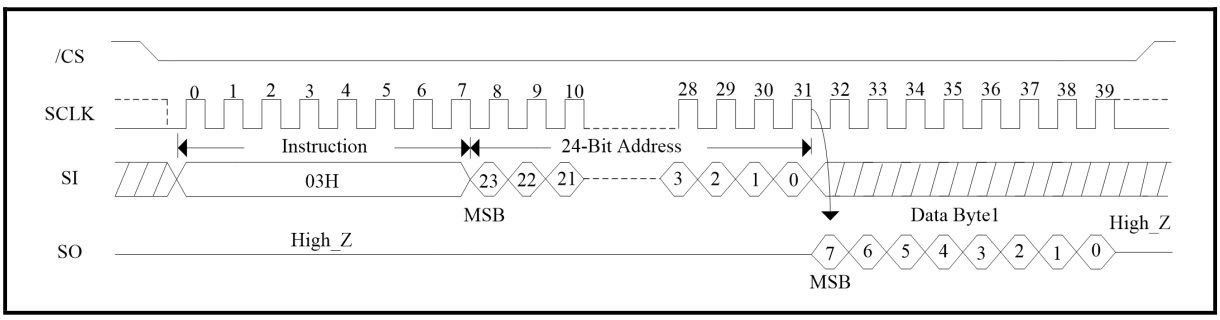


7.2 Read Instructions

7.2.1 Read Data (03H)

See ***Figure 12***, the Read Data Bytes (READ) instruction is followed by a 3-byte address (A23-A0), each bit being latched-in during the rising edge of SCLK. Then the memory content, at that address, is shifted out on SO, each bit being shifted out, at a Max frequency fR, during the falling edge of SCLK. The address is automatically incremented to the next higher address after each byte of data is shifted out allowing for a continuous stream of data. This means that the entire memory can be accessed with a single instruction as long as the clock continues. The instruction is completed by driving /CS high. The whole memory can be read with a single Read Data Bytes (READ) instruction. Any Read Data Bytes (READ) instruction, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

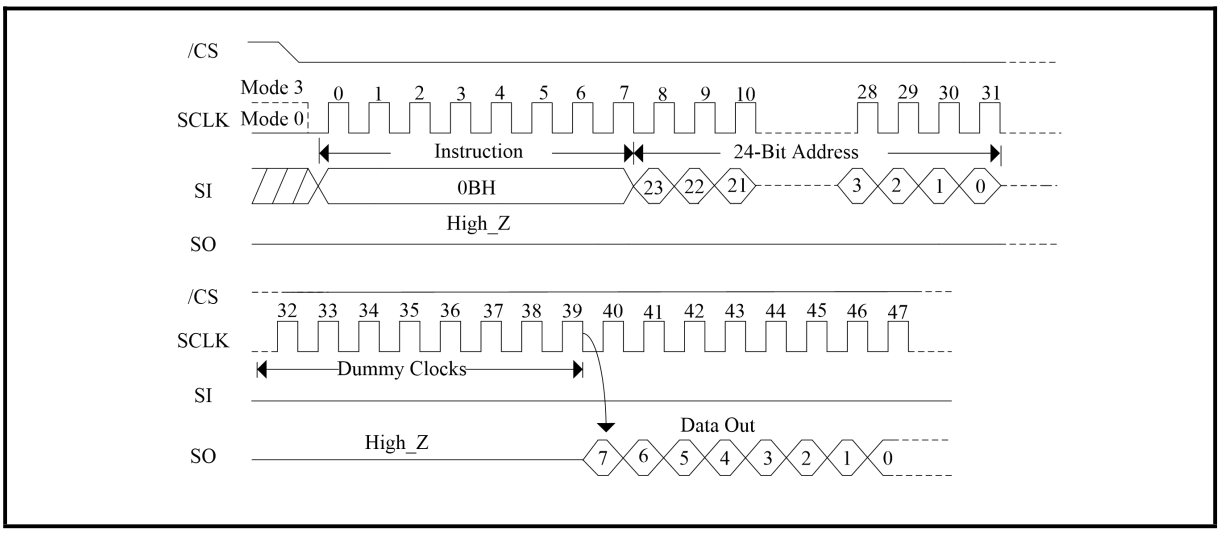
Figure 12. Read Data Bytes Sequence Diagram



7.2.2 Fast Read (0BH)

See ***Figure 13***, the Read Data Bytes at Higher Speed (Fast Read) instruction is for quickly reading data out. It is followed by a 3-byte address (A23-A0) and a dummy byte, each bit being latched-in during the rising edge of SCLK. Then the memory content, at that address, is shifted out on SO, each bit being shifted out, at a Max frequency fc, during the falling edge of SCLK. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out.

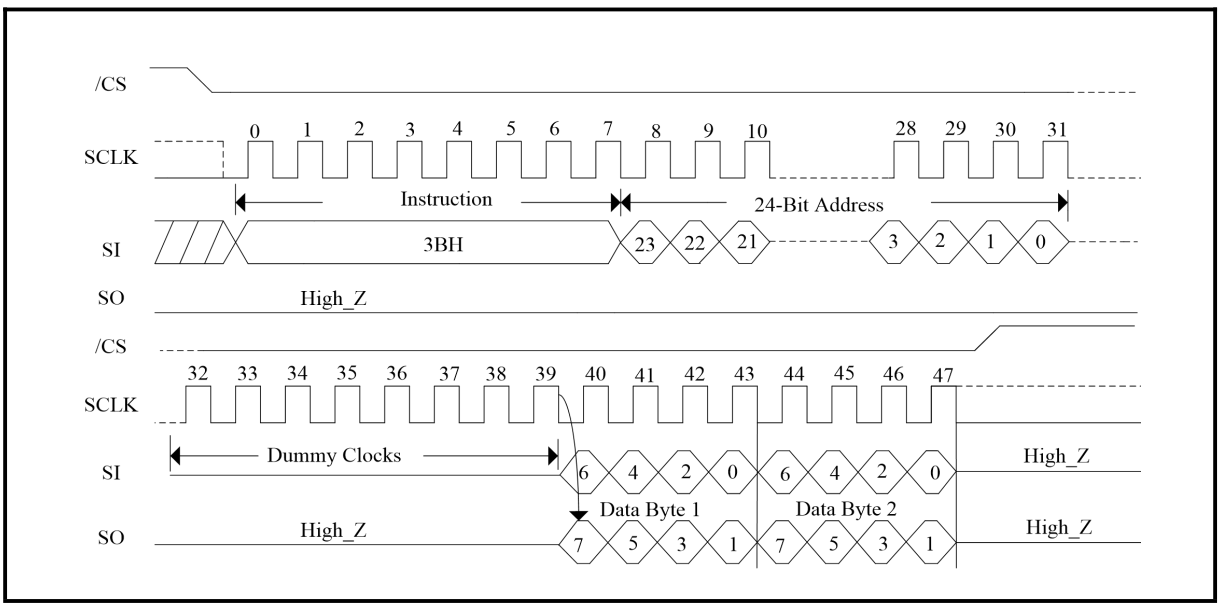
Figure 13. Fast Read Sequence Diagram



7.2.3 Dual Output Fast Read (3BH)

See ***Figure 14***, the Dual Output Fast Read instruction is followed by 3-byte address (A23-A0) and a dummy byte, each bit being latched in during the rising edge of SCLK, then the memory contents are shifted out 2-bit per clock cycle from SI and SO. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out.

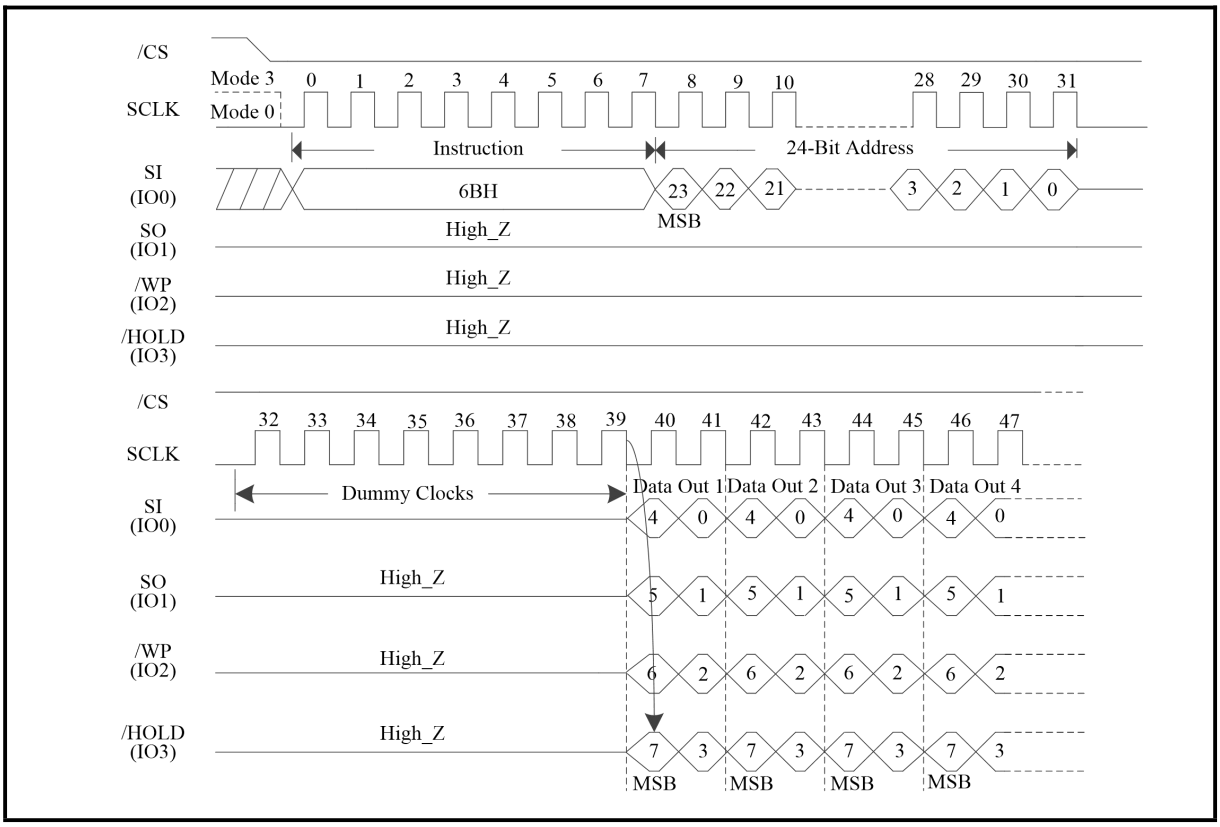
Figure 14. Dual Output Fast Read Sequence Diagram



7.2.4 Quad Output Fast Read (6BH)

See ***Figure 15***, the Quad Output Fast Read instruction is followed by 3-byte address (A23-A0) and a dummy byte, each bit being latched in during the rising edge of SCLK, then the memory contents are shifted out 4-bit per clock cycle from IO3, IO2, IO1 and IO0. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The Quad Enable bit (QE) of Status Register must be set to enable.

Figure 15. Quad Output Fast Read Sequence Diagram



7.2.5 Dual I/O Fast Read (BBH)

See ***Figure 16***, the Dual I/O Fast Read instruction is similar to the Dual Output Fast Read instruction but with the capability to input the 3-byte address (A23-0) and a “Continuous Read Mode” byte 2-bit per clock by SI and SO, each bit being latched in during the rising edge of SCLK, then the memory contents are shifted out 2-bit per clock cycle from SI and SO. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out.

Dual I/O Fast Read with “continuous Read Mode”

The Dual I/O Fast Read instruction can further reduce instruction overhead through setting the “continuous Read Mode” bits (M7-4) after the inputs 3-byte address A23-A0).If the “continuous Read Mode” bits(M5-4)=(1,0),then the next Dual I/O fast Read instruction (after CS/ is raised and then lowered) does not require the BBH instruction code. The instruction sequence is shown in the following ***Figure 16***. If the “continuous Read Mode” bits (M5-4) does not equal (1,0), the next instruction requires the first BBH instruction code, thus returning to normal operation. A “continuous Read Mode” Reset instruction can be used to reset (M5-4) before issuing normal instruction.

Figure 16. Dual I/O Fast Read Sequence Diagram (Initial instruction or previous (M5-4)≠(1,0))

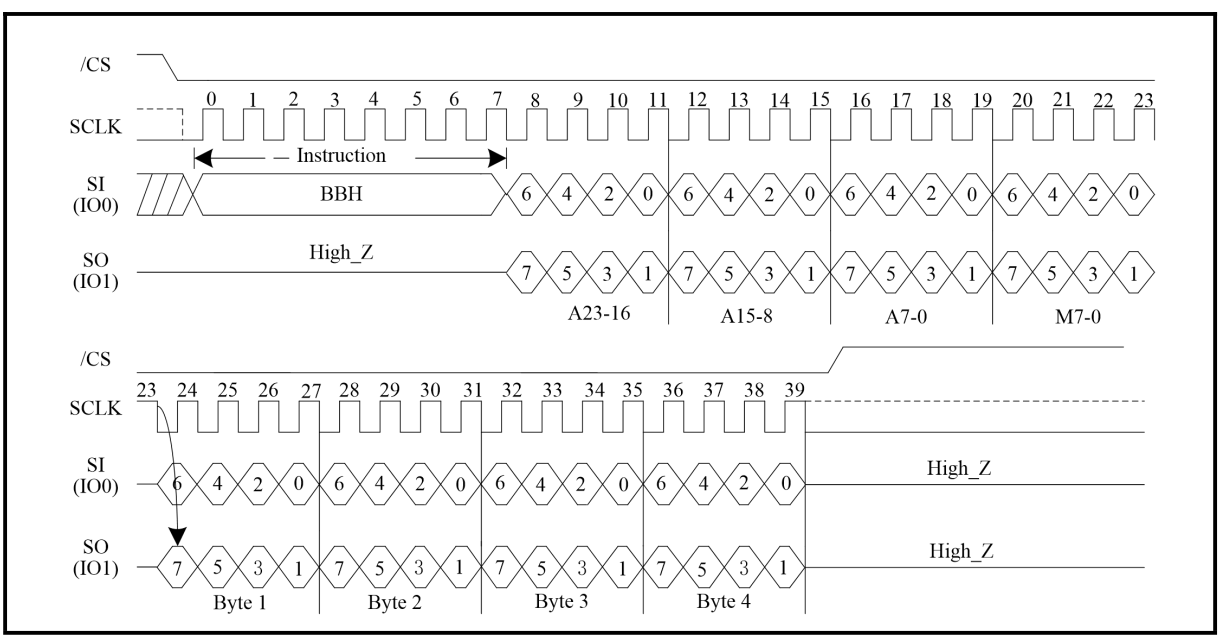
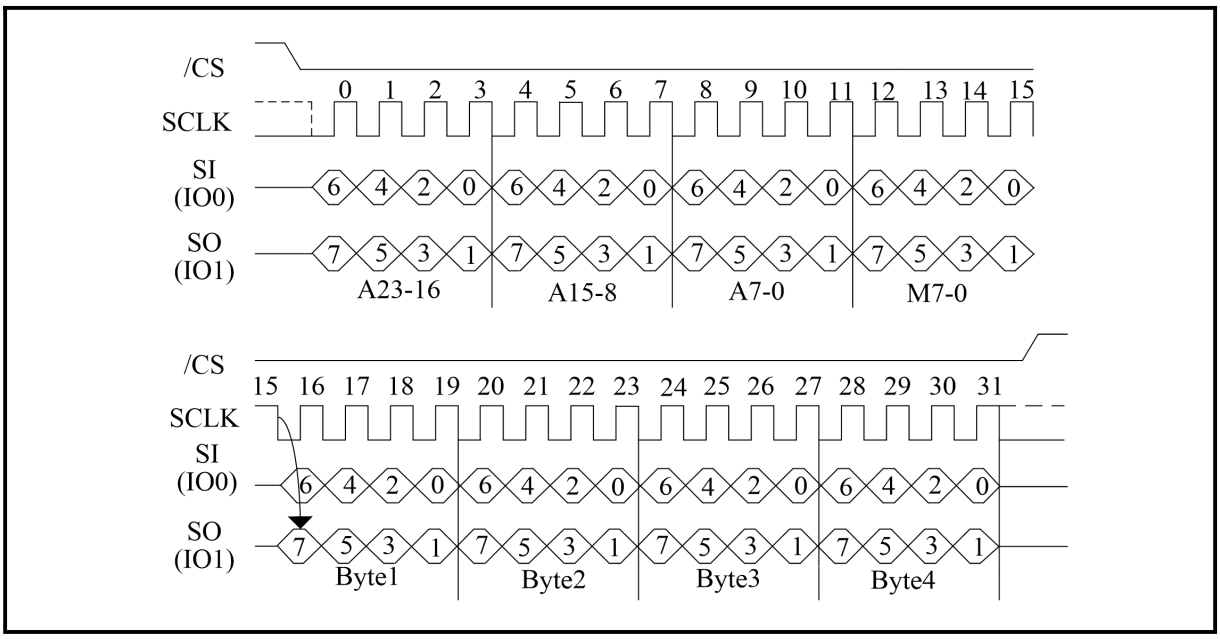


Figure 17. Dual I/O Fast Read Sequence Diagram (Previous instruction set (M5-4) =(1,0))



7.2.6 Quad I/O Fast Read (EBH)

See ***Figure 18***, the Quad I/O Fast Read instruction is similar to the Dual I/O Fast Read instruction but with the capability to input the 3-byte address (A23-0) and a “Continuous Read Mode” byte and 4-dummy clock 4-bit per clock by IO0, IO1, IO3, IO4, each bit being latched in during the rising edge of SCLK, then the memory contents are shifted out 4-bit per clock cycle from IO0, IO1, IO2, IO3. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The Quad Enable bit (QE) of Status Register must be set to enable for the Quad I/O Fast read instruction, as shown in ***Figure 18***.

Quad I/O Fast Read with “Continuous Read Mode”

The Quad I/O Fast Read instruction can further reduce instruction overhead through setting the “Continuous Read Mode” bits (M7-0) after the input Address bits (A23-0), If the “Continuous Read Mode” bits (M5-4)= (1,0), then the next Fast Read Quad I/O instruction(after /CS is raised and then lowered) does not require the EBH instruction code. If the “Continuous Read Mode” bits M5-4 do not equal to (1,0), the next instruction requires the first EBH instruction code, thus returning to normal operation. A “Continuous Read Mode” Reset instruction can also be used to reset (M5-4) before issuing normal instruction.

Figure 18. Quad I/O Fast Read Sequence Diagram (Initial instruction or previous (M5-4≠(1,0)))

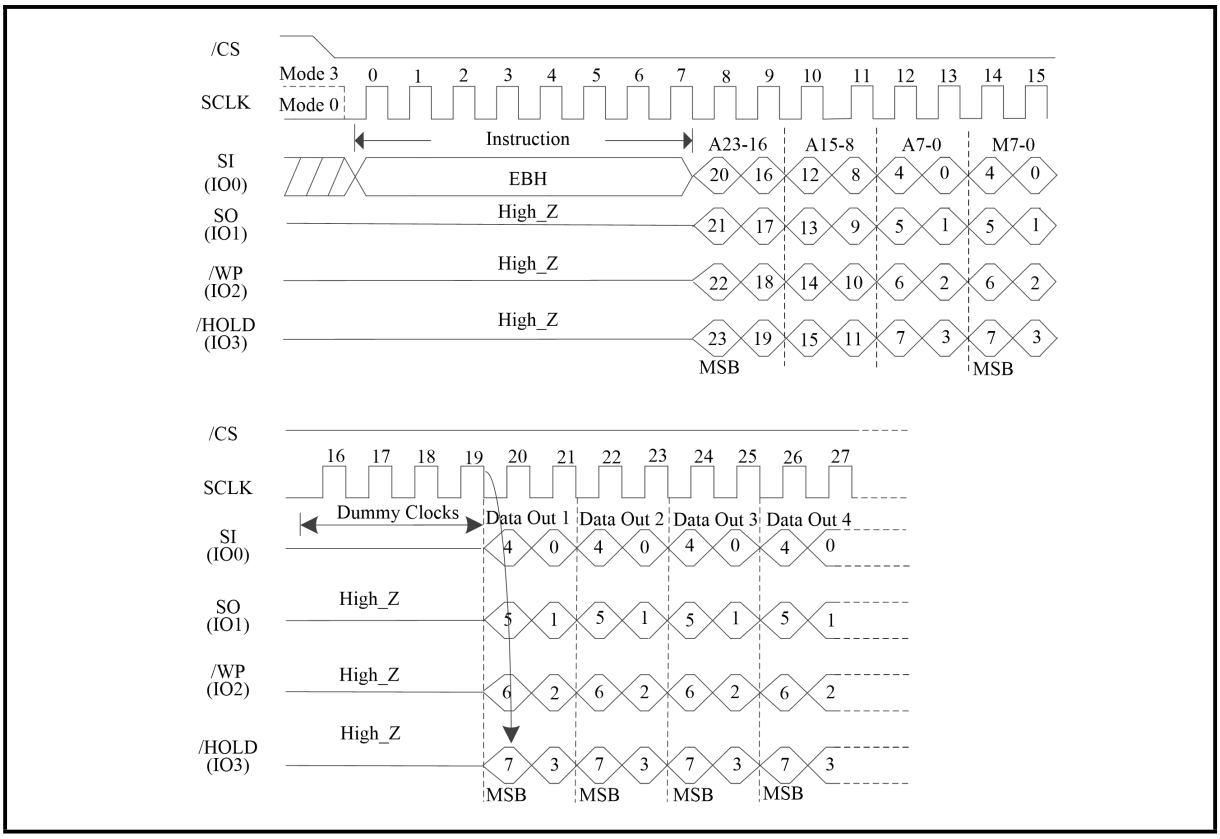
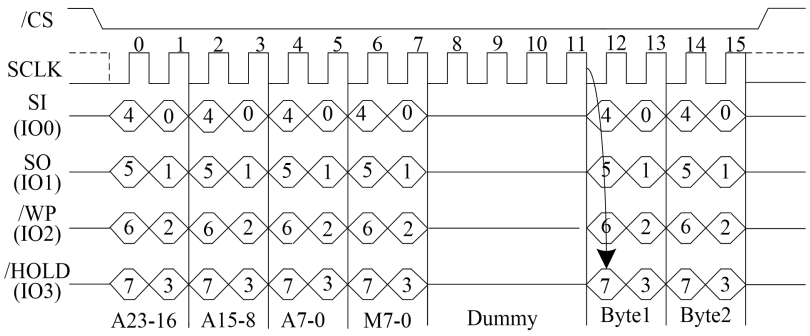


Figure 19. Quad I/O Fast Read Sequence Diagram (Initial instruction or previous (M5-4=(1,0)))



Quad I/O Fast Read with "8/16/32/64-Byte Wrap Around"

The Quad I/O Fast Read instruction can also be used to access a specific portion within a page by issuing a "Set Burst with Wrap" (77H) instruction prior to EBH. The "Set Burst with Wrap" (77H) instruction can either enable or disable the "Wrap Around" feature for the following EBH instructions. When "Wrap Around" is enabled, the data being accessed can be limited to either an 8, 16, 32 or 64-byte section of a 256-byte page. The output data starts at the initial address specified in the instruction, once it reaches the ending boundary of the 8/16/32/64-byte section, the output will wrap around to the beginning boundary automatically until /CS is pulled high to terminate the instruction.

The Burst with Wrap feature allows applications that use cache to quickly fetch a critical address and then fill the cache afterwards within a fixed length (8/16/32/64-byte) of data without issuing multiple read instructions.

The "Set Burst with Wrap" instruction allows three "Wrap Bits", W6-4 to be set. The W4 bit is used to enable or disable the "Wrap Around" operation while W6-5 are used to specify the length of the wrap around section within a page.

7.2.7 Quad I/O Word Fast Read (E7H)

The Quad I/O Word Fast Read instruction is similar to the Quad Fast Read instruction except that the lowest address bit (A0) must equal 0 and 2-dummy clock. The instruction sequence is shown in the followed ***Figure 20***, the first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The Quad Enable bit (QE) of Status Register (S9) must be set to enable for the Quad I/O Word Fast Read instruction. The Quad Enable bit (QE) of Status Register must be set to enable.

Quad I/O Word Fast Read with "Continuous Read Mode"

The Quad I/O Word Fast Read instruction can further reduce instruction overhead through setting the "Continuous Read Mode" bits (M7-0) after the input 3-byte Address bits (A23-0). If the "Continuous Read Mode" bits (M5-4) = (1, 0), then the next Quad I/O Fast Read instruction (after /CS is raised and then lowered) does not require the E7H instruction code, the instruction sequence is shown in the followed ***Figure 21***. If the "Continuous Read Mode" bits M5-4 do not equal to (1,0), the next instruction requires the first E7H instruction code, thus returning to normal operation. A "Continuous Read Mode" Reset instruction can also be used to reset (M5-4) before issuing normal instruction.

Figure 20. Quad I/O Word Fast Read Sequence Diagram (Initial instruction or previous (M5-4)≠(1,0))

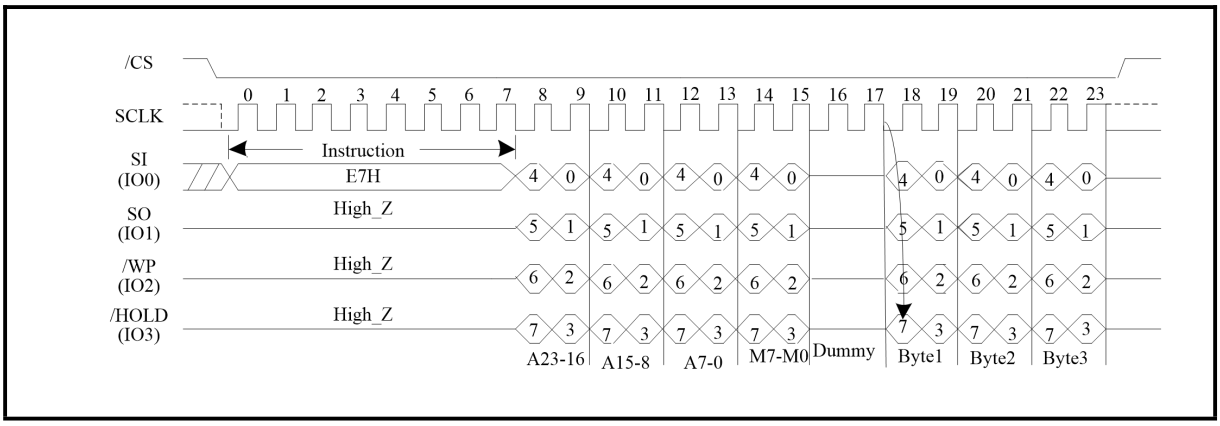
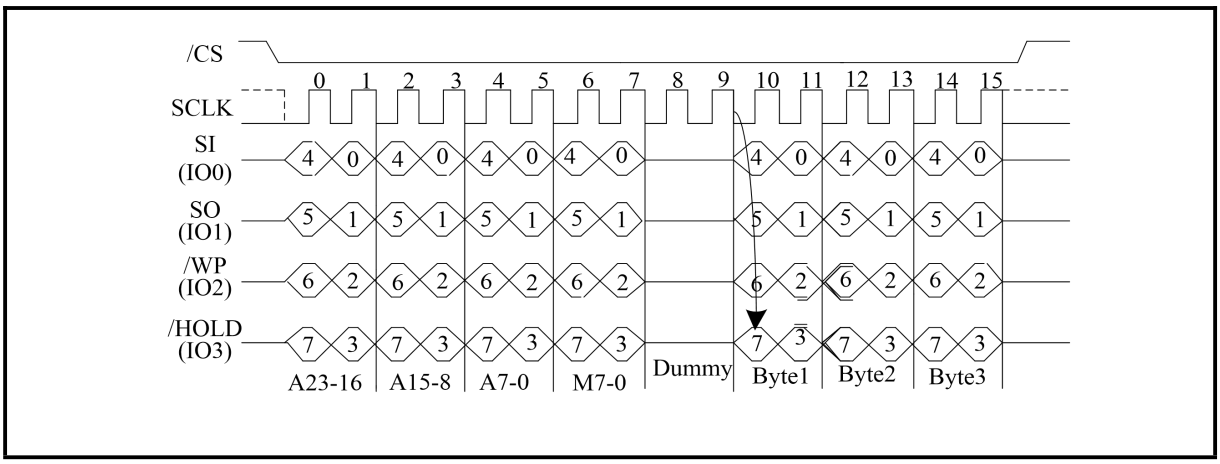


Figure 21. Quad I/O Word Fast Read Sequence Diagram (Initial instruction or previous (M5-4)=(1,0))



Quad I/O Word Fast Read with "8/16/32/64-Byte Wrap Around" in standard SPI mode

The Quad I/O Fast Read instruction can also be used to access a specific portion within a page by issuing a "Set Burst with Wrap" (77H) instruction prior to E7H. The "Set Burst with Wrap" (77H) instruction can either enable or disable the "Wrap Around" feature for the following E7H instructions. When "Wrap Around" is enabled, the data being accessed can be limited to either an 8, 16, 32 or 64-byte section of a 256-byte page. The output data starts at the initial address specified in the instruction, once it reaches the ending boundary of the 8/16/32/64-byte section, the output will wrap around to the beginning boundary automatically until /CS is pulled high to terminate the instruction.

The Burst with Wrap feature allows applications that use cache to quickly fetch a critical address and then fill the cache afterwards within a fixed length (8/16/32/64-byte) of data without issuing multiple read instructions.

The "Set Burst with Wrap" instruction allows three "Wrap Bits", W6-4 to be set. The W4 bit is used to enable or disable the "Wrap Around" operation while W6-5 are used to specify the length of the wrap around section within a page.

7.2.8 Set Burst with Wrap (77H)

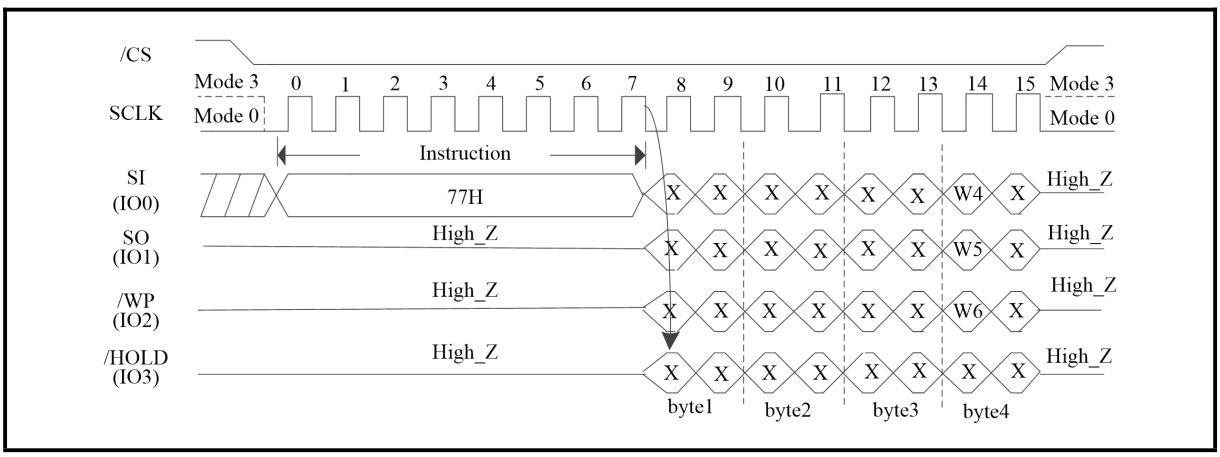
See ***Figure 22***, The Set Burst with Wrap instruction is used in conjunction with “EBH” and “E7H” instructions to access a fixed length of 8/16/32/64-byte section within a 256-byte page, in standard SPI mode.

The Set Burst with Wrap instruction sequence:/CS goes low ->Send Set Burst with Wrap instruction ->Send24 Dummy bits ->Send 8 bits” Wrap bits”->/CS goes high.

If W6-4 is set by a Set Burst with Wrap instruction, all the following “EBH” and “E7H” instructions will use the W6-4 setting to access the 8/16/32/64-byte section within any page. To exit the “Wrap Around” function and return to normal read operation, another Set Burst with Wrap instruction should be issued to set W4=1. The default value of W4 upon power on is 1.

W6 , W5		W4 = 0		W4 =1 (DEFAULT)	
		Wrap Around	Wrap Length	Wrap Around	Wrap Length
0	0	Yes	8-byte	No	N/A
0	1	Yes	16-byte	No	N/A
1	0	Yes	32-byte	No	N/A
1	1	Yes	64-byte	No	N/A

Figure 22. Set Burst with Wrap Sequence Diagram



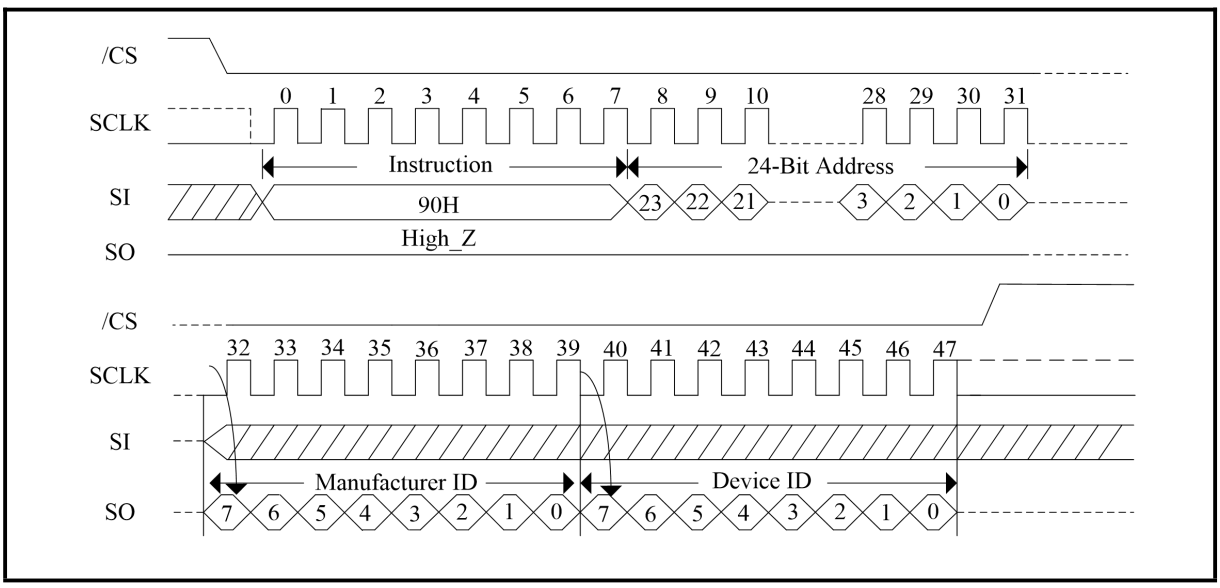
7.3 ID and Security Instructions

7.3.1 Read Manufacture ID/ Device ID (90H)

See ***Figure 23***, The Read Manufacturer/Device ID instruction is an alternative to the Release from Power-Down/Device ID instruction that provides both the JEDEC assigned Manufacturer ID and the specific Device ID.

The instruction is initiated by driving the /CS pin low and shifting the instruction code “90H” followed by a 24-bit address (A23-A0) of 000000H. If the 24-bit address is initially set to 000001H, the Device ID will be read first.

Figure 23. Read Manufacture ID/ Device ID Sequence Diagram

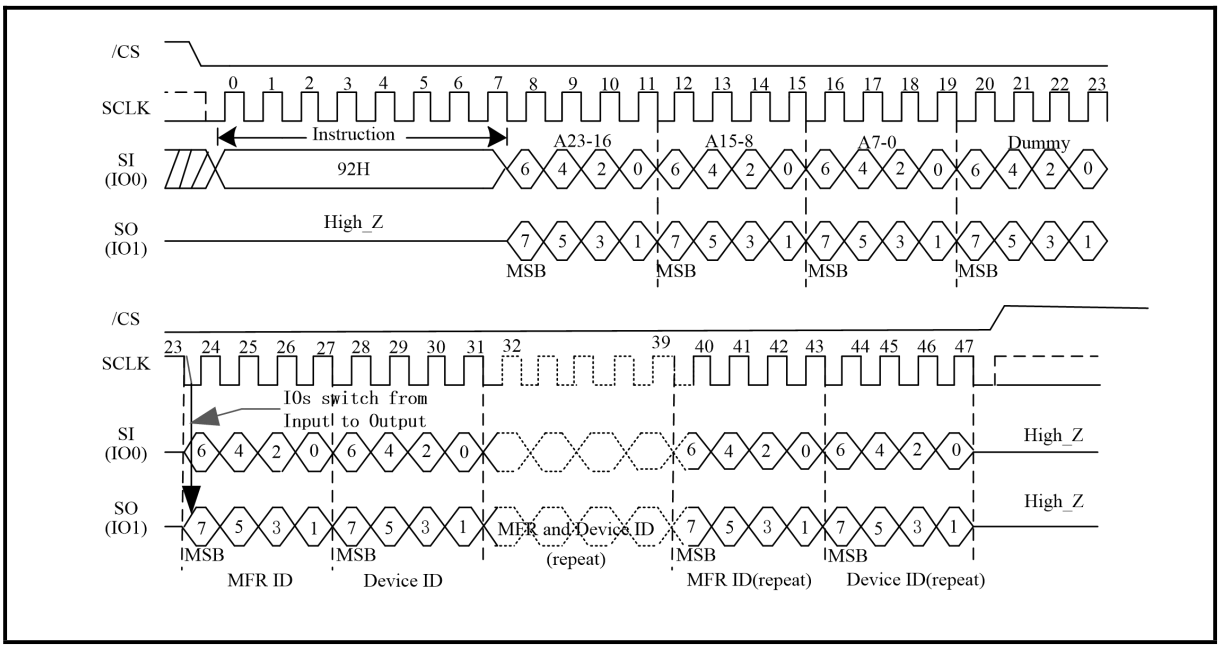


7.3.2 Dual I/O Read Manufacture ID/ Device ID (92H)

See ***Figure 24***, the Dual I/O Read Manufacturer/Device ID instruction is an alternative to the Release from Power-Down/Device ID instruction that provides both the JEDEC assigned Manufacturer ID and the specific Device ID by Dual I/O.

The instruction is initiated by driving the /CS pin low and shifting the instruction code “92H” followed by a 24-bit address (A23-A0) of 000000H. If the 24-bit address is initially set to 000001H, the Device ID will be read first.

Figure 24. Dual I/O Read Manufacture ID/ Device ID Sequence Diagram

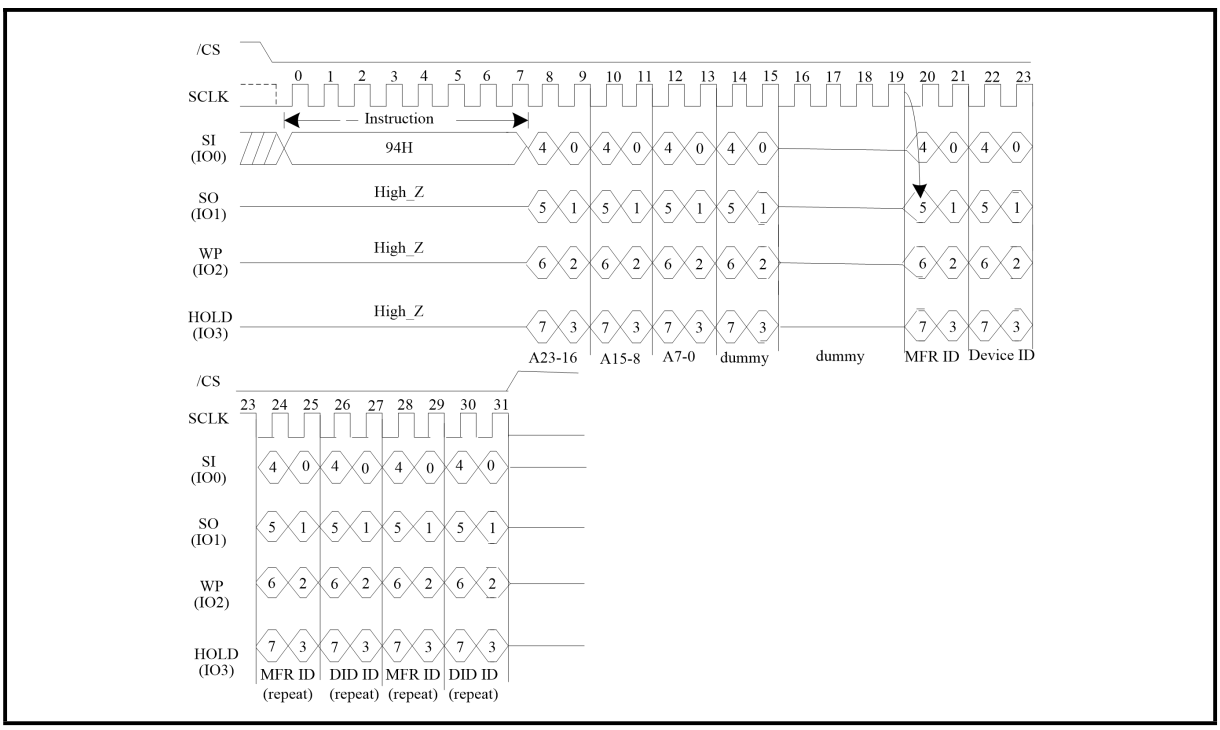


7.3.3 Quad I/O Read Manufacture ID/ Device ID (94H)

See ***Figure 25***, the Quad I/O Read Manufacturer/Device ID instruction is an alternative to the Release from Power-Down/Device ID instruction that provides both the JEDEC assigned Manufacturer ID and the specific Device ID by quad I/O. The Quad Enable bit (QE) of Status Register must be set to enable.

The instruction is initiated by driving the /CS pin low and shifting the instruction code “94H” followed by a 24-bit address (A23-A0) of 000000H and 4 dummy clocks. If the 24-bit address is initially set to 000001H, the Device ID will be read first.

Figure 25. Quad I/O Read Manufacture ID/ Device ID Sequence Diagram

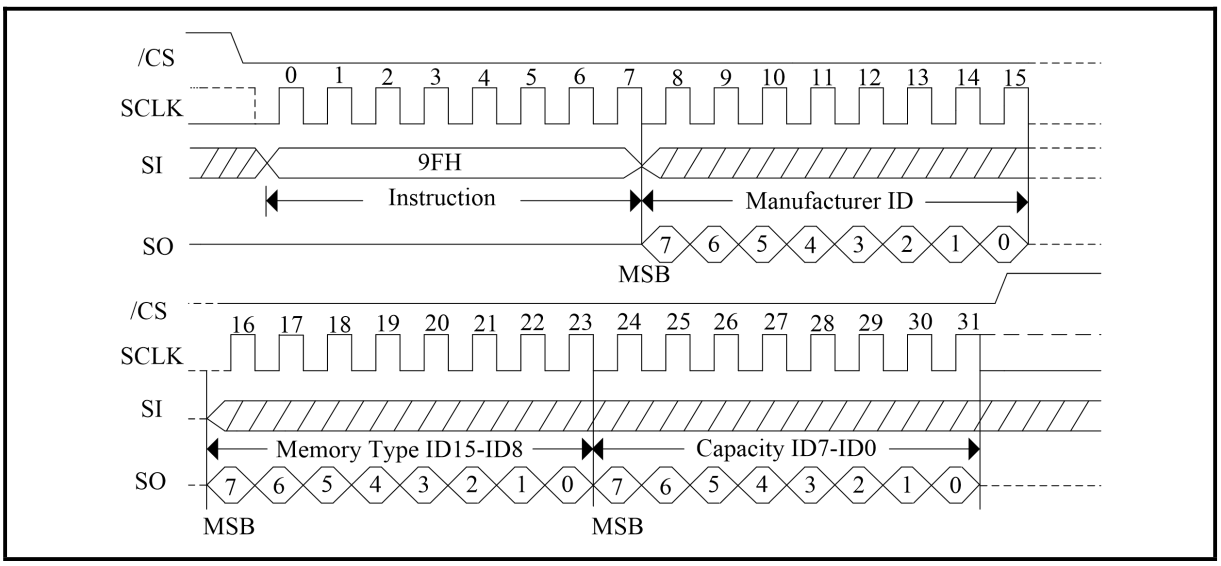


7.3.4 Read JEDEC ID (9FH)

The JEDEC ID instruction allows the 8-bit manufacturer identification to be read, followed by two bytes of device identification. The device identification indicates the memory type in the first byte, and the memory capacity of the device in the second byte. JEDEC ID instruction while an Erase or Program cycle is in progress, is not decoded, and has no effect on the cycle that is in progress. The JEDEC ID instruction should not be issued while the device is in Deep Power-Down Mode.

See ***Figure 26***, the device is first selected by driving /CS to low. Then, the 8-bit instruction code for the instruction is shifted in. This is followed by the 24-bit device identification, stored in the memory, being shifted out on Serial Data Output, each bit being shifted out during the falling edge of Serial Clock. The JEDEC ID instruction is terminated by driving /CS to high at any time during data output. When /CS is driven high, the device is put in the Standby Mode. Once in the Standby Mode, the device waits to be selected, so that it can receive, decode and execute instructions.

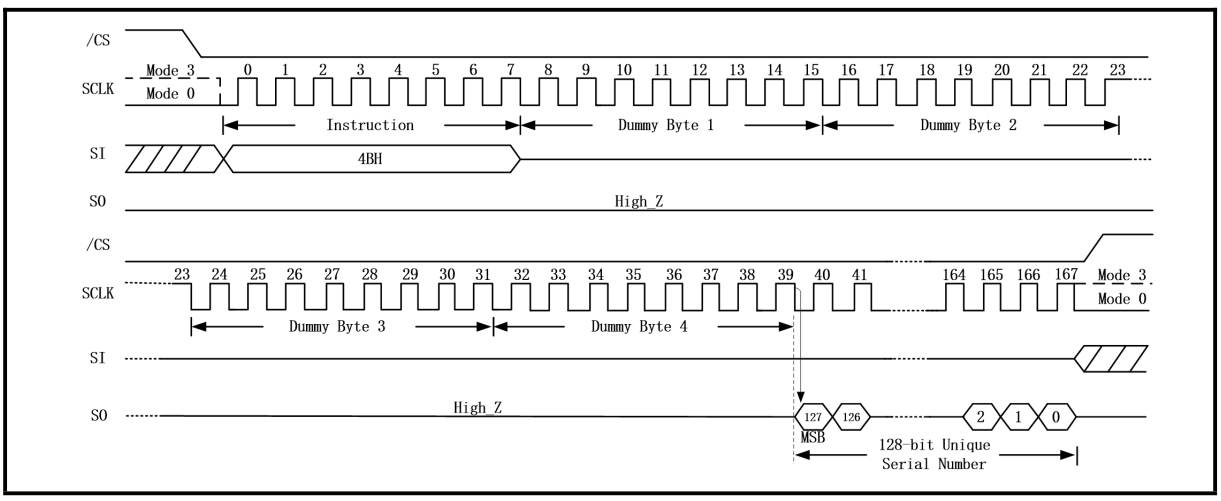
Figure 26. JEDEC ID Sequence Diagram



7.3.5 Read Unique ID Number (4Bh)

The Read Unique ID Number instruction accesses a factory-set read-only 128-bit number that is unique to each BY25Q128FS device. The ID number can be used in conjunction with user software methods to help prevent copying or cloning of a system. The Read Unique ID instruction is initiated by driving the /CS pin low and shifting the instruction code “4Bh” followed by four bytes of dummy clocks. After which, the 128-bit ID is shifted out on the falling edge of SCLK as shown in ***Figure 27.***

Figure 27. Read Unique ID Sequence Diagram

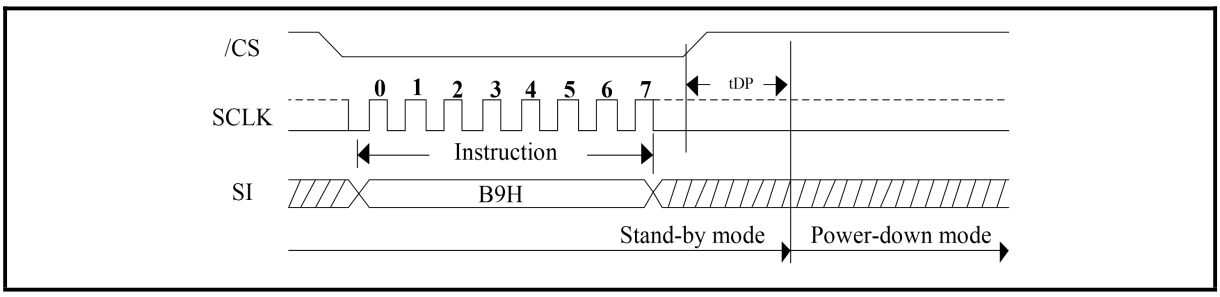


7.3.6 Deep Power-Down (B9H)

Although the standby current during normal operation is relatively low, standby current can be further reduced with the Deep Power-down instruction. The lower power consumption makes the Deep Power-down (DPD) instruction especially useful for battery powered applications (***see ICC1 and ICC2***). The instruction is initiated by driving the /CS pin low and shifting the instruction code "B9h" as shown in ***Figure 28***.

The /CS pin must be driven high after the eighth bit has been latched. If this is not done the Deep Power down instruction will not be executed. After /CS is driven high, the power-down state will entered within the time duration of tDP. While in the power-down state only the Release from Deep Power-down/Device ID instruction, software reset sequence or hardware reset sequence, which restores the device to normal operation, will be recognized. All other Instructions are ignored. This includes the Read Status Register instruction, which is always available during normal operation. Ignoring all but one instruction also makes the Power Down state a useful condition for securing maximum write protection. The device always powers-up in the normal operation with the standby current of ICC1.

Figure 28. Deep Power-Down Sequence Diagram



7.3.7 Release from Deep Power-Down/Read Device ID (ABH)

The Release from Power-Down or Device ID instruction is a multi-purpose instruction. It can be used to release the device from the Power-Down state or obtain the devices electronic identification (ID) number.

See ***Figure 29***, to release the device from the Power-Down state, the instruction is issued by driving the /CS pin low, shifting the instruction code "ABH" and driving /CS high Release from Power-Down will take the time duration of tRES1 (***See AC Characteristics***) before the device will resume normal operation and other instruction are accepted. The /CS pin must remain high during the tRES1 time duration.

When used only to obtain the Device ID while not in the Power-Down state, the instruction is initiated by driving the /CS pin low and shifting the instruction code "ABH" followed by 3-dummy byte. The Device ID bits are then shifted out on the falling edge of SCLK with most significant bit (MSB) first as shown in ***Figure 30***. The Device ID value for the BY25Q128FS is listed in Manufacturer and Device Identification table. The Device ID can be read continuously. The instruction is completed by driving /CS high.

When used to release the device from the Power-Down state and obtain the Device ID, the instruction is the same as previously described, and shown in ***Figure 30***, except that after /CS is driven high it must remain high for a time duration of tRES2 (***See AC Characteristics***). After this time duration the device will resume normal operation and other instruction will be accepted. If the Release from Power-Down/Device ID instruction is issued while an Erase, Program or Write cycle is in process (when WIP equal 1) the instruction is ignored and will not have any effects on the current cycle.

Figure 29. Release Power-Down Sequence Diagram

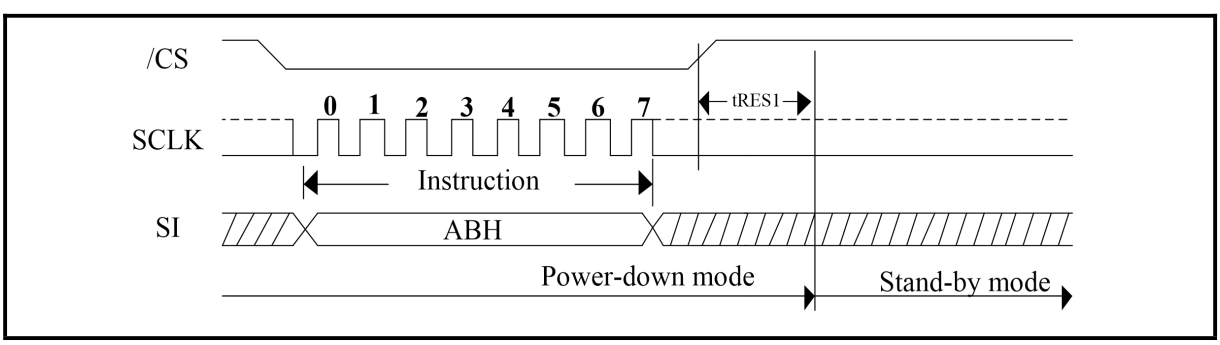
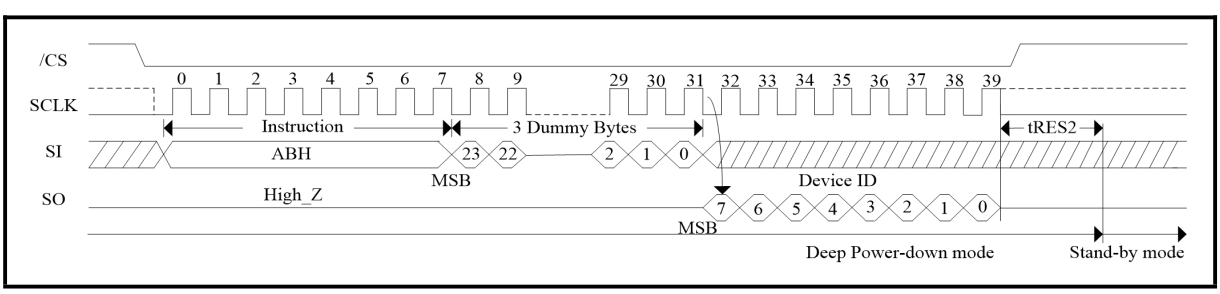


Figure 30. Release Power-Down/Read Device ID Sequence Diagram

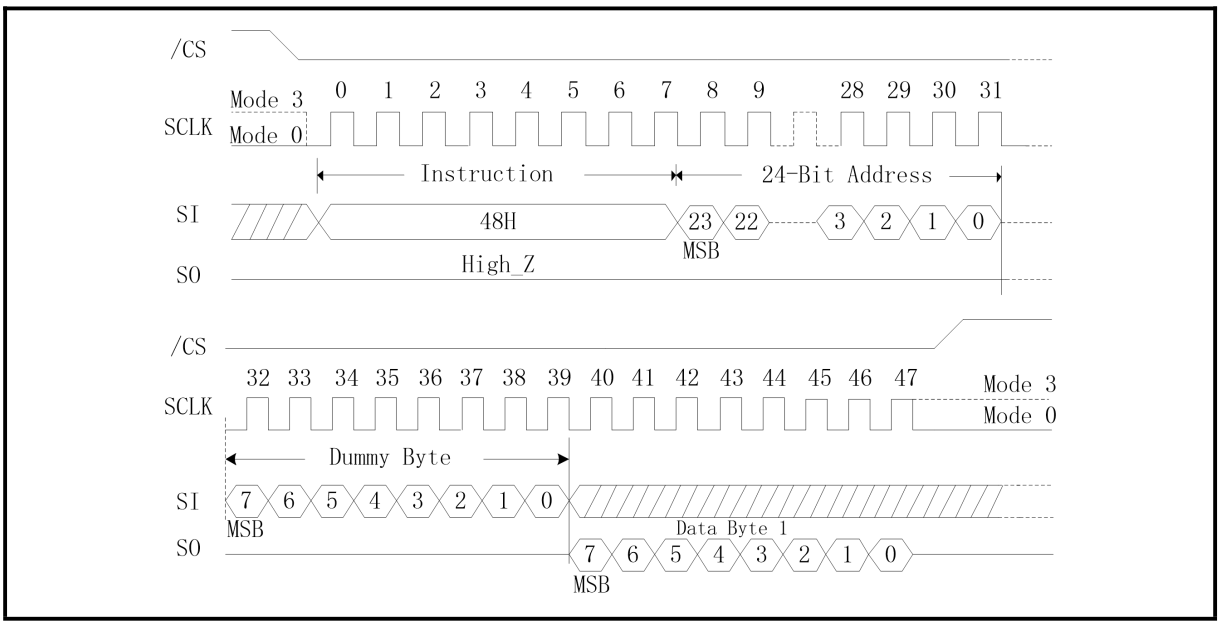


7.3.8 Read Security Registers (48H)

See ***Figure 31***, the instruction is followed by a 3-byte address (A23-A0) and the dummy byte. Each bit being latched-in during the rising edge of SCLK. Then the memory content, at that address, is shifted out on SO, each bit being shifted out, at a Max frequency fC, during the falling edge of SCLK. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. Once the A9-A0 address reaches the last byte of the register (Byte 3FFH), it will reset to 000H, the instruction is completed by driving /CS high.

ADDRESS	A23-A16	A15-12	A11-10	A9-0
Security Register #1	00H	0 0 0 1	0 0	Byte Address
Security Register #2	00H/	0 0 1 0	0 0	Byte Address
Security Register #3	00H	0 0 1 1	0 0	Byte Address

Figure 31. Read Security Registers instruction Sequence Diagram



7.3.9 Erase Security Registers (44H)

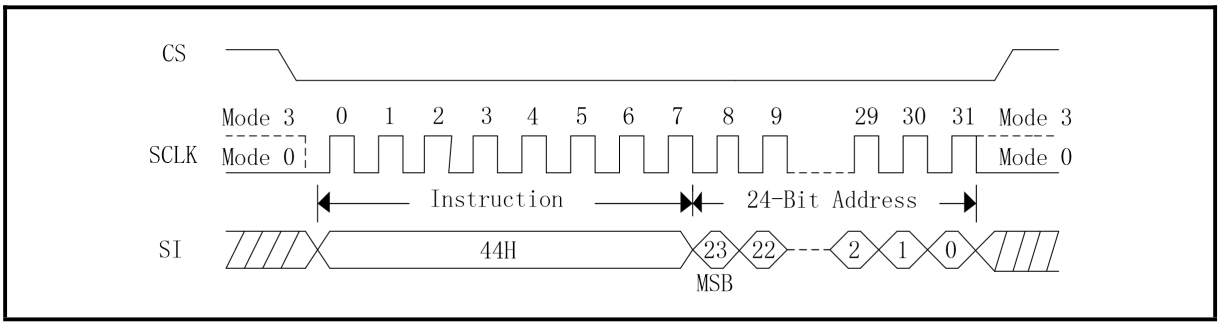
The BY25Q128FS provides three 1024-byte Security Registers which can be erased and programmed individually. These registers may be used by the system manufacturers to store security and other important information separately from the main memory array.

See ***Figure 32***, the Erase Security Registers instruction is similar to Block/Sector Erase instruction. A Write Enable instruction must previously have been executed to set the Write Enable Latch bit.

The Erase Security Registers instruction sequence: /CS goes low sending Erase Security Registers instruction /CS goes high. /CS must be driven high after the eighth bit of the instruction code has been latched in otherwise the Erase Security Registers instruction is not executed. As soon as /CS is driven high, the self-timed Erase Security Registers cycle (whose duration is tSE) is initiated. While the Erase Security Registers cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Erase Security Registers cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch bit is reset. The Security Registers Lock Bit (LB) in the Status Register can be used to OTP protect the security registers. Once the LB bit is set to 1, the Security Registers will be permanently locked; the Erase Security Registers instruction will be ignored.

ADDRESS	A23-A16	A15-12	A11-10	A9-0
Security Register #1	00H	0 0 0 1	0 0	Byte Address
Security Register #2	00H	0 0 1 0	0 0	Byte Address
Security Register #3	00H	0 0 1 1	0 0	Byte Address

Figure 32. Erase Security Registers instruction Sequence Diagram



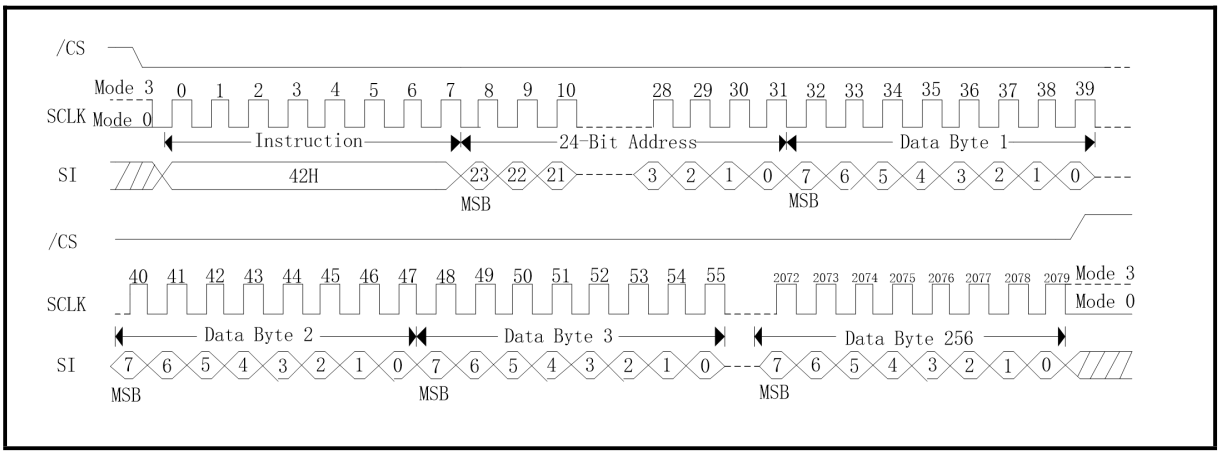
7.3.10 Program Security Registers (42H)

See ***Figure 33***, the Program Security Registers instruction is similar to the Page Program instruction. It allows from one byte to 1024 bytes of security register data to be programmed by four times (one time program 256 bytes). A Write Enable instruction must previously have been executed to set the Write Enable Latch bit before sending the Program Security Registers instruction. The Program Security Registers instruction is entered by driving /CS Low, followed by the instruction code (42H), 3-byte address and at least one data byte on SI. As soon as /CS is driven high, the self-timed Program Security Registers cycle (whose duration is tPP) is initiated. While the Program Security Registers cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Program Security Registers cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch bit is reset.

If the Security Registers Lock Bit (LB3/LB2/LB1) is set to 1, the Security Registers will be permanently locked. Program Security Registers instruction will be ignored.

ADDRESS	A23-A16	A15-12	A11-10	A9-0
Security Register #1	00H	0 0 0 1	0 0	Byte Address
Security Register #2	00H	0 0 1 0	0 0	Byte Address
Security Register #3	00H	0 0 1 1	0 0	Byte Address

Figure 33. Program Security Registers instruction Sequence Diagram



7.3.11 Read Serial Flash Discoverable Parameter (5AH)

See ***Figure 34***, The Serial Flash Discoverable Parameter (SFDP) standard provides a consistent method of describing the functional and feature capabilities of serial flash devices in a standard set of internal parameter tables. These parameter tables can be interrogated by host system software to enable adjustments needed to accommodate divergent features from multiple vendors. The concept is similar to the one found in the Introduction of JEDEC Standard, JESD68 on CFI. SFDP is a standard of JEDEC Standard No.216.

The Read SFDP instruction is initiated by driving the /CS pin low and shifting the instruction code “5Ah” followed by a 24-bit address (A23-A0) into the SI pin. Eight “dummy” clocks are also required in SPI mode.

Figure 34. Read Serial Flash Discoverable Parameter instruction Sequence Diagram

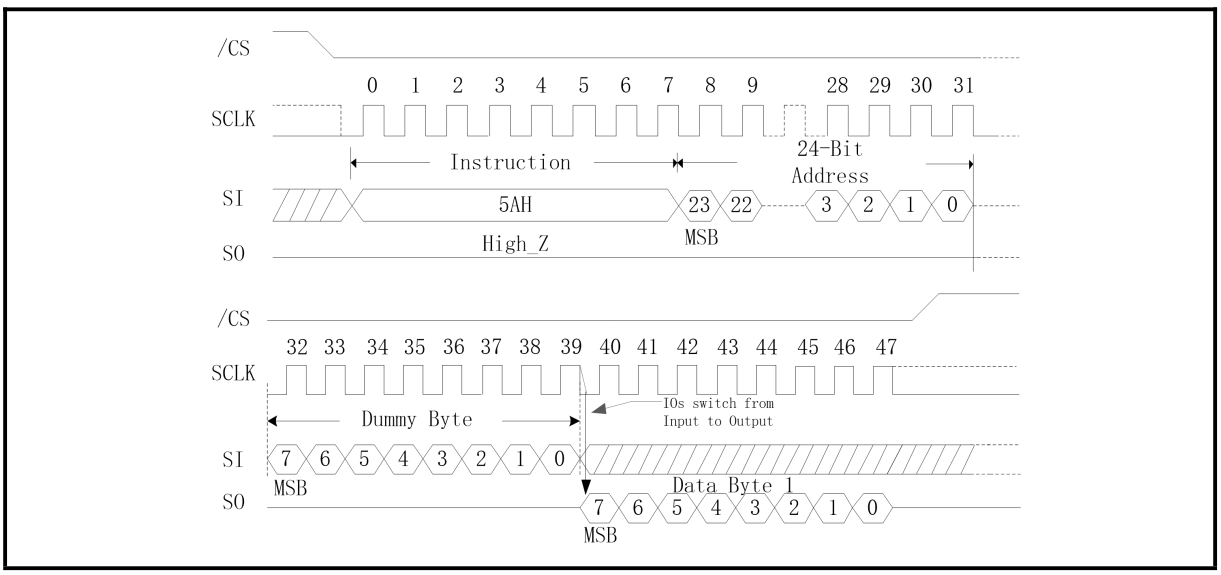


Table 7.3.11.a. Signature and Parameter Identification Data Values

Description	Comment	Add(H) (Byte)	DW Add (Bit)	Data	Data
SFDP Signature	Fixed:50444653H	00H	07:00	53H	53H
		01H	15:08	46H	46H
		02H	23:16	44H	44H
		03H	31:24:	50H	50H
SFDP Minor Revision Number	Start from 00H	04H	07:00	00H	00H
SFDP Major Revision Number	Start from 01H	05H	15:08	01H	01H
Number of Parameters Headers	Start from 00H	06H	23:16	01 H	01 H
Unused	Contains 0xFFH and can never be changed	07H	31:24	FFH	FFH
ID number (JEDEC)	00H: It indicates a JEDEC specified header	08H	07:00	00H	00H
Parameter Table Minor Revision Number	Start from 0x00H	09H	15:08	00H	00H
Parameter Table Major Revision Number	Start from 0x01H	0AH	23:16	01H	01H
Parameter Table Length (in double word)	How many DWORDs in the Parameter table	0BH	31:24	09H	09H
Parameter Table Pointer (PTP)	First address of JEDEC Flash Parameter table	0CH	07:00	30H	30H
		0DH	15:08	00H	00H
		0EH	23:16	00H	00H
Unused	Contains 0xFFH and can never be changed	0FH	31:24	FFH	FFH
ID Number LSB (Manufacturer ID)	It is indicates BY Technology Device manufacturer ID	10H	07:00	68H	68H
Parameter Table Minor Revision Number	Start from 0x00H	11 H	15:08	00H	00H
Parameter Table Major Revision Number	Start from 0x01H	12H	23:16	01H	01H
Parameter Table Length (in double word)	How many DWORDs in the Parameter table	13H	31:24	03H	03H
Parameter Table Pointer (PTP)	First address of BY Technology Device Flash Parameter table	14H	07:00	60H	60H
		15H	15:08	00H	00H
		16H	23:16	00H	00H
Unused	Contains 0xFFH and can never be changed	17H	31:24	FFH	FFH

Table 7.3.1.b. Parameter Table (0): JEDEC Flash Parameter Tables

Description	Comment	Add(H) (Byte)	DW Add (Bit)	Data	Data
Block/Sector Erase Size	00: Reserved; 01: 4KB erase; 10: Reserved; 11: not support 4KB erase	30H	01:00	01b	E5H
Write Granularity	0: 1Byte, 1: 64Byte or larger		02	1b	
Write Enable Instruction Requested for Writing to Volatile Status Registers	0: Nonvolatile status bit 1: Volatile status bit (BP status register bit)		03	0b	
Write Enable Opcode Select for Writing to Volatile Status Registers	0: Use 50H Opcode, 1: Use 06H Opcode, Note: If target flash status register is Nonvolatile, then bits 3 and 4 must be set to 00b.		04	0b	
Unused	Contains 111b and can never be changed		07:05	111b	
4KB Erase Opcode		31H	15:08	20H	20H
(1 -1 -2) Fast Read	0=Not support, 1=Support	32H	16	1b	F1H
Address Bytes Number used in addressing flash array	00: 3Byte only, 01: 3 or 4Byte, 10: 4Byte only, 11: Reserved		18:17	00b	
Double Transfer Rate (DTR) clocking	0=Not support, 1=Support		19	0b	
(1 -2-2) Fast Read	0=Not support, 1=Support		20	1b	
(1 -4-4) Fast Read	0=Not support, 1=Support		21	1b	
(1 -1 -4) Fast Read	0=Not support, 1=Support		22	1b	
Unused			23	1b	
Unused		33H	31:24	FFH	FFH
Flash Memory Density		37H:34H	31:00	07FFFFFFH	
(1 -4-4) Fast Read Number of Wait states	00000b: Wait states (Dummy Clocks) not support	38H	04:00	00100b	44H
(1 -4-4) Fast Read Number of Mode Bits	000b:Mode Bits not support		07:05	010b	
(1 -4-4) Fast Read Opcode		39H	15:08	EBH	EBH
(1 -1 -4) Fast Read Number of Wait states	00000b: Wait states (Dummy Clocks) not support	3AH	20:16	01000b	08H
(1 -1 -4) Fast Read Number of Mode Bits	000b:Mode Bits not support		23:21	000b	
(1 -1 -4) Fast Read Opcode		3BH	31:24	6BH	6BH
(1 -1 -2) Fast Read Number of Wait states	00000b: Wait states (Dummy Clocks) not support	3CH	04:00	01000b	08H
(1 -1 -2) Fast Read Number of Mode Bits	000b: Mode Bits not support		07:05	000b	
(1 -1 -2) Fast Read Opcode		3DH	15:08	3BH	3BH
(1 -2-2) Fast Read Number of Wait states	0000b: Wait states (Dummy Clocks) not support	3EH	20:16	00010b	42H
(1 -2-2) Fast Read Number of Mode Bits	000b: Mode Bits not support		23:21	010b	
(1 -2-2) Fast Read Opcode		3FH	31:24	BBH	BBH

(2-2-2) Fast Read	0=not support 1=support	40H	00	0b	EEH
Unused			03:01	111b	
(4-4-4) Fast Read	0=not support 1=support		04	0b	
Unused			07:05	111b	
Unused		43H:41H	31:08	0xFFH	0xFFH
Unused		45H:44H	15:00	0xFFH	0xFFH
(2-2-2) Fast Read Number of Wait states	0 0000b: Wait states (Dummy Clocks) not support	46H	20:16	00000b	00H
(2-2-2) Fast Read Number of Mode Bits	000b: Mode Bits not support		23:21	000b	
(2-2-2) Fast Read Opcode		47H	31:24	FFH	FFH
Unused		49H:48H	15:00	0xFFH	0xFFH
(4-4-4) Fast Read Number of Wait states	0 0000b: Wait states (Dummy Clocks) not support	4AH	20:16	000 00b	00H
(4-4-4) Fast Read Number of Mode Bits	000b: Mode Bits not support		23:21	000b	
(4-4-4) Fast Read Opcode		4BH	31:24	FFH	FFH
Sector Type 1 Size	Sector/block size=2^N bytes 0x00b: this sector type don’t exist	4CH	07:00	0CH	0CH
Sector Type 1 erase Opcode		4DH	15:08	20H	20H
Sector Type 2 Size	Sector/block size=2^N bytes 0x00b: this sector type don’t exist	4EH	23:16	0FH	0FH
Sector Type 2 erase Opcode		4FH	31:24	52H	52H
Sector Type 3 Size	Sector/block size=2^N bytes 0x00b: this sector type don’t exist	50H	07:00	10H	10H
Sector Type 3 erase Opcode		51H	15:08	D8H	D8H
Sector Type 4 Size	Sector/block size=2^N bytes 0x00b: this sector type don’t exist	52H	23:16	00H	00H
Sector Type 4 erase Opcode		53H	31:24	FFH	FFH

Table 7.3.1.c. Parameter Table (1): BY Technology Flash Parameter Tables

Description	Comment	Add(H) (Byte)	DW Add (Bit)	Data	Data
Vcc Supply Maximum Voltage	2000H=2.000V 2700H=2.700V 3600H=3.600V	61H:60H	15:00	3600H	3600H
Vcc Supply Minimum Voltage	1650H=1.650V 2250H=2.250V 2350H=2.350V 2700H=2.700V	63H:62H	31:16	2700H	2700H
HW Reset# pin	0=not support 1=support	65H:64H	00	1b	E99FH
HW Hold# pin	0=not support 1=support		01	1b	
Deep Power Down Mode	0=not support 1=support		02	1b	
SW Reset	0=not support 1=support		03	1b	
SW Reset Opcode	Should be issue Reset Enable(66H)before Reset cmd.		11:04	99H	
Program Suspend/Resume	0=not support 1=support		12	0b	
Erase Suspend/Resume	0=not support 1=support		13	1b	
Unused			14	1b	
Wrap-Around Read mode	0=not support 1=support		15	1b	
Wrap-Around Read mode Opcode		66H	23:16	77H	77H
Wrap-Around Read data length	08H:support 8B wrap-around read 16H:8B&16B 32H:8B&16B&32B 64H:8B&16B&32B&64B	67H	31:24	64H	64H
Individual block lock	0=not support 1=support	6BH:68H	00	0b	EBFCH
Individual block lock bit(Volatile/Nonvolatile)	0=Volatile 1=Nonvolatile		01	0b	
Individual block lock Opcode			09:02	FFH	
Individual block lock Volatile protect bit default protect status	0=protect 1=unprotect		10	0b	
Secured OTP	0=not support 1=support		11	1b	
Read Lock	0=not support 1=support		12	0b	
Permanent Lock	0=not support 1=support		13	1b	
Unused			15:14	11b	
Unused			31:16	FFFFH	FFFFH

7.4 Program and Erase Instructions

7.4.1 Page Program (02H)

The Page Program instruction is for programming the memory. A Write Enable instruction must previously have been executed to set the Write Enable Latch bit before sending the Page Program instruction.

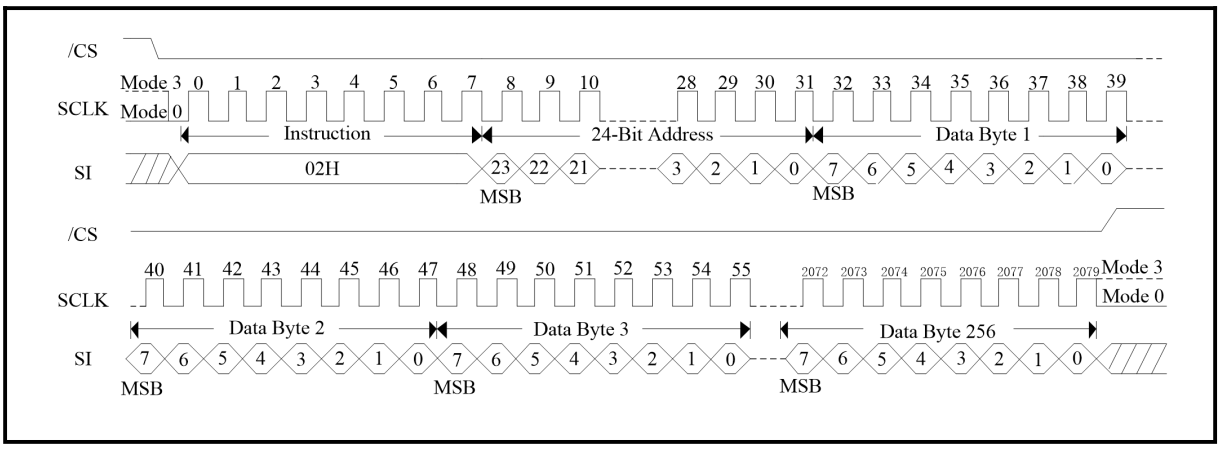
See ***Figure 35***, the Page Program instruction is entered by driving /CS Low, followed by the instruction code, 3-byte address and at least one data byte on SI. If the 8 least significant address bits (A7-A0) are not all zero, all transmitted data that goes beyond the end of the current page are programmed from the start address of the same page (from the address whose 8 least significant bits (A7-A0) are all zero). /CS must be driven low for the entire duration of the sequence. The Page Program instruction sequence: /CS goes low-> sending Page Program instruction ->3-byte address on SI ->at least 1 byte data on SI-> /CS goes high.

If more than 256 bytes are sent to the device, previously latched data are discarded and the last 256 data bytes are guaranteed to be programmed correctly within the same page. If less than 256 data bytes are sent to device, they are correctly programmed at the requested addresses without having any effects on the other bytes of the same page. /CS must be driven high after the eighth bit of the last data byte has been latched in; otherwise the Page Program instruction is not executed.

As soon as /CS is driven high, the self-timed Page Program cycle (whose duration is tPP) is initiated. While the Page Program cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Page Program cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch bit is reset.

A Page Program instruction applied to a page which is protected by the Block Protect (BP4, BP3, BP2, BP1, BP0) bits (see ***Table 6-Table 7***) are not executed.

Figure 35. Page Program Sequence Diagram



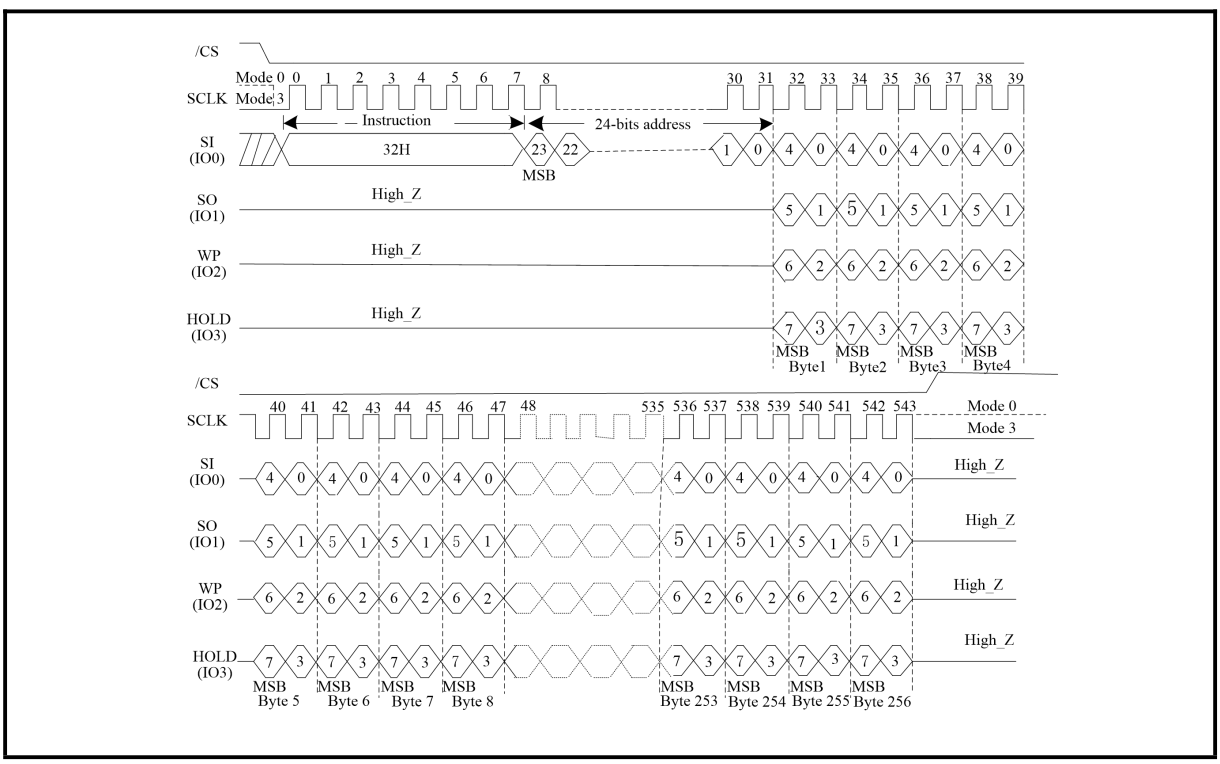
7.4.2 Quad Page Program (32H)

The Quad Page Program instruction is for programming the memory using for pins: IO0, IO1, IO2 and IO3. To use Quad Page Program the Quad enable in status register Bit9 must be set (QE=1). A Write Enable instruction must previously have been executed to set the Write Enable Latch bit before sending the Page Program instruction. The Quad Page Program instruction is entered by driving /CS Low, followed by the instruction code (32H), three address bytes and at least one data byte on IO pins. The Quad Enable bit (QE) of Status Register must be set to enable.

The instruction sequence is shown in ***Figure 36***. If more than 256 bytes are sent to the device, previously latched data are discarded and the last 256 data bytes are guaranteed to be programmed correctly within the same page. If less than 256 data bytes are sent to device, they are correctly programmed at the requested addresses without having any effects on the other bytes of the same page. /CS must be driven high after the eighth bit of the last data byte has been latched in; otherwise the Quad Page Program instruction is not executed.

As soon as /CS is driven high, the self-timed Quad Page Program cycle (whose duration is tPP) is initiated. While the Quad Page Program cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Quad Page Program cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch bit is reset. A Quad Page Program instruction applied to a page which is protected by the Block Protect (BP4, BP3, BP2, BP1, BP0) bits (see ***Table 6-Table 7***) is not executed

Figure 36. Quad Page Program Sequence Diagram

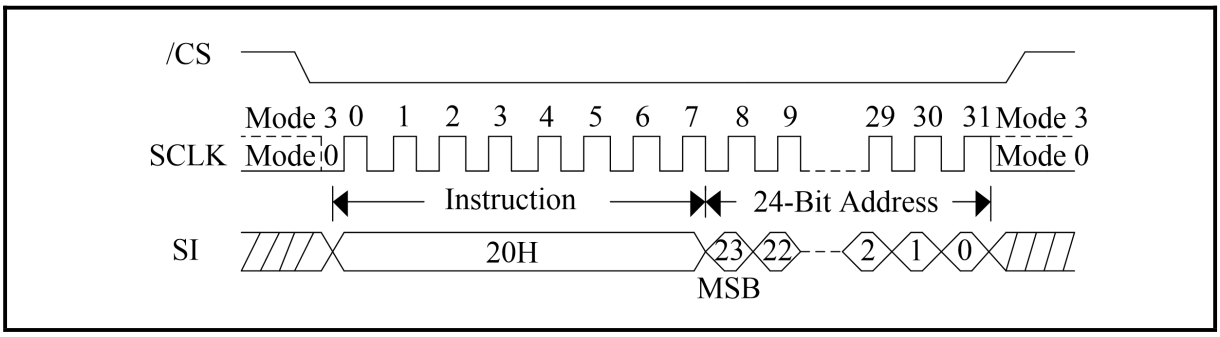


7.4.3 Sector Erase (20H)

The Sector Erase instruction is for erasing the all data of the chosen sector. A Write Enable instruction must previously have been executed to set the Write Enable Latch bit. The Sector Erase instruction is entered by driving /CS low, followed by the instruction code, and 3-address byte on SI. Any address inside the sector is a valid address for the Sector Erase instruction. /CS must be driven low for the entire duration of the sequence.

See ***Figure 37***, The Sector Erase instruction sequence: /CS goes low-> sending Sector Erase instruction-> 3-byte address on SI ->/CS goes high. /CS must be driven high after the eighth bit of the last address byte has been latched in; otherwise the Sector Erase instruction is not executed. As soon as /CS is driven high, the self-timed Sector Erase cycle (whose duration is tSE) is initiated. While the Sector Erase cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Sector Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch bit is reset. A Sector Erase instruction applied to a sector which is protected by the Block Protect (BP4, BP3, BP2, BP1, BP0) bits (see ***Table 6-Table 7***) is not executed.

Figure 37. Sector Erase Sequence Diagram

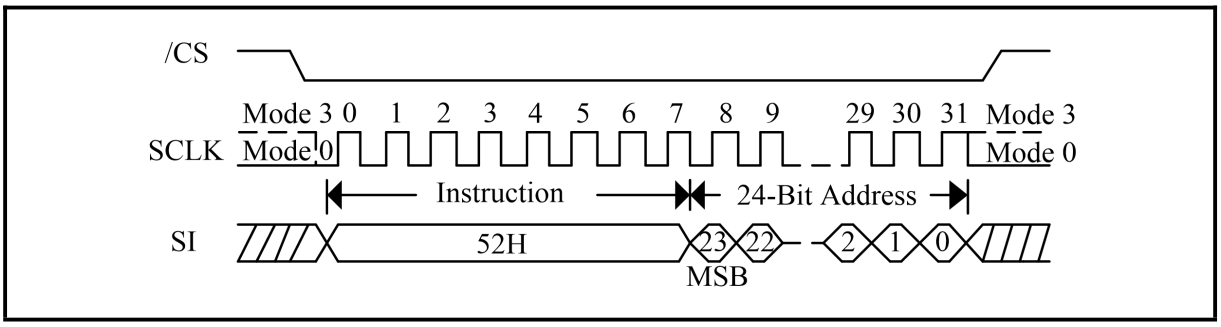


7.4.4 32KB Block Erase (52H)

The 32KB Block Erase instruction is for erasing the all data of the chosen block. A Write Enable instruction must previously have been executed to set the Write Enable Latch bit. The 32KB Block Erase instruction is entered by driving /CS low, followed by the instruction code, and 3-byte address on SI. Any address inside the block is a valid address for the 32KB Block Erase instruction. /CS must be driven low for the entire duration of the sequence.

See ***Figure 38***, the 32KB Block Erase instruction sequence: /CS goes low ->sending 32KB Block Erase instruction ->3-byte address on SI ->/CS goes high. /CS must be driven high after the eighth bit of the last address byte has been latched in; otherwise the 32KB Block Erase instruction is not executed. As soon as /CS is driven high, the self-timed Block Erase cycle (whose duration is tBE) is initiated. While the Block Erase cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Block Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch bit is reset. A 32KB Block Erase instruction applied to a block which is protected by the Block Protect (BP4, BP3, BP2, BP1, BP0) bits (see ***Table 6-Table 7***) is not executed.

Figure 38. 32KB Block Erase Sequence Diagram

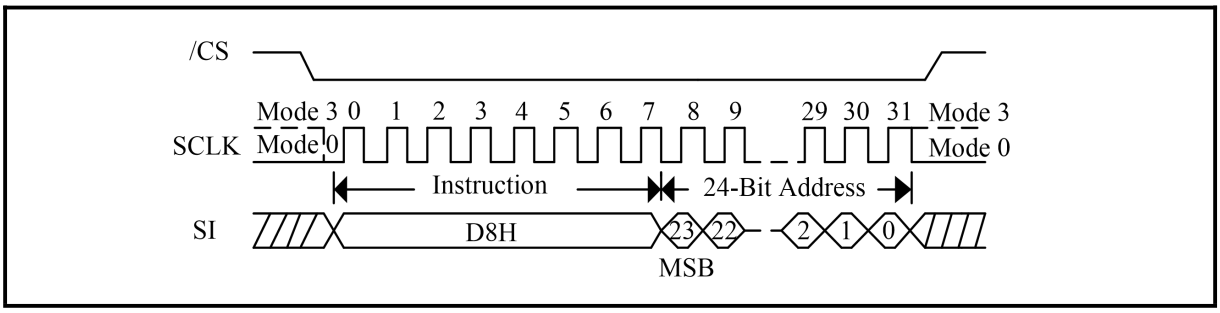


7.4.5 64KB Block Erase (D8H)

The 64KB Block Erase instruction is for erasing the all data of the chosen block. A Write Enable instruction must previously have been executed to set the Write Enable Latch bit. The 64KB Block Erase instruction is entered by driving /CS low, followed by the instruction code, and 3-byte address on SI. Any address inside the block is a valid address for the 64KB Block Erase instruction. /CS must be driven low for the entire duration of the sequence.

See ***Figure 39***, the 64KB Block Erase instruction sequence: /CS goes low sending 64KB Block Erase instruction 3-byte address on SI /CS goes high. /CS must be driven high after the eighth bit of the last address byte has been latched in; otherwise the 64KB Block Erase instruction is not executed. As soon as /CS is driven high, the self-timed Block Erase cycle (whose duration is tBE) is initiated. While the Block Erase cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Block Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch bit is reset. A 64KB Block Erase instruction applied to a block which is protected by the Block Protect (BP4, BP3, BP2, BP1, BP0) bits (see ***Table 6-Table 7***) is not executed.

Figure 39. 64KB Block Erase Sequence Diagram



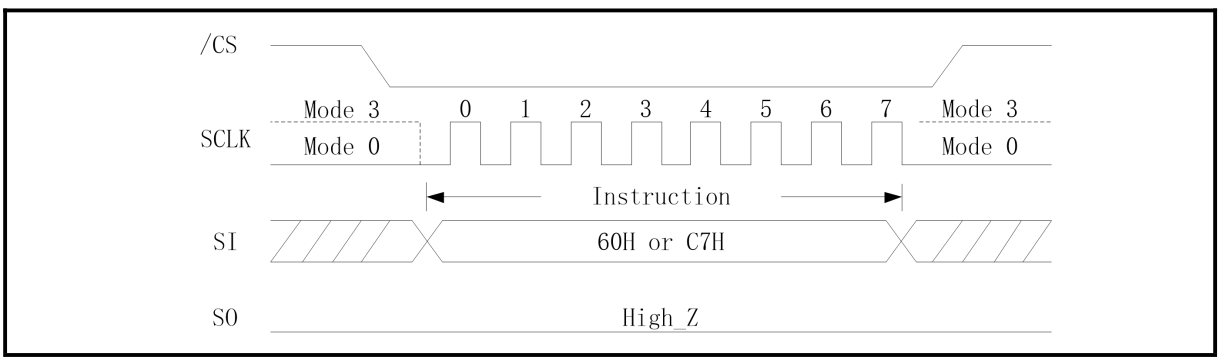
7.4.6 Chip Erase (60/C7H)

The Chip Erase instruction sets all memory within the device to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Chip Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the /CS pin low and shifting the instruction code “C7h” or “60h”. The Chip Erase instruction sequence is shown in ***Figure 40***.

The /CS pin must be driven high after the eighth bit has been latched. If this is not done the Chip Erase instruction will not be executed. After /CS is driven high, the self-timed Chip Erase instruction will commence for a time duration of tCE. While the Chip Erase cycle is in progress, the Read Status Register instruction may still be accessed to check the status of the WIP bit.

The WIP bit is a 1 during the Chip Erase cycle and becomes a 0 when finished and the device is ready to accept other Instructions again. After the Chip Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Chip Erase instruction is executed only if all Block Protect (BP2, BP1, and BP0) bits are 0.The Chip Erase instruction is ignored if one or more sectors are protected.

Figure 40. Chip Erase Sequence Diagram



7.4.7 Erase Suspend (75H)

The Erase Suspend instruction “75h” allows the system to interrupt a Sector/32K/64K Block Erase operation (The time between the Erase instruction and the Erase Suspend instruction is tES). After the erase operation has entered the suspended state, the memory array can be read or programed except for the Sector/32KB Block/64KB Block being erased. Write status register operation can't be suspended. The Program/Erase Suspend instruction sequence is shown in ***Figure 41***.

Table 11. Readable or Programmable Area of Memory While an Erase Operation is Suspended

Suspended operation	Readable Region or Programmable Of Memory Array
Sector Erase(4KB)	All but the Sector being Erased
Block Erase(32KB)	All but the 32KB Block being Erased
Block Erase(64KB)	All but the 64KB Block being Erased

When the Serial NOR Flash receives the Suspend instruction, there is a latency of tESL before the Write Enable Latch (WEL) bit clears to “0” and the SUS sets to “1”, after which the device is ready to accept one of the instructions listed in "Table Acceptable Instructions During Erase Suspend after tESL" (e.g. FAST READ). Refer to " AC Characteristics" for tESL timings. "Table Acceptable instructions During Suspend (tESL not required)" lists the Instructions for which the tESL latencies do not apply. For example, “05h”, “66h” and “99h” can be issued at any time after the Suspend instruction.

Status Register bit 15 (SUS) can be read to check the suspend status. The SUS (Erase Suspend Bit) sets to “1” when an erase operation is suspended. The SUS clears to “0” when the erase instruction is resumed.

Table 12. Acceptable instructions During Erase Suspend after tESL

Instruction Name	Instruction code	Erase Suspend
Write Enable	06h	*
Write Disable	04h	*
Read Data	03h	*
Fast Read	0Bh	*
Dual Output Fast Read	3Bh	*
Quad Output Fast Read	6Bh	*
Dual I/O Fast Read	BBh	*
Quad I/O Fast Read	EBh	*
Quad I/O Word Fast Read	E7h	*
Set Burst with Wrap	77h	*
Read Mftr./Device ID	90h	*
Dual IO Read Mftr./Device ID	92h	*
Quad IO Read Mftr./Device ID	94h	*
Read JEDEC ID	9Fh	*
Read Unique ID Number	4Bh	*
Release Powen-down/Device ID	ABh	*
Read Securty Registers	48h	*
Read SFDP	5Ah	*
Page Program	02h	*
Quad Page Program	32h	*

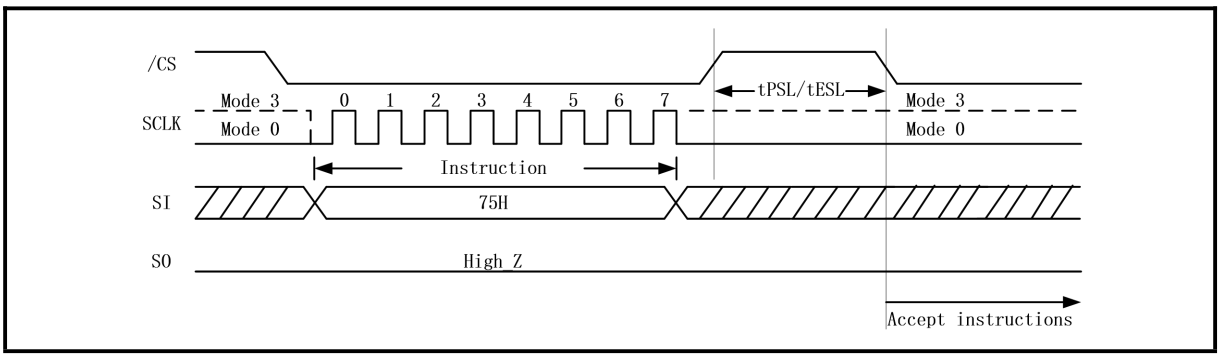
Instruction Name	Instruction code	Erase Suspend
Program/Erase Resume	7Ah	*

Table 13. Acceptable Instructions During Suspend（tESL not required）

Instruction Name	Instruction code	Erase Suspend
Read Status Register-1	05H	*
Read Status Register-2	35H	*
Read Status Register-3	15H	*
Enable Reset	66H	*
Reset Device	99H	*

tESL: Erase Suspend Latency.

Figure 41. Erase Suspend Instruction Sequence

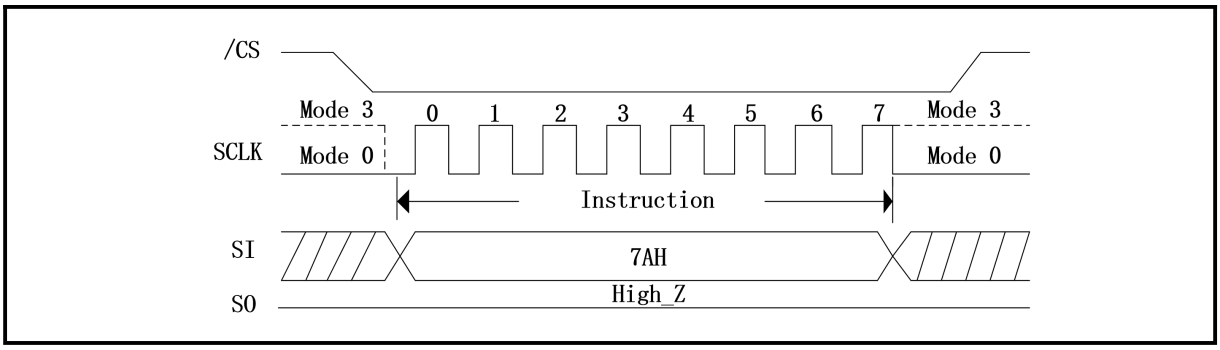


7.4.8 Erase Resume (7AH)

The Erase Resume instruction “7Ah” must be written to resume the Sector or Block Erase operation after an Erase Suspend. The Resume instruction “7AH” will be accepted by the device only if the SUS bit in the Status Register equals to 1 and the WIP bit equals to 0.

After the Resume instruction is issued the SUS bit will be cleared from 1 to 0 immediately, the WIP bit will be set from 0 to 1 within 200 ns and the Sector or Block will complete the erase operation. If the SUS bit equals to 0 or the WIP bit equals to 1, the Resume instruction “7Ah” will be ignored by the device. The Erase Resume instruction sequence is shown in ***Figure 42***.

Figure 42. Erase Resume Instruction Sequence



8. Electrical Characteristics

8.1 Absolute Maximum Ratings

Parameter	Symbol	Conditions	Range	Unit.
Supply Voltage	VCC		–0.5 to 4	V
Voltage Applied to Any Pin	VIO	Relative to Ground	–0.5 to 4	V
Transient Voltage on any Pin	VIOT	<20nS Transient Relative to Ground	–2.0V to VCC+2.0V	V
Storage Temperature	TSTG		–65 to +150	°C
Electrostatic Discharge Voltage	VESD	Human Body Model(1)	–2000 to +2000	V

Notes:

1.JEDEC Std JESD22-A114 (C1=100pF, R1=1500 ohms, R2=500 ohms)

8.2 Operating Ranges

Parameter	Symbol	Conditions	Spec		Unit.
			Min	Max	
Supply Voltage	VCC		2.7	3.6	V
Temperature Operating	TA	Commercial	-40	+85	°C
		Industrial	-40	+85	

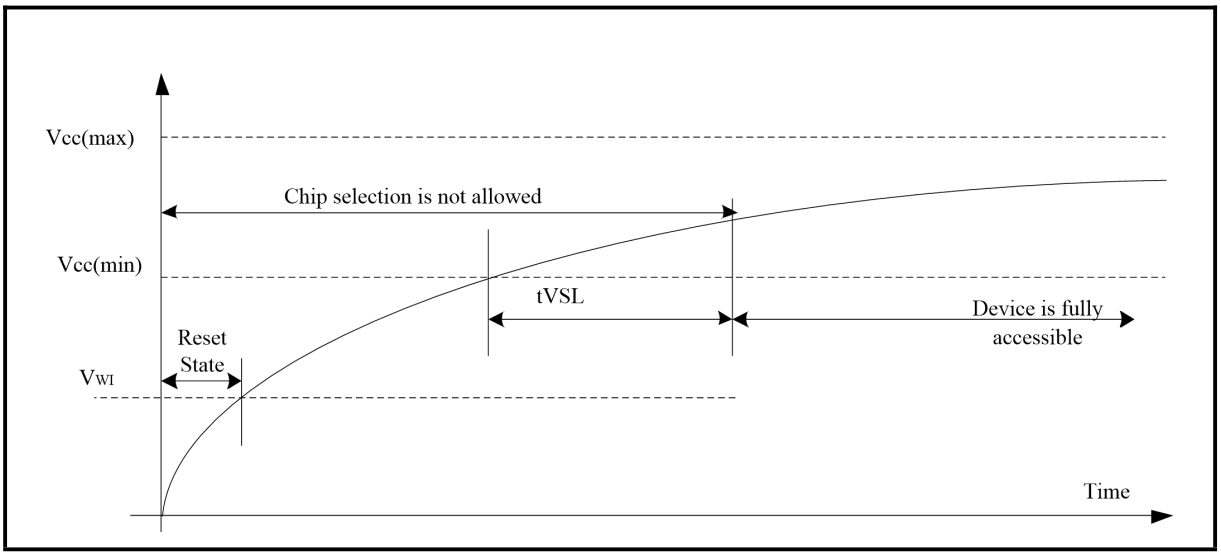
8.3 Latch Up Characteristics

Parameter	Min	Max
Input Voltage Respect To VSS On I/O Pins	-1.0V	VCC+1.0V
VCC Current	-100mA	100mA

8.4 Power-up Timing

Symbol	Parameter	Min	Max	Unit.
tVSL	VCC(min) To /CS Low	1		ms
V_{WI}	Write Inhibit Threshold Voltage V_{WI}	1.9	2.3	V

Figure 43. Power-up Timing and Voltage Levels



8.5 DC Electrical Characteristics

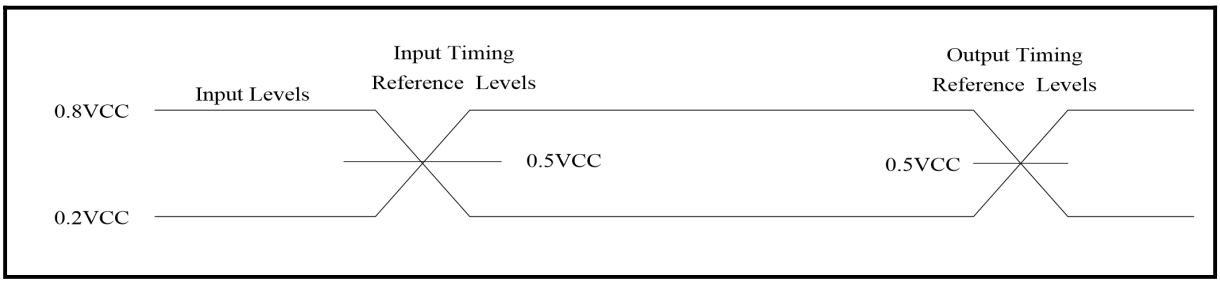
(T= -40℃~85℃, VCC=2.7~3.6V)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
ILI	Input Leakage Current				±2	μA
ILO	Output Leakage Current				±2	μA
ICC1	Standby Current	/CS=VCC, VIN=VCC or VSS		14	25	μA
ICC2	Deep Power-Down Current	/CS=VCC, VIN=VCC or VSS		0.6	2	μA
ICC3	Operating Current: (Read)	SCLK=0.1VCC/ 0.9VCC, at 120MHz,Q=Open(*1,*,2*4 I/O)		8	15	mA
		SCLK=0.1VCC/ 0.9VCC, at 80MHz,Q=Open(*1,*,2*4 I/O)		6	10	mA
ICC4	Operating Current(Page Program)	/CS=VCC			8	mA
ICC5	Operating Current(WRSR)	/CS=VCC			8	mA
ICC6	Operating Current(Sector Erase)	/CS=VCC			10	mA
ICC7	Operating Current(Block Erase)	/CS=VCC			10	mA
ICC8	Operating Current (Chip Erase)	/CS=VCC			10	mA
VIL	Input Low Voltage		-0.5		0.2VCC	V
VIH	Input High Voltage		0.8VCC		VCC+0.4	V
VOL	Output Low Voltage	IOL =100μA			0.4	V
VOH	Output High Voltage	IOH =-100μA	VCC-0.2			V

8.6 AC Measurement Conditions

Symbol	Parameter	Min	Tpy.	Max	Unit.	Conditions
CL	Load Capacitance			30	pF	
TR, TF	Input Rise And Fall time			5	ns	
VIN	Input Pause Voltage	0.2VCC to 0.8VCC			V	
IN	Input Timing Reference Voltage	0.5VCC			V	
OUT	Output Timing Reference Voltage	0.5VCC			V	

Figure 44. AC Measurement I/O Waveform



8.7 AC Electrical Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit.
Fc	Clock frequency for all instructions, except Read Data instruction (03H), on 3.0 - 3.6V power supply	DC.		120	MHz
Fc	Clock frequency for all instructions, except Read Data instruction (03H), on 2.7-2.9V power supply	DC.		108(4)	MHz
fR	Clock freq. for Read Data instruction (03H)	DC.		100	MHz
tCLH	Serial Clock High Time	4.5			ns
tCLL	Serial Clock Low Time	4.5			ns
tCLCH	Serial Clock Rise Time (Slew Rate)	0.1(1)			V/ns
tCHCL	Serial Clock Fall Time (Slew Rate)	0.1(1)			V/ns
tSLCH	/CS Active Setup Time	5			ns
tCHSH	/CS Active Hold Time	5			ns
tSHCH	/CS Not Active Setup Time	5			ns
tCHSL	/CS Not Active Hold Time	5			ns

Symbol	Parameter	Min.	Typ.	Max.	Unit.
tSHSL	/CS High Time（read/write）	20			ns
tSHQZ	Output Disable Time			6	ns
tCLQX	Output Hold Time	0			ns
tDVCH	Data In Setup Time	3			ns
tCHDX	Data In Hold Time	2			ns
tHLCH	/Hold Low Setup Time (relative to Clock)	5			ns
tHHCH	/Hold High Setup Time (relative to Clock)	5			ns
tCHHL	/Hold High Hold Time (relative to Clock)	5			ns
tCHHH	/Hold Low Hold Time (relative to Clock)	5			ns
tHLQZ	/Hold Low To High-Z Output			6	ns
tHHQX	/Hold Low To Low-Z Output			6	ns
tCLQV	Clock Low To Output Valid			7.5(3)	ns
tWHSL	Write Protect Setup Time Before /CS Low	20			ns
tSHWL	Write Protect Hold Time After /CS High	100			ns
tDP	/CS High To Deep Power-Down Mode			20	μs
tRES1	/CS High To Standby Mode Without Electronic Signature Read			66	μs
tRES2	/CS High To Standby Mode With Electronic Signature Read			66	μs
tESL	Erase Suspend Latency			30	μs
tES	Latency between Erase and next Suspend	20			μs
tERS	Latency between Erase Resume and next Suspend	20			μs
tRST	/CS High To Next Instruction After Reset			1	ms
tW	Write Status Register Cycle Time		5	30(2)	ms
tBP1	Byte Program Time (First Byte) (2)		110	120	μs
tBP2	Additional Byte Program Time (After First Byte) (2)		3.5	9	μs
tPP	Page Programming Time		0.9	2.4	ms
tSE	Sector Erase Time		70	300	ms
tBE	Block Erase Time(32K Bytes/64K Bytes)		0.25/0.4	1.6/2	S
tCE	Chip Erase Time		100	150	S

Notes:
1. Tested with clock frequency lower than 50 MHz.
2. For multiple bytes after first byte within a page, tBPn = tBP1 + tBP2 * N, where N is the number of bytes programmed.
3. tCLQV for command 9Fh/90h read ID and read SR will be 9.5nS
4. Read frequency for dual out read (3BH) and quad out read (6BH) should be 90MHz

Figure 45. Serial input Timing

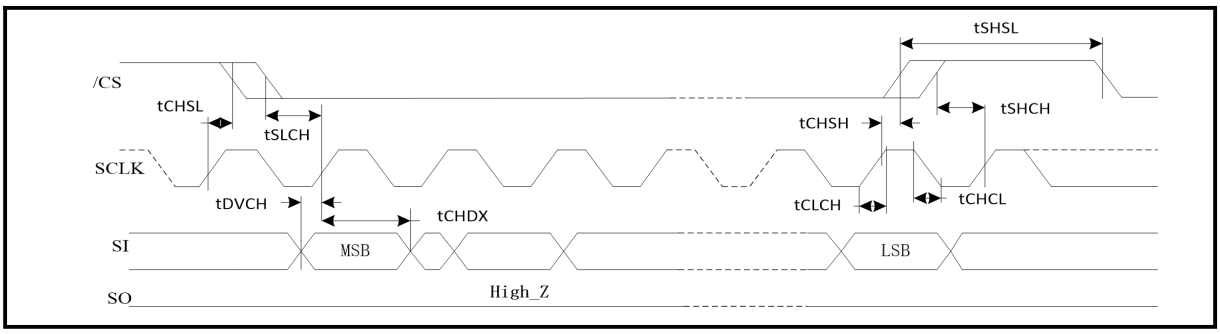


Figure 46. Output Timing

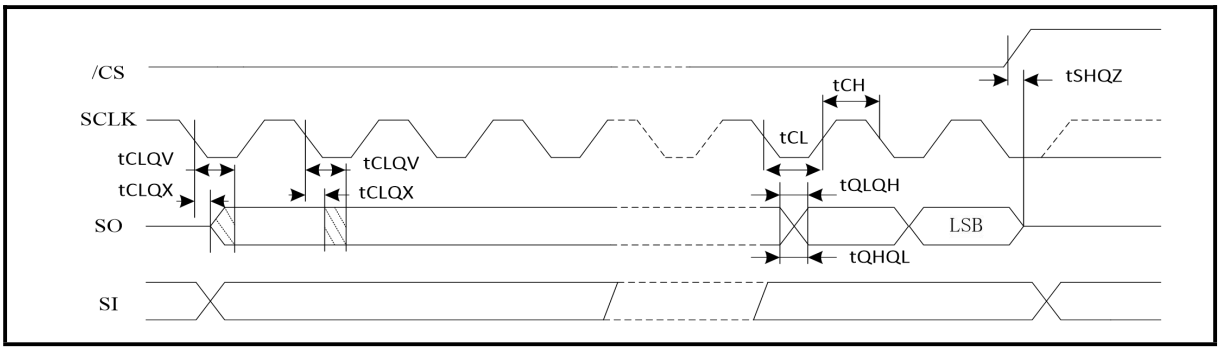


Figure 47. Hold Timing

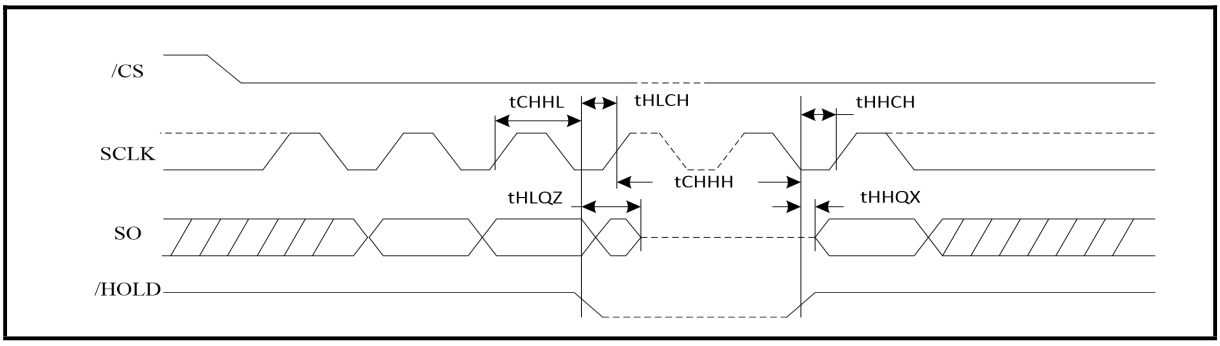
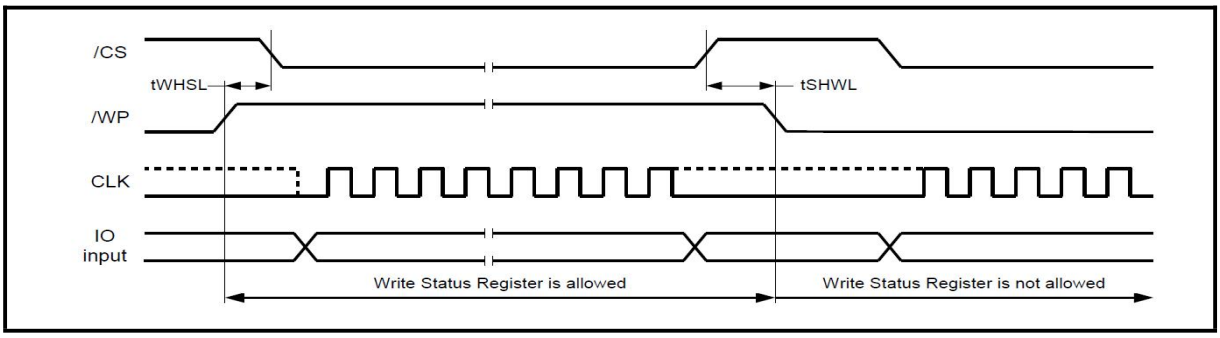
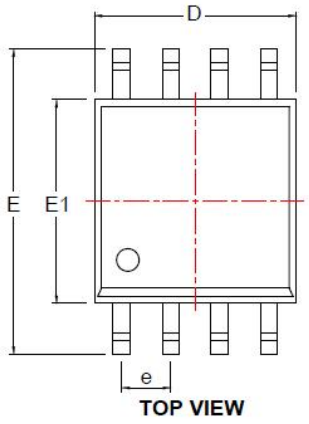


Figure 48. /WP Timing

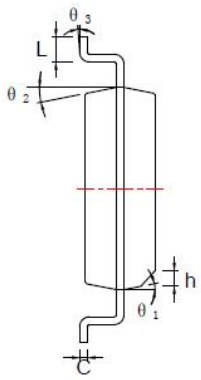


9. Package Information

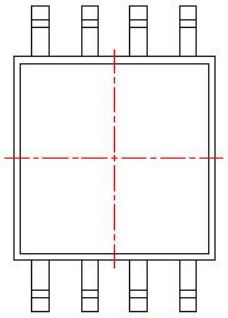
9.1 Package 8-Pin SOP 208-mil



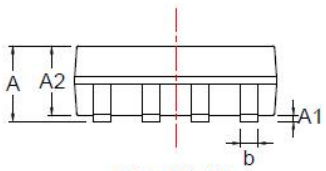
TOP VIEW



SIDE VIEW



BTM VIEW



SIDE VIEW

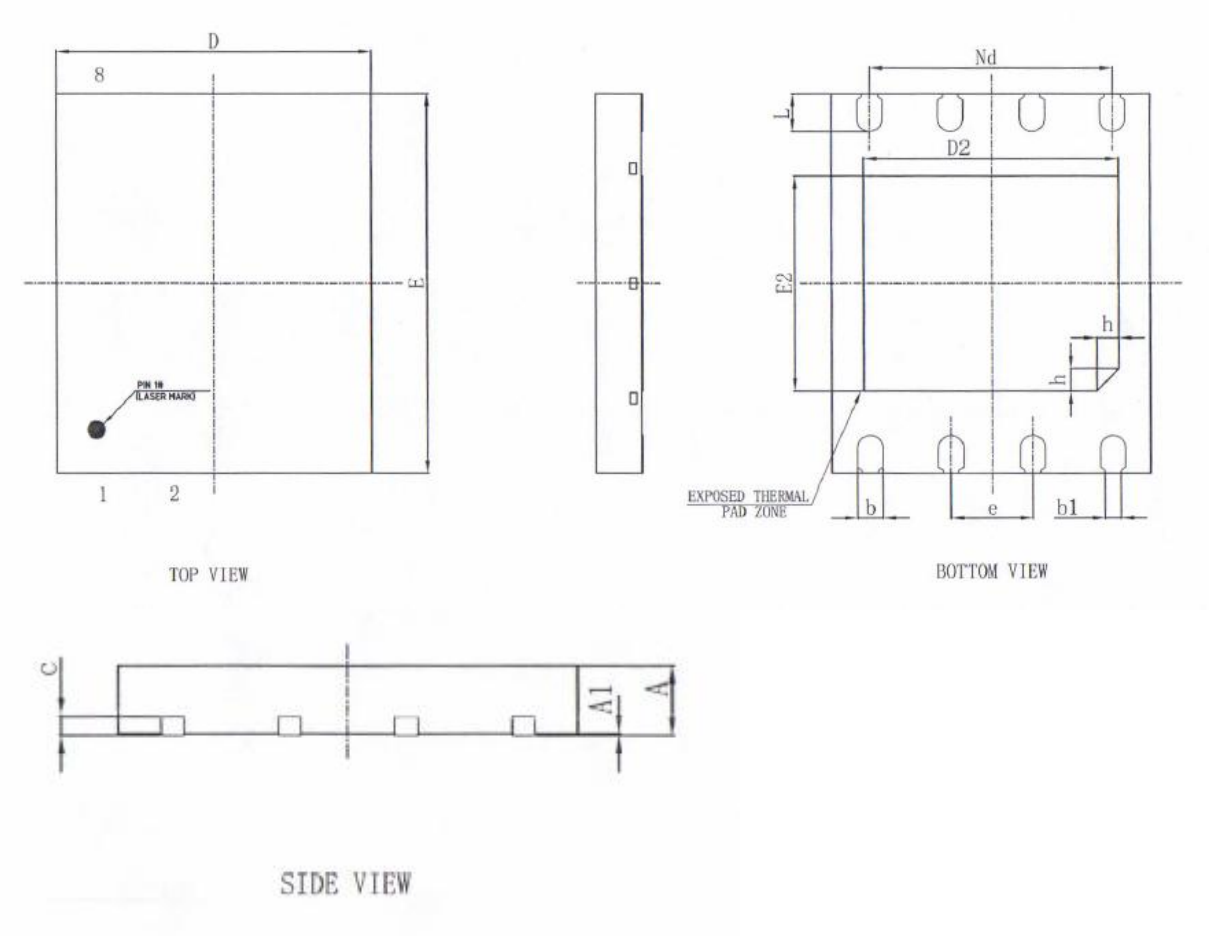
DIMENSIONS IN MUILLIMETERS

SYMBOL	MIN	NOM	MAX
A	1.75	1.95	2.15
A_1	0.05	0.15	0.25
A_2	1.70	1.80	1.90
b	0.40	0.45	0.50
c	0.19	0.20	0.21
D	5.13	5.23	5.33
E	7.70	7.90	8.10
E_1	5.10	5.25	5.40
e	1.17	1.27	1.37
L	0.50	0.65	0.80
h	0.30	0.40	0.50
θ_1	••••	——	••••
θ_2	••••••	——	••••••
θ_3	••••••	——	••••••

Note:

1、 The exposed metal pad area on the bottom of the package is floating.

9.2 Package 8-Pad WSON (5x6mm)



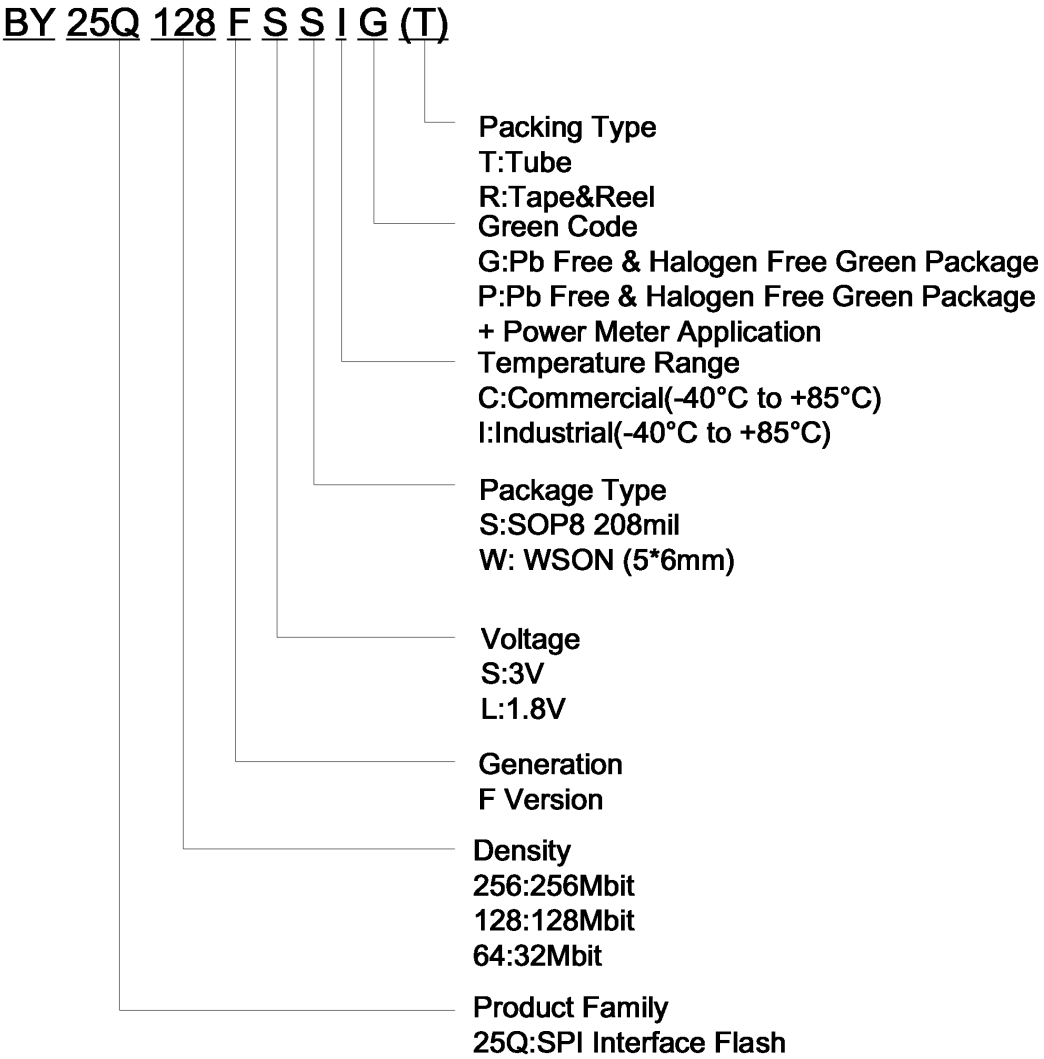
Dimensions

Symbol / Unit		A	A1	b	b1	c	D	Nd	e	E	D2	E2	L	h
mm	Min	0.70	0	0.35	0.25REF	0.18	4.90	3.81BSC	1.27BSC	5.90	3.90	3.30	0.55	0.30
	Nom	0.75	0.02	0.40		0.203	5.00			6.00	4.00	3.40	0.60	0.35
	Max	0.80	0.05	0.45		0.25	5.10			6.10	4.10	3.50	0.65	0.40

Note:

1、 The exposed metal pad area on the bottom of the package is floating.

10. Order Information



10.1 Valid part Numbers and Top Side Marking

The following table provides the valid part numbers for BY25Q128FS SPI Flash Memory. Pls contact BY Technology for specific availability by density and package type.

For consumer and industry application:

Package Type	Density	Product Number	Top Side Marking
S SOP8 208mil	128M-bit	BY25Q128FSSIG	BoyaMicro 25Q128FSSIG YYWW
W WSON8 6*5mm	128M-bit	BY25Q128FSWIG	Boya 25Q128FSWIG YYWW

For Power Meter application:

Package Type	Density	Product Number	Top Side Marking
S SOP8 208mil	128M-bit	BY25Q128FSSIP	BoyaMicro 25Q128FSSIP YYWW
W WSON8 6*5mm	128M-bit	BY25Q128FSWIP	Boya 25Q128FSWIP YYWW

10.2 Minimum Packing Quantity (MPQ)

Package Type	Packing Type	Qty for 1 Tube or Reel	Vacuum bag/ Inner Box	MPQ
SOP8 208mil	Tube	95ea/Tube	100Tubes/Bag 1Bag/InnerBox	9,500
	Tape&Reel (13inch, 16mm)	2000ea/Reel	1Reel/Bag 2Bags/InnerBox	4,000
WSON8 5*6mm	Tape&Reel (13inch)	3000ea/Reel	1Reel/Bag 1Bag/InnerBox	3,000

11. Document Change History

REVISION	CHANGE DESCRIPTION	CLAUSE	ORIGINATOR DATE
1.0	Initiate; Base on BY25Q128FS_v1.0;	/	Zuohuan Yu 2021-09-27
1.1	Add SOP8-208mil and DFN8 5*6 package information	/	Zuohuan Yu 2022-9-27
1.2	Update DC/AC spec	/	Zuohuan Yu 2022-10-27
1.3	1, Update DRV[1:0] default value to 01b (50%) 2, Add SFDP table	/	Zuohuan Yu 2022-11-1
1.4	1， Update DRV[1:0] default value to 10b (75%) 2， Update read frequency and erase time	/	Zuohuan Yu 2022-11-21
1.5	Update frequency	/	Zuohuan Yu 2022-12-14
1.6	Update tRES1/tRES2	/	Zuohuan Yu 2023-01-18
1.7	Update Commercial Temperature Range	/	Zuohuan Yu 2023-02-10
1.8	Update the logo and abbreviation	/	Zuohuan Yu 2023-04-04
1.9	Add the note of the DFN package	/	Zuohuan Yu 2023-07-20
2.0	Update suspend command description	/	Xingyue Huang 2024-6-4