DATASHEET

FOR

32M BIT SPI NOR FLASH

BY25FQ32ES

(Preliminary Datasheet)

Features

- **Serial Peripheral Interface**
  - Standard SPI: SCLK, /CS, SI, SO, /WP, /HOLD
  - Dual SPI: SCLK, /CS, IO0, IO1, /WP, /HOLD
  - Quad SPI: SCLK, /CS, IO0, IO1, IO2, IO3
  - QPI: SCLK, /CS, IO0, IO1, IO2, IO3
  - DTR (Double Transfer Rate) Read
- **Read**
  - Normal Read (Serial): 88MHz clock rate
  - Fast Read (Serial): 133MHz clock rate with 30PF load
  - Dual I/O data transfer up to 266Mbits/S with DQS
  - Quad I/O data transfer up to 664Mbits/S with DQS
  - QPI data transfer up to 664Mbits/S with DQS
  - DTR Quad I/O Data transfer up to1064Mbits/s with DQS
  - Allows XIP (execute in place) Operation: Continuous Read with 8/16/32/64-byte Wrap
  - Support for Data Strobe function (DQS Pin)
- **Program**
  - Serial-input Page Program up to 256bytes
  - Program Suspend and Resume
- **Erase**
  - Block Erase (64/32 KB)
  - Sector Erase (4 KB)
  - Chip Erase
  - Erase Suspend and Resume
- **Program/Erase Speed**
  - Page Program time: 0.16ms typical
  - Sector Erase time: 25ms typical
  - Block Erase time: 0.06/0.12s typical
  - Chip Erase time: 8s typical
- **Flexible Architecture**
  - Sector of 4K-byte
  - Block of 32/64K-byte
- **Low Power Consumption**
  - 9μA typical stand-by current
  - 1μA typical power-down current
- **Software/Hardware Write Protection**
  - 3x1024-Byte Security Registers with OTP Locks
  - Discoverable Parameters (SFDP) register
  - Enable/Disable protection with WP Pin
  - Write protect all/portion of memory via software
  - Top or Bottom, Sector or Block selection
- **Single Supply Voltage**
  - Full voltage range: 2.7~3.6V
- **Temperature Range**
  - Industrial (-40℃ to +85℃)
- **Cycling Endurance/Data Retention**
  - Typical 100k Program-Erase cycles on any sector
  - Typical 20-year data retention

CONTENTS

1. DESCRIPTION 6
2. SIGNAL DESCRIPTION 9
2.1 Input/Output Summary 9
2.2 Chip Select (/CS) 9
2.3 Serial Clock (SCLK) 9
2.4 Serial Input (SI)/IO0 10
2.5 Serial Data Output (SO)/IO1 10
2.6 Write Protect (/WP)/IO2 10
2.7 HOLD (/HOLD) /RESET /IO3 10
2.8 VCC Power Supply 10
2.9 VSS Ground 10
2.10 Data Strobe Signal (DQS) 11
3. BLOCK/SECTOR ADDRESSES 12
4. SPI OPERATION 13
4.1 Standard SPI Instructions 13
4.2 Dual SPI Instructions 13
4.3 Quad SPI Instructions 13
4.4 QPI Instructions 13
4.5 DTR Instructions 13
4.6 Switch between SPI and QPI operation 14
5. OPERATION FEATURES 15
5.1 Supply Voltage 15
5.1.1 Operating Supply Voltage 15
5.1.2 Power-up Conditions 15
5.1.3 Device Reset 15
5.1.4 Power-down 15
5.2 Active Power and Standby Power Modes 15
5.3 Hold Condition 15
5.4 Software Reset & Hardware RESET 16
5.4.1 Software Reset 16
5.4.2 Hardware Reset (/HOLD pin) 16
5.4.3 Hardware Reset (JEDEC Standard Hardware Reset) 17
5.5 Data Strobe Function 18
5.6 Write Protect Features 18
5.7 Status Register 19
5.7.1 Status Register Table 19
5.7.2 The Status and Control Bits 20
5.8 Array Memory Protection 23
5.8.1 Block Protect Table 23
6. DEVICE IDENTIFICATION 25
7. INSTRUCTIONS DESCRIPTION 26
7.1 Configuration and Status Instructions 32
7.1.1 Write Enable (06H) 32
7.1.2 Write Enable for Volatile Status Register (50H) 33
7.1.3 Write Disable (04H) 34
7.1.4 Read Status Register (05H or 35H or 15H) 35

7.1.5 Write Status Register (01H or 31H or 11H) 36
7.1.6 Enter QPI Mode (38H) 38
7.1.7 Exit QPI Mode (FFH) 38
7.1.8 Enable Reset (66H) and Reset Device (99H) 39
7.2 Read Instructions 40
7.2.1 Read Data (03H) 40
7.2.2 Fast Read (0BH) 41
7.2.3 DTR Fast Read (0DH) 42
7.2.4 Dual Output Fast Read (3BH) 43
7.2.5 Quad Output Fast Read (6BH) 44
7.2.6 Dual I/O Fast Read (BBH) 45
7.2.7 DTR Fast Read Dual I/O (BDH) 47
7.2.8 Quad I/O Fast Read (EBH) 49
7.2.9 DTR Fast Read Quad I/O(EDH) 52
7.2.10 Quad I/O Word Fast Read (E7H) 54
7.2.11 Set Burst with Wrap (77H) 56
7.2.12 Set Read Parameters (C0H) 57
7.2.13 Burst Read with Wrap (0CH) 59
7.2.14 DTR Burst Read with Wrap (0EH) 60
7.3 ID and Security Instructions 61
7.3.1 Read Manufacture ID/ Device ID (90H) 61
7.3.2 Dual I/O Read Manufacture ID/ Device ID (92H) 62
7.3.3 Quad I/O Read Manufacture ID/ Device ID (94H) 63
7.3.4 Read JEDEC ID (9FH) 64
7.3.5 Read Unique ID Number (4Bh) 65
7.3.6 Deep Power-Down (B9H) 66
7.3.7 Release from Deep Power-Down/Read Device ID (ABH) 67
7.3.8 Read Security Registers (48H) 69
7.3.9 Erase Security Registers (44H) 70
7.3.10 Program Security Registers (42H) 71
7.3.11 Read Serial Flash Discoverable Parameter (5AH) 72
7.4 Program and Erase Instructions 73
7.4.1 Page Program (02H) 73
7.4.2 Quad Page Program (32H) 75
7.4.3 Sector Erase (20H) 76
7.4.4 32KB Block Erase (52H) 77
7.4.5 64KB Block Erase (D8H) 78
7.4.6 Chip Erase (60/C7H) 79
7.4.7 Program/Erase Suspend (75H) 80
7.4.8 Program/Erase Resume (7AH) 83
8. ELECTRICAL CHARACTERISTICS 84
8.1 Absolute Maximum Ratings(1) 84
8.2 Operating Ranges 84
8.3 Latch Up Characteristics 85
8.4 Power-up and Power-Down Timing 85
8.5 DC Electrical Characteristics 86
8.6 AC Measurement Conditions 87
8.7 AC Electrical Characteristics 88
9. PACKAGE INFORMATION 92
9.1 Package 8-pad USON8 2*3mm(0.55mm) 92
9.2 Package 8-pad USON8 4*3mm 93
9.3 Package 8-pad USON8 4*4mm 94
9.4 Package 8-pad WSON8 5*6mm 95

9.5 Package 8-Pin SOP8 150mil 96
9.6 Package 8-Pin SOP8 208mil 97
9.7 Package 16-pin SOP16 300mil 98
9.8 Package TFBGA-24ball (5x5 Ball Array) 99
10. ORDER INFORMATION 100
10.1 Valid part Numbers and Top Side Marking 101
10.2 Minimum Packing Quantity (MPQ) 102
11. DOCUMENT CHANGE HISTORY 103

1. DESCRIPTION

The BY25FQ32ES is 32M-bit Serial Peripheral Interface(SPI) Flash memory, and support the standard Serial Peripheral Interface (SPI), Dual/Quad I/O SPI as well as 2-clocks instruction cycle Quad Peripheral Interface (QPI): Serial Clock, Chip Select, Serial Data I/O0 (DI), I/O1 (DO), I/O2 (/WP), and I/O3 (/HOLD). SPI clock frequencies of up to 133MHz are supported allowing equivalent clock rates of 266MHz (133MHz x 2) for Dual I/O and 664MHz (166MHzx4) for Quad I/O when using the Fast Read Dual/Quad and QPI instructions. The Double Transfer Rate (DTR) Read is transferred with speed of 1064Mbits/s. These transfer rates can outperform standard Asynchronous 8 and 16-bit Parallel Flash memories. The Continuous Read Mode allows for efficient memory access with as few as 8-clocks of instruction-overhead to read a 24-bit address, allowing true XIP (execute in place) operation. The device uses a single low voltage power supply, ranging from 2.7 Volt to 3.6 Volt.

Additionally, the device supports JEDEC standard manufacturer and device ID and three 1024bytes Security Registers.

In order to meet environmental requirements, BY Technology offers 8-pad USON8 2*3mm, 8-pad USON8 4*3mm,8-pad USON8 4*4mm, 8-pad WSON8 5*6mm, 8-pin SOP8 150mil,8-pin SOP8 208mil,16-pin SOP16 300mil, TFBGA-24ball (5x5 Ball Array), and other special order packages, please contacts BY Technology for ordering information.

Figure 1. Logic diagram

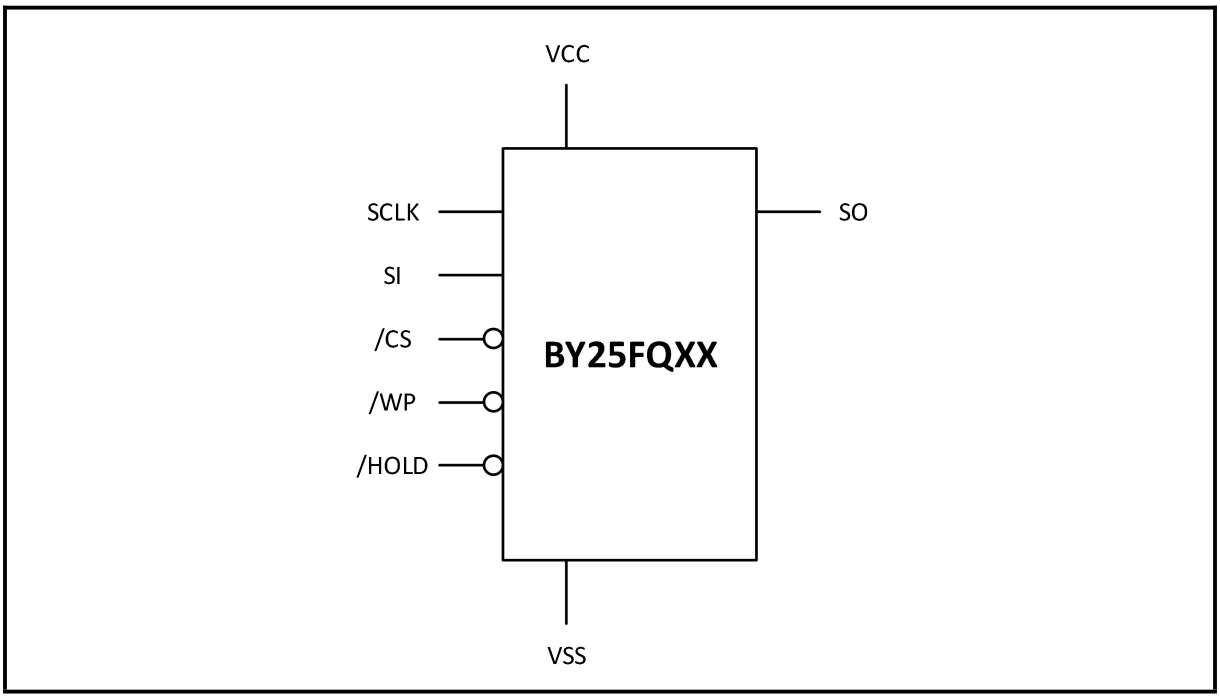


Figure 2. Pin Configuration SOP8 150/208mil

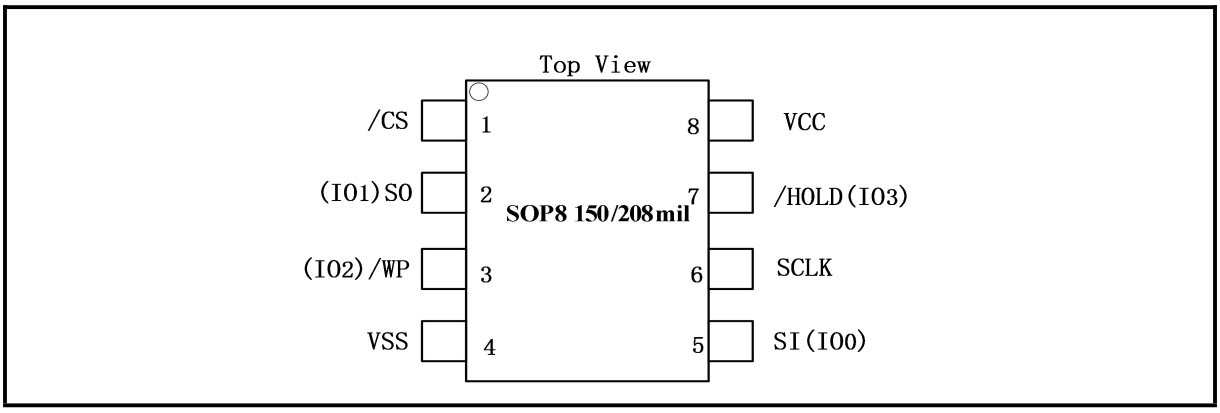


*Figure 3. Pin Configuration WSON8 5*6mm, USON8 4*4mm, USON8 4*3mm and USON8 2*3mm*

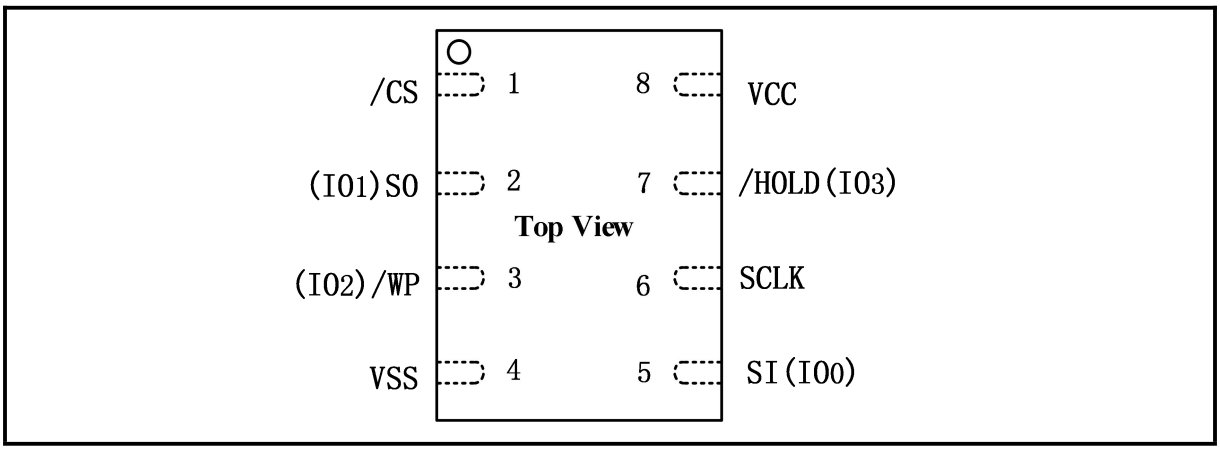


Figure 4. Pin Configuration SOP16 300mil

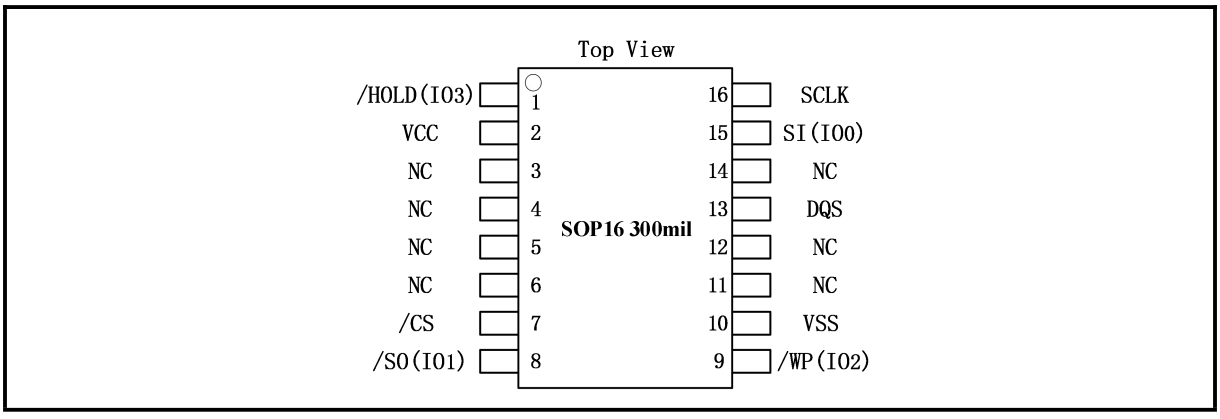
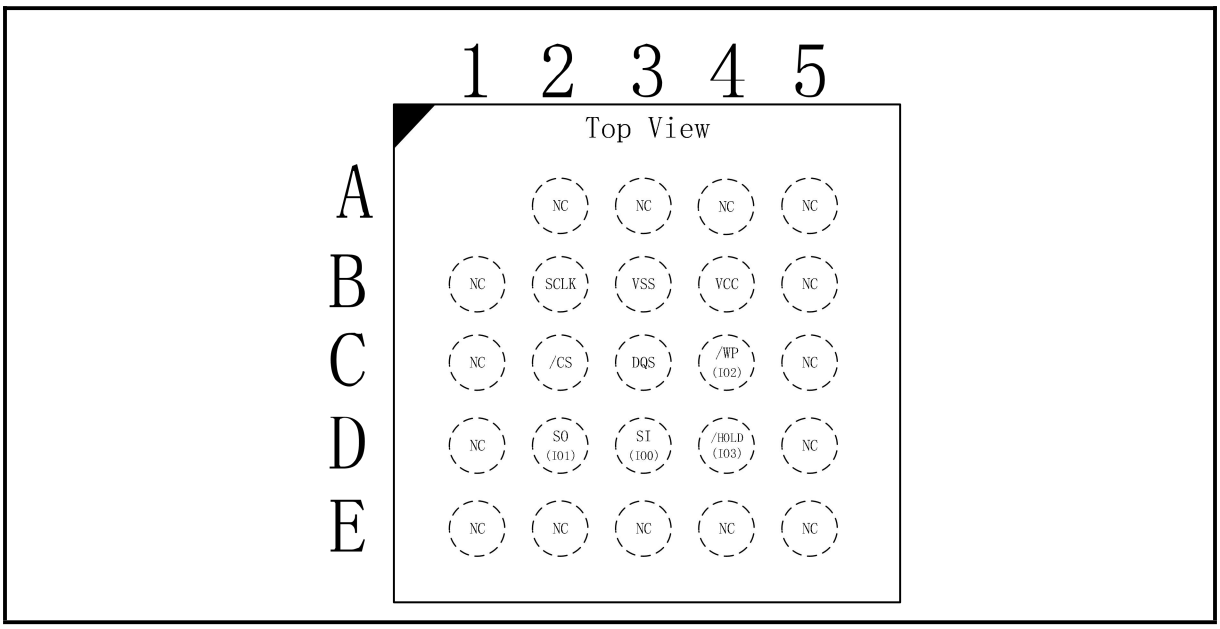


Figure 5. Pin Configuration TFBGA6*8mm-24Ball (5x5 ball array)



2. SIGNAL DESCRIPTION

During all operations, VCC must be held stable and within the specified valid range: VCC (min) to VCC (max).

All of the input and output signals must be held High or Low (according to voltages of VIH, VOH, VIL or VOL, see ***DC Electrical Characteristics***). These signals are described next.

2.1 Input/Output Summary

Table 1. Signal Names

Pin Name	I/O	Description
/CS	I	Chip Select
SO (IO1)	I/O	Serial Output for single bit data Instructions. IO1 for Dual or Quad Instructions
/WP (IO2)	I/O	Write Protect in single bit or Dual data Instructions. IO2 in Quad mode. The signal has an internal pull-up resistor and may be left unconnected in the host system if not used for Quad Instructions
VSS		Ground
SI (IO0)	I/O	Serial Input for single bit data Instructions. IO0 for Dual or Quad Instructions
SCLK	I	Serial Clock
/HOLD (IO3)	I/O	Hold (pause) serial transfer in single bit or Dual data Instructions. IO3 in Quad-I/O. The signal has an internal pull-up resistor and may be left unconnected in the host system if not used for Quad Instructions
VCC		Core and I/O Power Supply
DQS(1)	O	Data Strobe Signal Output

Notes:

1. The Data Strobe Signal (DQS) is used in 16-pin SOP 300mil、TFBGA6*8mm-24Ball (5x5 ball array) packages

2.2 Chip Select (/CS)

The chip select signal indicates when an instruction for the device is in process and the other signals are relevant for the memory device. When the /CS signal is at the logic high state, the device is not selected and all input signals are ignored and all output signals are high impedance. Unless an internal Program, Erase or Write Status Registers embedded operation is in progress, the device will be in the Standby Power mode. Driving the /CS input to logic low state enables the device, placing it in the Active Power mode. After Power Up, a falling edge on /CS is required prior to the start of any instruction.

2.3 Serial Clock (SCLK)

This input signal provides the synchronization reference for the SPI interface. Instructions, addresses, or data input are latched on the rising edge of the SCLK signal. Data output changes after the falling edge of SCLK.

2.4 Serial Input (SI)/IO0

This input signal is used to transfer data serially into the device. It receives instructions, addresses, and data to be programmed. Values are latched on the rising edge of serial SCLK clock signal.

SI becomes IO0 an input and output during Dual and Quad Instructions for receiving instructions, addresses, and data to be programmed (values latched on rising edge of serial SCLK clock signal) as well as shifting out data (on the falling edge of SCLK).

2.5 Serial Data Output (SO)/IO1

This output signal is used to transfer data serially out of the device. Data is shifted out on the falling edge of the serial SCLK clock signal.

SO becomes IO1 an input and output during Dual and Quad Instructions for receiving instructions, addresses, and data to be programmed (values latched on rising edge of serial SCLK clock signal) as well as shifting out data (on the falling edge of SCLK).

2.6 Write Protect (/WP)/IO2

When /WP is driven Low (VIL), while the Status Register Protect bits (SRP1 and SRP0) of the Status Registers (SR2[0] and SR1[7]) are set to 0 and 1 respectively, it is not possible to write to the Status Registers. This prevents any alteration of the Status Registers. As a consequence, all the data bytes in the memory area that are protected by the Block Protect, BP4, BP3 bits in the status registers, are also hardware protected against data modification while /WP remains Low. The /WP function is not available when the Quad mode is enabled (QE) in Status Register 2 (SR2[1]=1).

The /WP function is replaced by IO2 for input and output during Quad mode for receiving addresses, and data to be programmed (values are latched on rising edge of the SCLK signal) as well as shifting out data (on the falling edge of SCLK). /WP has an internal pull-up resistance; when unconnected; /WP is at VIH and may be left unconnected in the host system if not used for Quad mode.

2.7 HOLD (/HOLD) /RESET /IO3

The /HOLD function is only available when QE=0, which can be configured either as a /HOLD pin or as a /RESET pin depending on Status Register setting. If QE=1, the /HOLD function is disabled, the pin acts as dedicated data I/O pin, and the /HOLD or /RESET function is not available.

When QE=0 and HOLD/RST= 0, the /HOLD signal goes low to stop any serial communications with the device, but doesn't stop the operation of write status register, programming, or erasing in progress.

The operation of HOLD, need /CS keep low, and starts on falling edge of the /HOLD signal, with SCLK signal being low (if SCLK is not being low, HOLD operation will not start until SCLK being low). The HOLD condition ends on rising edge of /HOLD signal with SCLK being low (If SCLK is not being low, HOLD operation will not end until SCLK being low).

2.8 VCC Power Supply

VCC is the supply voltage. It is the single voltage used for all device functions including read, program, and erase.

2.9 VSS Ground

VSS is the reference for the VCC supply voltage.

2.10 Data Strobe Signal (DQS)

Data Strobe Signal Output. DQS is used in 16-pin SOP 300mil、TFBGA6*8mm-24Ball (5x5 ball array) packages.

3. BLOCK/SECTOR ADDRESSES

Table 2. Block/Sector Addresses of BY25FQ32ES

Memory Density	Block (64k byte)	Block (32k byte)	Sector No.	Sector Size(KB)	Address range
32Mbit	Block 0	Half block 0	Sector 0	4	000000h-000FFFh
			:	:	:
			Sector 7	4	007000h-007FFFh
		Half block 1	Sector 8	4	008000h-008FFFh
			:	4	:
			Sector 15	4	00F000h-00FFFFh
	:	:	:	:	:
	Block 15	Half block 30	Sector 240	4	0F0000h-0F0FFFh
			:	:	:
			Sector 247	4	0F7000h-0F7FFFh
		Half block 31	Sector 248	4	0F8000h-0F8FFFh
			:	:	:
			Sector 255	4	0FF000h-0FFFFFh
	:	:	:	:	:
	Block 56	Half block 112	Sector 888	4	378000h-378FFFh
			:	:	:
			Sector 895	4	37F000h-37FFFFh
		Half block 113	Sector 896	4	380000h-380FFFh
			:	:	:
			Sector 903	4	387000h-387FFFh
	:	:	:	:	:
	Block 63	Half block 126	Sector 1008	4	3F0000h-3F0FFFh
			:	:	:
			Sector 1015	4	3F7000h-3F7FFFh
		Half block 127	Sector 1016	4	3F8000h-3F8FFFh
			:	:	:
			Sector 1023	4	3FF000h-3FFFFFh

Notes:

2. Big Block = Uniform Big Block, and the size is 16M bits.
3. Block = Uniform Block, and the size is 64K bytes.
4. Half block = Half Uniform Block, and the size is 32k bytes.
5. Sector = Uniform Sector, and the size is 4K bytes.

4. SPI OPERATION

4.1 Standard SPI Instructions

The BY25FQ32ES features a serial peripheral interface on 4 signals bus: Serial Clock (SCLK), Chip Select (/CS), Serial Data Input (SI) and Serial Data Output (SO). Both SPI bus mode 0 and 3 are supported. Input data is latched on the rising edge of SCLK and data shifts out on the falling edge of SCLK.

4.2 Dual SPI Instructions

The BY25FQ32ES supports Dual SPI operation when using the “Dual Output Fast Read” (3BH), “Dual I/O Fast Read” (BBH) and “Read Manufacture ID/Device ID Dual I/O” (92H) instructions. These instructions allow data to be transferred to or from the device at two times the rate of the standard SPI. When using the Dual SPI instruction the SI and SO pins become bidirectional I/O pins: IO0 and IO1.

4.3 Quad SPI Instructions

The BY25FQ32ES supports Quad SPI operation when using the “Quad Output Fast Read”(6BH), “Quad I/O Fast Read” (EBH) ,”Quad I/O word Fast Read”(E7H),”Read Manufacture ID/Device ID Quad I/O”(94H) and “Quad Page Program”(32H) instructions. These instructions allow data to be transferred to or from the device at four times the rate of the standard SPI. When using the Quad SPI instruction the SI and SO pins become bidirectional I/O pins: IO0 and IO1, and /WP and /HOLD pins become IO2 and IO3. Quad SPI instructions require the non-volatile Quad Enable bit (QE) in Status Register to be set.

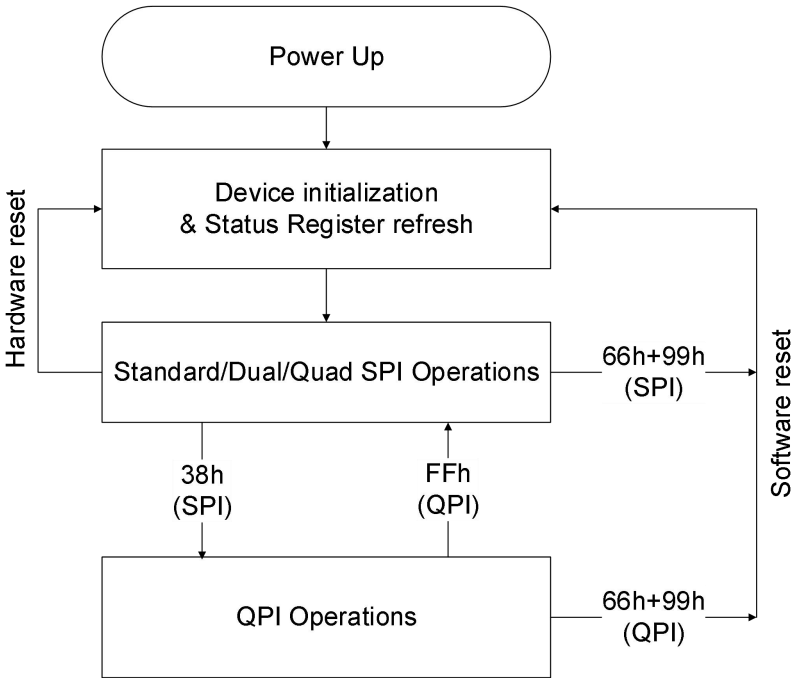
4.4 QPI Instructions

The BY25FQ32ES supports Quad Peripheral Interface (QPI) operations only when the device is switched from Standard/Dual/Quad SPI mode to QPI mode using the “Enter QPI (38h)” instruction. The typical SPI protocol requires that the byte-long instruction code being shifted into the device only via DI pin in eight serial clocks. The QPI mode utilizes all four IO pins to input the instruction code, thus only two serial clocks are required. This can significantly reduce the SPI instruction overhead and improve system performance in an XIP environment. Standard/Dual/Quad SPI mode and QPI mode are exclusive. Only one mode can be active at any given time. “Enter QPI (38h)” and “Exit QPI (FFh)” instructions are used to switch between these two modes. Upon power-up or after a software reset using “Enable Reset (66h)” and “Reset (99h)” instruction, the default state of the device is Standard/Dual/Quad SPI mode. To enable QPI mode, the non-volatile Quad Enable bit (QE) in Status Register-2 is required to be set to 1. When using QPI instructions, the DI and DO pins become bidirectional IO0 and IO1, and the /WP and /HOLD pins become IO2 and IO3 respectively.

4.5 DTR Instructions

The BY25FQ32ES supports DTR operation when using the DTR instructions (0DH/BDH/EDH/0EH). These instructions allow data to be transferred to or from the device at eight times the rate of the standard SPI, and data output will be latched on both rising and falling edges of the serial clock. When using the DTR instructions the SI and SO pins become bidirectional I/O pins: IO0 and IO1.

4.6 Switch between SPI and QPI operation



5. OPERATION FEATURES

5.1 Supply Voltage

5.1.1 Operating Supply Voltage

Prior to selecting the memory and issuing instructions to it, a valid and stable VCC voltage within the specified [VCC(min), VCC(max)] range must be applied (see ***Electrical Characteristics***). In order to secure a stable DC supply voltage, it is recommended to decouple the VCC line with a suitable capacitor (usually of the order of 10*nF* to 100*nF*) close to the VCC/VSS package pins. This voltage must remain stable and valid until the end of the transmission of the instruction and, for a Write instruction, until the completion of the internal write cycle (tW).

5.1.2 Power-up Conditions

When the power supply is turned on, VCC rises continuously from VSS to VCC. During this time, the Chip Select (/CS) line is not allowed to float but should follow the VCC voltage, it is therefore recommended to connect the /CS line to VCC via a suitable pull-up resistor.

In addition, the Chip Select (/CS) input offers a built-in safety feature, as the /CS input is edge sensitive as well as level sensitive: after power-up, the device does not become selected until a falling edge has first been detected on Chip Select (/CS). This ensures that Chip Select (/CS) must have been High, prior to going Low to start the first operation.

5.1.3 Device Reset

In order to prevent inadvertent Write operations during power-up (continuous rise of VCC), a power on reset (POR) circuit is included. At Power-up, the device does not respond to any instruction until VCC has reached the power on reset threshold voltage (this threshold is lower than the minimum VCC operating voltage defined in ***Power-up Timing***).

When VCC is lower than V_{WI}, the device is reset.

5.1.4 Power-down

At Power-down (continuous decrease in VCC), as soon as VCC drops from the normal operating voltage to below the power on reset threshold voltage(V_{WI}), the device stops responding to any instruction sent to it. During Power-down, the device must be deselected (Chip Select (/CS) should be allowed to follow the voltage applied on VCC) and in Standby Power mode (that is there should be no internal Write cycle in progress).

5.2 Active Power and Standby Power Modes

When Chip Select (/CS) is Low, the device is selected, and in the Active Power mode. The device consumes ICC.

When Chip Select (/CS) is High, the device is deselected. If a Write cycle is not currently in progress, the device then goes in to the Standby Power mode, and the device consumption drops to ICC1.

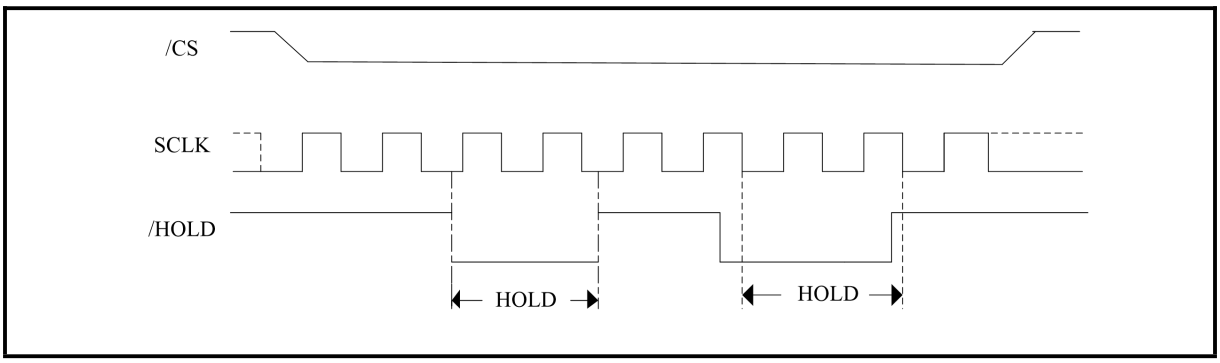
5.3 Hold Condition

When QE=0, HOLD/RST=0, the Hold (/HOLD) signal is used to pause any serial communications with the device without resetting the clocking sequence. During the Hold condition, the Serial Data Output (SO) is high impedance, and Serial Data Input (SI) and Serial Clock (SCLK) are Don't Care.

To enter the Hold condition, the device must be selected, with Chip Select (/CS) Low. Normally, the device is kept selected, for the whole duration of the Hold condition. Deselecting the device while it is in the Hold condition, has the effect of resetting the state of the device, and this mechanism can be used if it is required to reset any processes that had been in progress.

The Hold condition starts when the Hold (/HOLD) signal is driven Low at the same time as Serial Clock (SCLK) already being Low (as shown in ***Figure 4***).The Hold condition ends when the Hold (HOLD) signal is driven High at the same time as Serial Clock (C) already being Low. ***Figure 4*** also shows what happens if the rising and falling edges are not timed to coincide with Serial Clock (SCLK) being Low.

Figure 4. Hold condition activation



5.4 Software Reset & Hardware RESET

5.4.1 Software Reset

The BY25FQ32ES can be reset to the initial power-on state by a software reset sequence. This sequence must include two consecutive instructions: Enable Reset (66h) & Reset (99h). If the instruction sequence is successfully accepted, the device will take approximately tRST to reset. No instruction will be accepted during the reset period.

5.4.2 Hardware Reset (/HOLD pin)

The BY25FQ32ES can also be configured to utilize hardware /RESET pin. The HOLD/RST bit in the Status Register-3 is the configuration bit for /HOLD pin function or /RESET pin function. When HOLD/RST=0 (factory default), the pin acts as a /HOLD pin as described above; when HOLD/RST=1, the pin acts as a /RESET pin. Drive the /RESET pin low for a minimum period of 1us reset the device to its initial power-on state. Any on-going Program/Erase operation will be interrupted and data corruption may happen. While /RESET is low, the device will not accept any instruction input.

If QE bit is set to 1, the /HOLD or /RESET function will be disabled, the pin will become one of the four data I/O pin.

Hardware /RESET pin has the highest priority among all the input signals. Drive /RESET low for a minimum period of 1us will interrupt any on-going external/internal operations, regardless the status of other SPI signals (/CS, CLK, IOs, /WP and /HOLD).

Notes:

1. While a faster /RESET pulse (as short as a few hundred nanoseconds) will often reset the device, a 1us minimum pulse is recommended to ensure reliable operation.

5.4.3 Hardware Reset (JEDEC Standard Hardware Reset)

The BY25FQ32ES supports JEDEC Standard Hardware Reset. The JEDEC Standard Hardware Reset sequence can also be used to reset the device to its power on state without cycling power.

The reset sequence does not use the SCLK pin. The SCLK has to be low (mode 0) or high (mode 3) through the entire reset sequence. This prevents any confusion with a instruction, as no instruction bits are transferred (clocked).

A reset is commanded when the data on the SI pin is 0101 on four consecutive positive edges of the /CS pin with no edge on the SCLK pin throughout. The is a sequence where

1. /CS is driven active low to select the device.
2. Clock (SCLK) remains stable in either a high or low state.
3. SI is driven low by the bus master, simultaneously with /CS going active low. No SPI bus slave drives SI during /CS low before a transition of SCLK i.e.: slave streaming output active is not allowed until after the first edge of SCLK.
4. /CS is driven inactive. The slave captures the state of SI on the rising edge of /CS.

The above steps are repeated 4 times, each time alternating the state of SI.

After the fourth /CS pulse, the slave triggers its internal reset. SI is low on the first /CS, high on the second, low on the third, high on the fourth. This provides a value of 5H, unlike random noise. Any activity on SCLK during this time will halt the sequence and a Reset will not be generated. Figure below illustrates the timing for hardware Reset operation.

Figure 7. JEDEC Standard Hardware Reset

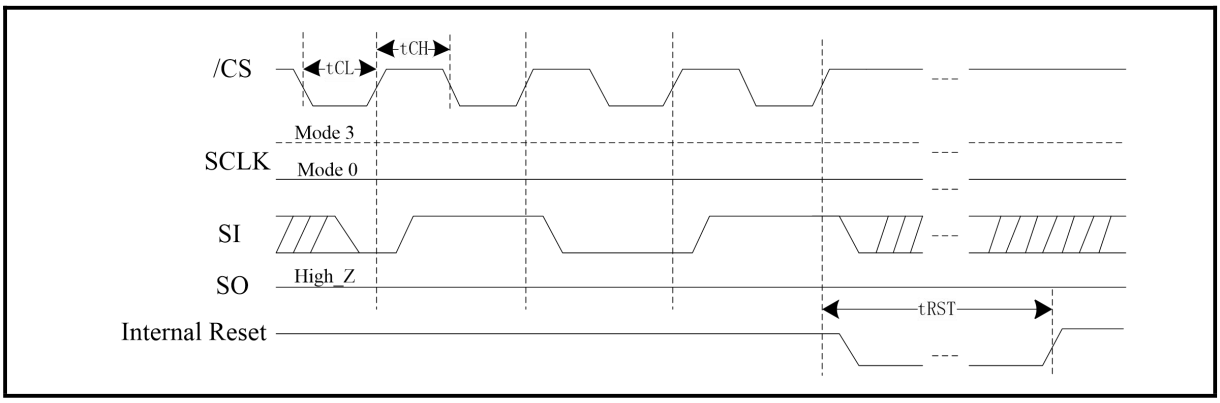


Table 3. JEDEC Standard Hardware Reset Timing Parameters

Parameter	Min.	Typ.	Max.	Unit.
tCL	20			ns
tCH	20			ns
Setup Time	5			ns
Hold Time	5			ns

5.5 Data Strobe Function

The Data Strobe function is used in 16-pin SOP 300mil、TFBGA6*8mm-24Ball (5x5 ball array) packages, and the DQS pin is an active output pin for the Data Strobe (DQS) signal during DTR Read operations in SPI and QPI mode and non DTR Read operations in QPI mode (except 9FH, 90H, ABH, 92H, see ***Table 4***). The DQS signal is typically used in high speed applications to indicate when the output data is ready to be fetched by the controllers. When the data strobe function is enabled, DQS signal is driven to ground once CS# goes LOW, and will start to toggle when the output data is ready on the I/O pins. The toggling frequency is the same as the CLK frequency. For DTR Read operations, the data should be latched on both rising edge and falling edge of the DQS signal.

Table 4. Instructions and modes supporting DQS

Instructions	SPI	QPI
Fast Read (0BH)	-	DQS
Quad I/O Fast Read (EBH)	-	DQS
DTR Fast Read Quad I/O(EDH)	DQS	DQS
Burst Read with Wrap (0CH)	-	DQS
DTR Burst Read with Wrap (0EH)	-	DQS
Quad I/O Read Manufacture ID/ Device ID (94H)	-	DQS
Read Security Registers (48H)	-	DQS
Read Serial Flash Discoverable Parameter (5AH)	-	DQS

5.6 Write Protect Features

1. Software Protection (Memory array):

   - The Block Protect (BP4, BP3, BP2, BP1, BP0) bits define the section of the memory array that can be read but not change.

2. Hardware Protection (Status register): /WP going low to protected the writable bits of Status Register.

3. Deep Power-Down: In Deep Power-Down Mode, all instructions are ignored except the Release from deep Power-Down Mode instruction.

4. Device resets when VCC is below threshold: Upon power-up or at power-down, the BY25FQ32ES will maintain a reset condition while VCC is below the threshold value of V_{WI}. While reset, all operations are disabled and no instructions are recognized.

5. Time delay write disable after Power-up: During power-up and after the VCC voltage exceeds $VCC_{(min)}$, all program and erase related instructions are further disabled for a time delay of tVSL. This includes the Write Enable, Page Program, Sector Erase, Block Erase, Chip Erase and the Write Status Register instructions.

6. Write Enable: The Write Enable instruction is set the Write Enable Latch bit. The WEL bit will return to reset by following situation:

   -Power –up
   -Write Disable
   -Write Status Register (Whether the SR is protected, WEL will return to reset)
   -Page Program (Whether the program area is protected, WEL will return to reset)
   -Sector Erase/Block Erase/Chip Erase (Whether the erase area is protected, WEL will return to reset)
   -Software Reset
   -Hardware Reset

7. One Time Program (OTP) write protection for array and Security Registers using Status Register.

5.7 Status Register

5.7.1 Status Register Table

See ***Table 3*** for detail description of the Status Register bits.

Table 3. Status Register

	SR3							
	S23	**S22**	**S21**	**S20**	**S19**	**S18**	**S17**	**S16**
	HOLD/RST	**DRV1**	**DRV0**	**DC**	**Reserved**	**Reserved**	**Reserved**	**Reserved**
Default (1)	0	0	0	0	×	×	×	×

	SR2							
	S15	**S14**	**S13**	**S12**	**S11**	**S10**	**S9**	**S8**
	SUS1	**CMP**	**LB3**	**LB2**	**LB1**	**SUS2**	**QE**	**SRP1**
Default (1)	0	0	0	0	0	0	0	0
	Read Only		OTP	OTP	OTP	Read Only		

	SR1							
	S7	**S6**	**S5**	**S4**	**S3**	**S2**	**S1**	**S0**
	SRP0	**BP4**	**BP3**	**BP2**	**BP1**	**BP0**	**WEL**	**WIP**
Default (1)	0	0	0	0	0	0	0	0
							Read Only	Read Only

Notes:

1. The default value is set by Manufacturer during wafer sort, Marked as Default in following text

5.7.2 The Status and Control Bits

5.7.2.1 WIP bit

The Write in Progress (WIP) bit indicates whether the memory is busy in program/erase/write status register progress. When WIP bit sets to 1, means the device is busy in program/erase/write status register progress, when WIP bit sets 0, means the device is not in program/erase/write status register progress.

5.7.2.2 WEL bit

The Write Enable Latch (WEL) bit indicates the status of the internal Write Enable Latch. When set to 1 the internal Write Enable Latch is set, when set to 0 the internal Write Enable Latch is reset and no Write Status Register, Program or Erase, etc. instruction is accepted.

5.7.2.3 BP4, BP3, BP2, BP1, BP0 bits

The Block Protect (BP4, BP3, BP2, BP1, BP0) bits are non-volatile. They define the size of the area to be software protected against Program and Erase instructions. These bits are written with the Write Status Register instruction. When WPS=0, and the Block Protect (BP4, BP3, BP2, BP1, BP0) bits are set to 1, the relevant memory area (as defined in ***Table 6-Table 7***).becomes protected against Page Program, Sector Erase and Block Erase instructions. The Block Protect (BP4, BP3, BP2, BP1, BP0) bits can be written provided that the Hardware Protected mode has not been set. The Chip Erase instruction is executed, if the Block Protect (BP2, BP1, BP0) bits are 0 and CMP=0 or The Block Protect (BP2, BP1, BP0) bits are 1 and CMP=1.

5.7.2.4 SRP1, SRP0 bits

The Status Register Protect (SRP1 and SRP0) bits are non-volatile Read/Write bits in the status register. The SRP bits control the method of write protection: software protection, hardware protection, power supply lock-down or one time programmable protection.

Table 4. Status Register protect table

SRP1	SRP0	/WP	Status Register	Description
0	0	X	Software Protected	The Status Register can be written to after a Write Enable instruction, WEL=1.(Factory Default)
0	1	0	Hardware Protected	/WP=0, the Status Register locked and cannot be written.
0	1	1	Hardware Unprotected	/WP=1, the Status Register is unlocked and can be written to after a Write Enable instruction, WEL=1.
1	0	X	Power Supply Lock-Down(1)	Status Register is protected and cannot be written to again until the next Power-Down, Power-Up cycle.
1	1	X	One Time Program(2)	Status Register is permanently protected and cannot be written to.

Notes:

1. When SRP1, SRP0= (1, 0), a Power-Down, Power-Up cycle will change SRP1, SRP0 to (0, 0) state.
2. The One time Program feature is available upon special order. Please contact BY Technology for details.

5.7.2.5 QE bit

The Quad Enable (QE) bit is a non-volatile Read/Write bit in the Status Register that allows Quad SPI and QPI operation. When the QE bit is set to 0 (Default) the /WP pin and /HOLD pin are enable. When the QE pin is set to 1, the Quad IO2 and IO3 pins are enabled. (The QE bit should never be set to 1 during standard SPI or Dual SPI operation if the /WP or /HOLD pins directly to the power supply).

QE bit is required to be set to 1 before issuing an “Enter QPI (38h)” instruction to switch the device from Standard/Dual/Quad SPI mode to QPI mode; otherwise the command (38h) will be ignored. When the device is in QPI mode, QE bit will remain to be 1. A “Write Status Register” command in QPI mode cannot change QE bit from 1 to 0.

5.7.2.6 LB3/LB2/LB1 bits

The Security Register Lock (LB3/LB2/LB1) bits are non-volatile One Time Program (OTP) bits in Status Register (S13–S11) that provide the write protect control and status to the Security Registers. The default state of LB is 0, the security registers are unlocked. LB can be set to 1 individually using the Write Register instruction. LB is One Time Programmable, once they are set to 1, the Security Registers will become read-only permanently.

5.7.2.7 CMP bit

The Complement Protect (CMP) bit is a non-volatile Read/Write bit in the Status Register (S14). It is used in conjunction the BP4-BP0 bits to provide more flexibility for the array protection. Please see the Status registers Memory Protection table for details. The default setting is CMP=0.

5.7.2.8 SUS1/SUS2 bits

The Suspend Status (SUS1 and SUS2) bits are read only bits in the status register2 (S15 and S10) that are set to 1 after executing a Program/Erase Suspend (75H) instruction (The Erase Suspend will set SUS1 to 1, and the Program Suspend will set the SUS2 to 1). The SUS1 and SUS2 bits are cleared to 0 by Program/Erase Resume (7AH) instruction as well as a power-down, power-up cycle.

5.7.2.9 HOLD/RST bit

The /HOLD or /RESET Pin Function (HOLD/RST) bit is used to determine whether /HOLD or /RESET function should be implemented on the hardware pin. When HOLD/RST=0 (factory default), the pin acts as /HOLD; when HOLD/RST=1, the pin acts as /RESET. However, /HOLD or /RESET functions are only available when QE=0. If QE is set to 1, the /HOLD and /RESET functions are disabled, the pin acts as a dedicated data I/O pin.

5.7.2.10 DC bit

The Dummy Configuration (DC) bit is non-volatile, which selects the number of dummy cycles between the end of address and the start of read data output. Dummy cycles provide additional latency that is needed to complete the initial read access of the flash array before data can be returned to the host system. Some read commands require additional dummy cycles as the SCLK frequency increases.

The following dummy cycle tables provide different dummy cycle settings that are configured.

DC bit	Numbers of Dummy Cycles(1)	Dual IO Fast Read(BBH)	
		W/O DQS	with DQS
0	4	104 MHz	104 MHz
1	8	104/133R MHz(2)	104/133R MHz(2)

Notes:
1. The number of dummy includes M7-0.
2. "R" mean VCC range= 3.0V-3.6V.

DC bit	Numbers of Dummy Cycles(1)	Quad I/O Fast Read (EBH)	
		W/O DQS	with DQS
0(default)	6	104 MHz	104 MHz
1	8	104/133R MHz(2)	104/133R MHz(2)
	10(3)	133/166R MHz(2)	133/166R MHz(2)

Notes:
1. The number of dummy includes M7-0.
2. "R" mean VCC range= 3.0V-3.6V.
3. The 10 dummy is available. Please contact BY Technology.

DC bit	Numbers of Dummy Cycles(1)	DTR Fast Read (0DH)		DTR Fast Read Dual I/O (BDH)	
		W/O DQS	with DQS	W/O DQS	with DQS
0(default)	6	84 MHz	84 MHz	84 MHz	84 MHz
1	10	104 MHz	104 MHz	104 MHz	104 MHz

DC bit	Numbers of Dummy Cycles(1)	DTR Fast Read Quad I/O(EDH)	
		W/O DQS	with DQS
0(default)	8	84	84
1	10	104 MHz	104 MHz
	12(3)	104 MHz(	104/133R MHz(2)

Notes:
1. The number of dummy includes M7-0.
2. "R" mean VCC range= 3.0V-3.6V.
3. The 12 dummy is available. Please contact BY Technology.

5.7.2.11 DRV1/DRV0 bits

The Output Driver Strength (DRV1&DRV0) bits are used to determine the output driver strength for the Read instruction.

Table 5. The Output Driver Strength

DRV1,DRV0	Driver Strength
00	100%
01	75%(default)
10	50%
11	25%

5.8 Array Memory Protection

5.8.1 Block Protect Table

Table 6. BY25FQ32ES Block Memory Protection (CMP=0)

Status Register Content					Memory Content			
BP4	BP3	BP2	BP1	BP0	Blocks	Addresses	Density	Portion
X	X	0	0	0	NONE	NONE	NONE	NONE
0	0	0	0	1	63	3F0000H-3FFFFFH	64KB	Upper 1/64
0	0	0	1	0	62 to 63	3E0000H-3FFFFFH	128KB	Upper 1/32
0	0	0	1	1	60 to 63	3C0000H-3FFFFFH	256KB	Upper 1/16
0	0	1	0	0	56 to 63	380000H-3FFFFFH	512KB	Upper 1/8
0	0	1	0	1	48 to 63	300000H-3FFFFFH	1MB	Upper 1/4
0	0	1	1	0	32 to 63	200000H-3FFFFFH	2MB	Upper 1/2
0	1	0	0	1	0	000000H-00FFFFH	64KB	Lower 1/64
0	1	0	1	0	0 to 1	000000H-01FFFFH	128KB	Lower 1/32
0	1	0	1	1	0 to 3	000000H-03FFFFH	256KB	Lower 1/16
0	1	1	0	0	0 to 7	000000H-07FFFFH	512KB	Lower 1/8
0	1	1	0	1	0 to 15	000000H-0FFFFFH	1MB	Lower 1/4
0	1	1	1	0	0 to 31	000000H-1FFFFFH	2MB	Lower 1/2
X	X	1	1	1	0 to 63	000000H-3FFFFFH	4MB	ALL
1	0	0	0	1	63	3FF000H-3FFFFFH	4KB	Top Block
1	0	0	1	0	63	3FE000H-3FFFFFH	8KB	Top Block
1	0	0	1	1	63	3FC000H-3FFFFFH	16KB	Top Block
1	0	1	0	X	63	3F8000H-3FFFFFH	32KB	Top Block
1	0	1	1	0	63	3F8000H-3FFFFFH	32KB	Top Block
1	1	0	0	1	0	000000H-000FFFH	4KB	Bottom Block
1	1	0	1	0	0	000000H-001FFFH	8KB	Bottom Block
1	1	0	1	1	0	000000H-003FFFH	16KB	Bottom Block
1	1	1	0	X	0	000000H-007FFFH	32KB	Bottom Block
1	1	1	1	0	0	000000H-007FFFH	32KB	Bottom Block

Table 7. BY25FQ32ES Block Memory Protection (CMP=1)

Status Register Content					Memory Content			
BP4	BP3	BP2	BP1	BP0	Blocks	Addresses	Density	Portion
X	X	0	0	0	ALL	000000H-3FFFFFH	4MB	ALL
0	0	0	0	1	0 to 62	000000H-3EFFFFH	4032KB	Lower 63/64
0	0	0	1	0	0 to 61	000000H-3DFFFFH	3968KB	Lower 31/32
0	0	0	1	1	0 to 59	000000H-3BFFFFH	3840KB	Lower 15/16
0	0	1	0	0	0 to 55	000000H-37FFFFH	3584KB	Lower 7/8
0	0	1	0	1	0 to 47	000000H-2FFFFFH	3MB	Lower 3/4
0	0	1	1	0	0 to 31	000000H-1FFFFFH	2MB	Lower 1/2
0	1	0	0	1	1 to 63	010000H-3FFFFFH	4032KB	Upper 63/64
0	1	0	1	0	2 to 63	020000H-3FFFFFH	3968KB	Upper 31/32
0	1	0	1	1	4 to 63	040000H-3FFFFFH	3840KB	Upper 15/16
0	1	1	0	0	8 to 63	080000H-3FFFFFH	3584KB	Upper 7/8
0	1	1	0	1	16 to 63	100000H-3FFFFFH	3MB	Upper 3/4
0	1	1	1	0	32 to 63	200000H-3FFFFFH	2MB	Upper 1/2
X	X	1	1	1	NONE	NONE	NONE	NONE
1	0	0	0	1	0 to 63	000000H-3FEFFFH	4092KB	L-1023/1024
1	0	0	1	0	0 to 63	000000H-3FDFFFH	4088KB	L-511/512
1	0	0	1	1	0 to 63	000000H-3FBFFFH	4080KB	L-255/256
1	0	1	0	X	0 to 63	000000H-3F7FFFH	4064KB	L-127/128
1	0	1	1	0	0 to 63	000000H-3F7FFFH	4064KB	L-127/128
1	1	0	0	1	0 to 63	001000H-3FFFFFH	4092KB	U-1023/1024
1	1	0	1	0	0 to 63	002000H-3FFFFFH	4088KB	U-511/512
1	1	0	1	1	0 to 63	004000H-3FFFFFH	4080KB	U-255/256
1	1	1	0	X	0 to 63	008000H-3FFFFFH	4064KB	U-127/128
1	1	1	1	0	0 to 63	008000H-3FFFFFH	4064KB	U-127/128

6. DEVICE IDENTIFICATION

Three legacy Instructions are supported to access device identification that can indicate the manufacturer, device type, and capacity (density). The returned data bytes provide the information as shown in the below table.

Table 8. BY25FQ32ES ID Definition table

Operation Code	M7-M0	ID15-ID8	ID7-ID0
9FH	68	40	16
90H/92H/94H	68		15
ABH			15

7. INSTRUCTIONS DESCRIPTION

All instructions, addresses and data are shifted in and out of the device, beginning with the most significant bit on the first rising edge of SCLK after /CS is driven low. Then, the one byte instruction code must be shifted in to the device, most significant bit first on SI, each bit being latched on the rising edges of SCLK.

See ***Table 9***, every instruction sequence starts with a one-byte instruction code. Depending on the instruction, this might be followed by address bytes, or by data bytes, or by both or none. /CS must be driven high after the last bit of the instruction sequence has been shifted in. For the instruction of Read, Fast Read, Read Status Register or Release from Deep Power Down, and Read Device ID, the shifted-in instruction sequence is followed by a data out sequence. /CS can be driven high after any bit of the data-out sequence is being shifted out.

For the instruction of Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register, Write Enable, Write Disable or Deep Power-Down instruction, etc. /CS must be driven high exactly at a byte boundary, otherwise the instruction is rejected, and is not executed. That is /CS must drive high when the number of clock pulses after /CS being driven low is an exact multiple of eight. For Page Program, if at any time the input byte is not a full byte, nothing will happen and WEL will not be reset.

Table 9. Instruction Set Table

Instruction Set Table 1 (Standard/Dual/Quad SPI Instructions)(1)

Instruction Name	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6
Write Enable	06h					
Volatile SR Write Enable	50h					
Write Disable	04h					
Read Status Register-1	05h	(S7-S0)(2)				
Write Status Register-1(4)	01h	(S7-S0)(4)				
Read Status Register-2	35h	(S15-S8)(2)				
Write Status Register-2	31h	(S15-S8)				
Read Status Register-3	15h	(S23-S16)(2)				
Write Status Register-3	11h	(S23-S16)				
Chip Erase	C7h/60h					
Erase/Program Suspend	75h					
Erase/Program Resume	7Ah					
Power-down	B9h					
Release Power-down / ID	ABh	Dummy	Dummy	Dummy	(ID7-ID0)(2)	
Manufacturer/Device ID	90h	Dummy	Dummy	00h	(MF7-MF0)	(ID7-ID0)(2)
JEDEC ID	9Fh	(MF7-MF0)	(ID15-ID8)	(ID7-ID0)(2)		
Global Block Lock	7Eh					
Global Block Unlock	98h					
Enter QPI Mode	38h					
Enable Reset	66h					
Reset Device	99h					
Read Serial Flash Discoverable Parameter	5Ah	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)	Next bytes

Instruction Name	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6 ~ Byte 21
Read Unique ID	4Bh	Dummy	Dummy	Dummy	Dummy	(UID127-UID0)

Instruction Set Table 2 (Standard/Dual/Quad SPI Instructions) (1)

Instruction Name	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7	Byte 8	Byte 9
Page Program	02h	A23-A16	A15-A8	A7-A0	D7-D0(3)	Next bytes			
Quad Page Program	32h	A23-A16	A15-A8	A7-A0	D7-D0(3)(9)	Next bytes			
Sector Erase (4KB)	20h	A23-A16	A15-A8	A7-A0					
Block Erase (32KB)	52h	A23-A16	A15-A8	A7-A0					
Block Erase (64KB)	D8h	A23-A16	A15-A8	A7-A0					
Read Data	03h	A23-A16	A15-A8	A7-A0	(D7-D0)	(D7-D0)	Next bytes		
Fast Read	0Bh	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)	Next bytes		
Fast Read Dual Output	3Bh	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)(7)	Next bytes		
Fast Read Quad Output	6Bh	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)(9)	Next bytes		
Erase Security Register(5)	44h	A23-A16	A15-A8	A7-A0					
Program Security Register(5)	42h	A23-A16	A15-A8	A7-A0	D7-D0(3)	Next bytes			
Read Security Register(5)	48h	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)	Next bytes		
Fast Read Dual I/O	BBh	A23-A16(6)	A15-A8(6)	A7-A0(6)	M7-M0(6)	(D7-D0)(7)			
Mftr./Device ID Dual I/O	92h	A23-A16(6)	A15-A8(6)	A7-A0(6)	Dummy	(MF7-MF0)(7)	(D7-D0)(7)		
Set Burst with Wrap	77h	Dummy	Dummy	Dummy	W8-W0				
Fast Read Quad I/O(10)	EBh	A23-A16(8)	A15-A8(8)	A7-A0(8)	M7-M0(8)	Dummy	Dummy	(D7-D0)(9)	Next byte
Word Read Quad I/O(11) (12)	E7h	A23-A16(8)	A15-A8(8)	A7-A0(8)	M7-M0(8)	Dummy	(D7-D0)(9)	Next bytes	
Mftr./Device ID Quad I/O	94h	A23-A16(8)	A15-A8(8)	A7-A0(8)	Dummy	Dummy	Dummy	(MF7-MF0)(9)	(ID7-ID0)(9)

Instruction Set Table 3 (QPI Instructions) (14)

Instruction Name	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6
Write Enable	06h					
Volatile SR Write Enable	50h					
Write Disable	04h					
Read Status Register-1	05h	(S7-S0)(2)				
Write Status Register-1(4)	01h	(S7-S0)(4)				
Read Status Register-2	35h	(S15-S8)(2)				
Write Status Register-2	31h	(S15-S8)				
Read Status Register-3	15h	(S23-S16)(2)				
Write Status Register-3	11h	(S23-S16)				
Chip Erase	C7h/60h					
Erase/Program Suspend	75h					
Erase/Program Resume	7Ah					
Power-down	B9h					
Set Read Parameters	C0h	P7-P0				
Release Powerdown / ID	ABh	Dummy	Dummy	Dummy	(ID7-ID0)(2)	
Manufacturer/Device ID	90h	Dummy	Dummy	00h	(MF7-MF0)(2)	(ID7-ID0)(2)
JEDEC ID	9Fh	(MF7-MF0)(2)	(ID15-ID8)(2)	(ID7-ID0)(2)		
Exit QPI Mode	FFh					
Enable Reset	66h					
Reset Device	99h					
Page Program	02h	A23-A16	A15-A8	A7-A0	D7-D0(3)(9)	Next bytes
Sector Erase (4KB)	20h	A23-A16	A15-A8	A7-A0		
Block Erase (32KB)	52h	A23-A16	A15-A8	A7-A0		
Block Erase (64KB)	D8h	A23-A16	A15-A8	A7-A0		
Fast Read	0Bh	A23-A16	A15-A8	A7-A0	Dummy(15)	(D7-D0)
Burst Read with Wrap(16)	0Ch	A23-A16	A15-A8	A7-A0	Dummy(15)	(D7-D0)
Fast Read Quad I/O	EBh	A23-A16	A15-A8	A7-A0	M7-M0(15)	(D7-D0)
Read Security Registers(5)	48h	A23-A16(8)	A15-A8(8)	A7-A0(8)	Dummy	D7-D0
Erase Security Registers(5)	44h	A31-A24	A23-A16(8)	A15-A8(8)	A7-A0(8)	
Program Security Registers(5)	42h	A23-A16(8)	A15-A8(8)	A7-A0(8)	D7-D0	Next Byte
Read Serial Flash Discoverable Parameter	5Ah	A23-A16	A15-A8	A7-A0	Dummy	(D7-D0)

Instruction Set Table-DTR(SPI Instructions)

Data Input Output	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
Clock Number(1-1-1)	**8**	**4**	**4**	**4**	**6**	**4**	**4**
DTR Fast Read	0Dh	A23-A16	A15-A8	A7-A0	Dummy	D7-D0	
Clock Number(1-2-2)	**8**	**2**	**2**	**2**	**2**	**4**	**2**
DTR Fast Read Dual I/O	BDh	A23-A16	A15-A8	A7-A0	M7-M0	Dummy	(D7-D0)
Clock Number(1-4-4)	**8**	**1**	**1**	**1**	**1**	**7**	**1**
DTR Fast Read Quad I/O	EDh	A23-A16	A15-A8	A7-A0	M7-M0	Dummy	(D7-D0)

Instruction Set Table-DTR (QPI Instructions)

Data Input Output	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
Clock Number(4-4-4)	**2**	**1**	**1**	**1**	**8**	**1**	**1**
DTR Read with Wrap(13)	0Eh	A23-A16	A15-A8	A7-A0	Dummy	D7-D0	
DTR Fast Read	0Dh	A23-A16	A15-A8	A7-A0	Dummy	D7-D0	
Clock Number(4-4-4)	**2**	**1**	**1**	**1**	**1**	**7**	**1**
DTR Fast Read Quad I/O	EDh	A23-A16	A15-A8	A7-A0	M7-M0	Dummy	(D7-D0)

Notes:

1. Data bytes are shifted with Most Significant Bit first. Byte fields with data in parenthesis "( )" indicate data output from the device on 1, 2 or 4 IO pins.
2. The Status Register contents and Device ID will repeat continuously until /CS terminates the instruction.
3. At least one byte of data input is required for Page Program, Quad Page Program and Program Security Registers, up to 256 bytes of data input. If more than 256 bytes of data are sent to the device, the addressing will wrap to the beginning of the page and overwrite previously sent data.
4. Write Status Register-1 (01h) can also be used to program Status Register-1&2, see *section 7.1.5*.
5. Security Register Address:

Security Register 1	A23-16 = 00h	A15-8 = 10h	A7-0 = byte address
Security Register 2	A23-16 = 00h	A15-8 = 20h	A7-0 = byte address
Security Register 3	A23-16 = 00h	A15-8 = 30h	A7-0 = byte address

6. Dual SPI address input format:
   IO0 = A22, A20, A18, A16, A14, A12, A10, A8, A6, A4, A2, A0, M6, M4, M2, M0
   IO1 = A23, A21, A19, A17, A15, A13, A11, A9, A7, A5, A3, A1, M7, M5, M3, M1
7. Dual SPI data output format:
   IO0 = (D6, D4, D2, D0)
   IO1 = (D7, D5, D3, D1)
8. Quad SPI address input format:
   IO0 = A20, A16, A12, A8, A4, A0, M4, M0
   IO1 = A21, A17, A13, A9, A5, A1, M5, M1
   IO2 = A22, A18, A14, A10, A6, A2, M6, M2
   IO3 = A23, A19, A15, A11, A7, A3, M7, M3
9. Quad SPI data input/output format:
   IO0 = (D4, D0, ...)
   IO1 = (D5, D1, ...)
   IO2 = (D6, D2, ...)
   IO3 = (D7, D3, ...)
10. Fast Read Quad I/O data output format:
    IO0 = (x, x, x, x, D4, D0, D4, D0)
    IO1 = (x, x, x, x, D5, D1, D5, D1)
    IO2 = (x, x, x, x, D6, D2, D6, D2)
    IO3 = (x, x, x, x, D7, D3, D7, D3)
11. Word Read Quad I/O data output format:
    IO0 = (x, x, D4, D0, D4, D0, D4, D0)
    IO1 = (x, x, D5, D1, D5, D1, D5, D1)
    IO2 = (x, x, D6, D2, D6, D2, D6, D2)
    IO3 = (x, x, D7, D3, D7, D3, D7, D3)
12. For Word Read Quad I/O, the lowest address bit must be 0. (A0 = 0)
13. For Octal Word Read Quad I/O, the lowest four address bits must be 0. (A3, A2, A1, A0 = 0)
14. QPI Command, Address, Data input/output format:

CLK # 0 1 2 3 4 5 6 7 8 9 10 11

IO0 = C4, C0,	A20, A16,	A12, A8,	A4, A0,	D4, D0,	D4, D0
IO1 = C5, C1,	A21, A17,	A13, A9,	A5, A1,	D5, D1,	D5, D1
IO2 = C6, C2,	A22, A18,	A14, A10,	A6, A2,	D6, D2,	D6, D2
IO3 = C7, C3,	A23, A19,	A15, A11,	A7, A3,	D7, D3,	D7, D3

15. The number of dummy clocks for QPI Fast Read, QPI Fast Read Quad I/O & QPI Burst Read with Wrap is controlled by read parameter P7 – P4.
16. The wrap around length for QPI Burst Read with Wrap is controlled by read parameter P3 – P0.

Table 10. Instructions that need to send the Write Enable/Write Enable for Volatile Status Register instruction

Instruction		Write
Write Status Register	01h/31h/11h	06H/50H
Erase Security Registers	44h	06H
Program Security Registers	42h	06H
Page Program	02h	06H
Quad Page Program	32h	06H
Sector Erase	20h	06H
32KB Block Erase	52h	06H
64KB Block Erase	D8h	06H
Chip Erase	60h/C7h	06H

7.1 Configuration and Status Instructions

7.1.1 Write Enable (06H)

See ***Figure 5-Figure 6***，the Write Enable instruction is for setting the Write Enable Latch bit. The Write Enable Latch bit must be set prior to every Write Status Register, Program, Erase. The Write Enable instruction sequence: /CS goes low sending the Write Enable instruction, /CS goes high.

Please note that the Write Enable instruction sent when the Write Enable for Volatile Status Register instruction is valid is not accepted. Therefore, when need to send the Write Enable instruction, but do not know if the Write Enable for Volatile Status Register instruction is valid, please send the Write Disable instruction first.

Figure 5. Write Enable Sequence Diagram (SPI Mode)

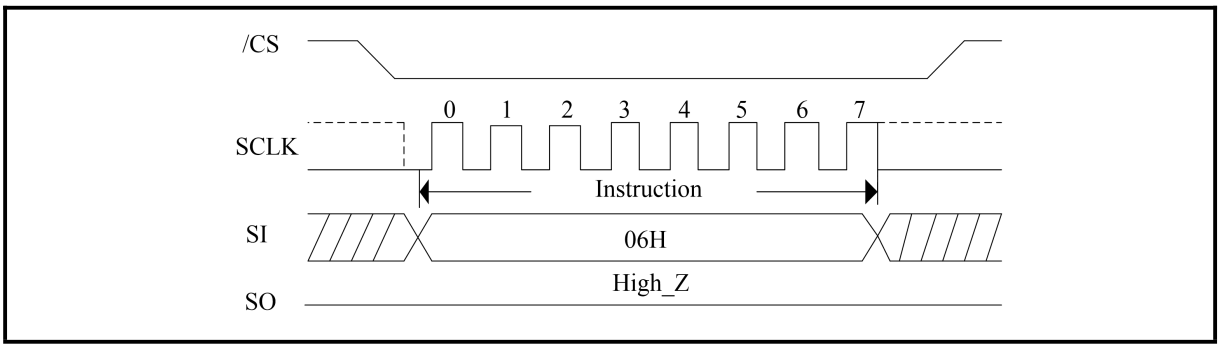
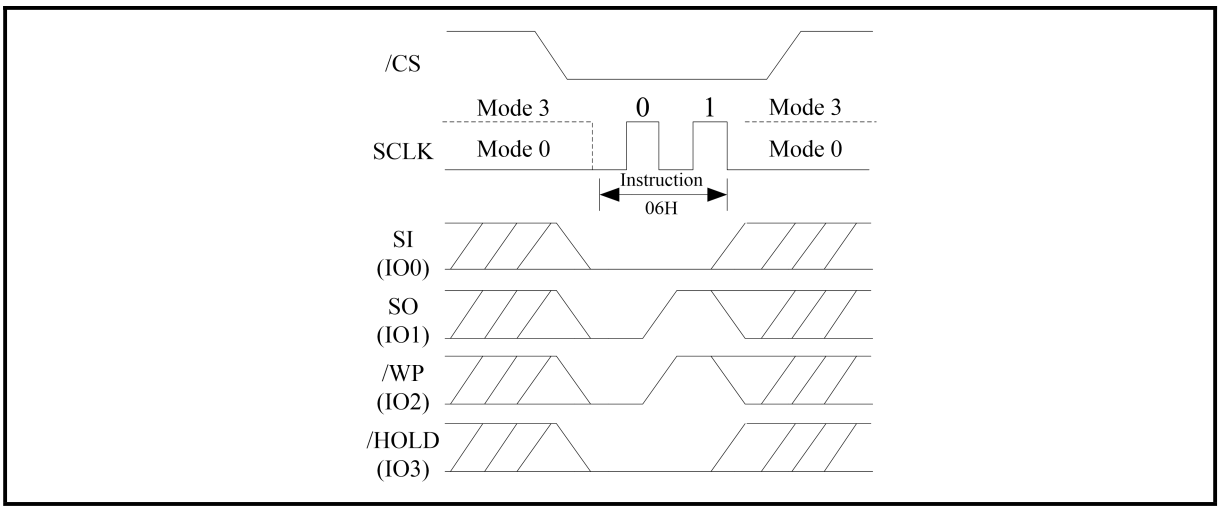


Figure 6. Write Enable Sequence Diagram (QPI Mode)



7.1.2 Write Enable for Volatile Status Register (50H)

See ***Figure 7-Figure 8***, the non-volatile Status Register bits can also be written to as volatile bits (HOLD/RST, DRV1, DRV0, DC, CMP, QE, SRP1, SRP0, BP4, BP3, BP2, BP1, BP0). This gives more flexibility to change the system configuration and memory protection schemes quickly without waiting for the typical non-volatile bit write cycles or affecting the endurance of the Status Register non-volatile bits. Write Enable for Volatile Status Register instruction will not set the Write Enable Latch bit, it is only valid for the Write Status Registers instruction to change the volatile Status Register bit values (After the software/hardware reset or re-powered, the volatile Status Register bit values will be restored to the default value or the value input by the Write Enable instruction).

Please note that the Write Enable for Volatile Status Register instruction sent when the Write Enable instruction is valid is not accepted. Therefore, when need to send the Write Enable for Volatile Status Register instruction, please first determine whether the Write Enable instruction is not valid.

Figure 7. Write Enable for Volatile Status Register (SPI Mode)

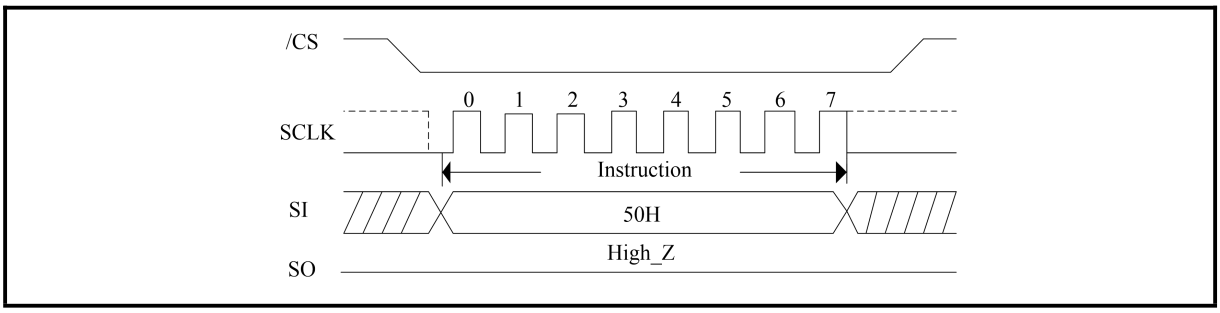
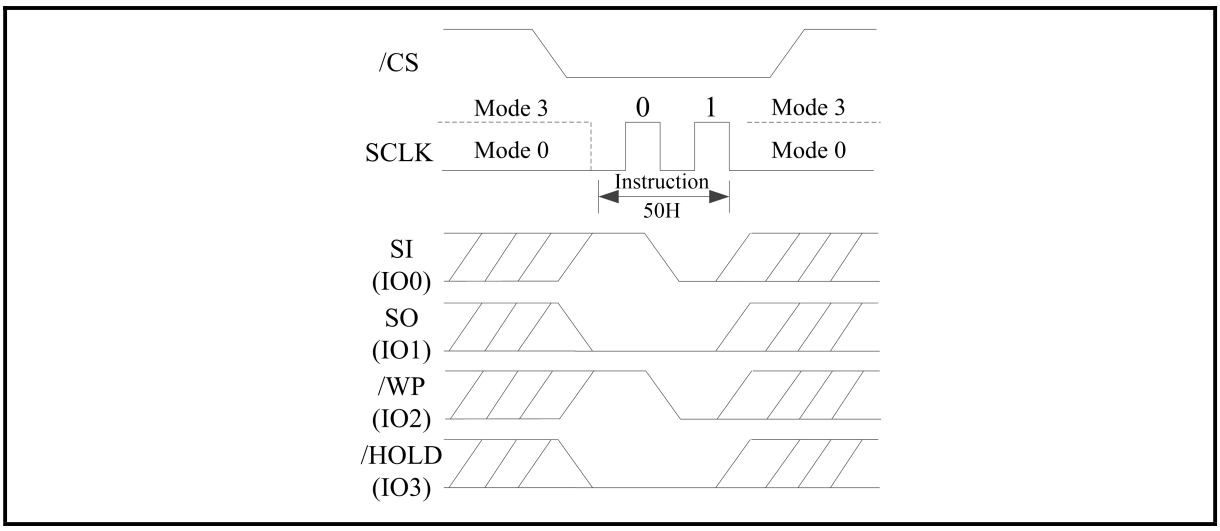


Figure 8. Write Enable for Volatile Status Register (QPI Mode)



7.1.3 Write Disable (04H)

See ***Figure 9-Figure 10***, the Write Disable instruction is for resetting the Write Enable Latch bit or invalidate the Write Enable for Volatile Status Register instruction. The Write Disable instruction sequence: /CS goes low -> sending the Write Disable instruction -> /CS goes high. The WEL bit is reset by following condition: Power-up and upon completion of the Write Status Register, Page Program, Sector Erase, Block Erase and Chip Erase, Program/Erase Security Registers and Reset instructions.

Figure 9. Write Disable Sequence Diagram (SPI Mode)

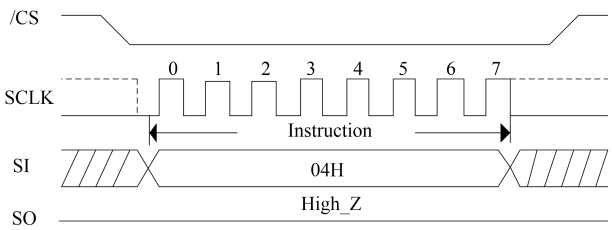
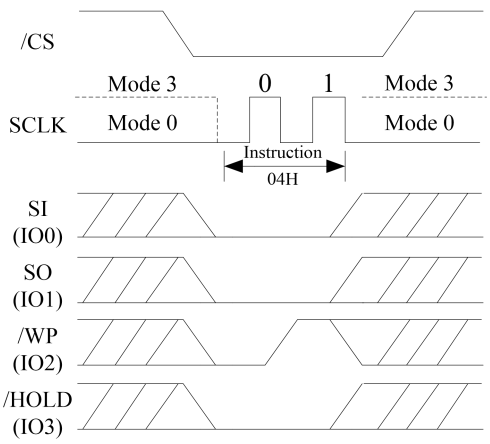


Figure 10. Write Disable Sequence Diagram (QPI Mode)



7.1.4 Read Status Register (05H or 35H or 15H)

See ***Figure 11-Figure 12***, the Read Status Register instruction is for reading the Status Register. The Status Register may be read at any time, even while a Program, Erase or Write Status Register cycle is in progress. When one of these cycles is in progress, it is recommended to check the Write in Progress (WIP) bit before sending a new instruction to the device. It is also possible to read the Status Register continuously. For instruction code “05H”, the SO will output Status Register bits S7~S0. The instruction code “35H”, the SO will output Status Register bits S15~S8, The instruction code “15H”, the SO will output Status Register bits S23~16.

Figure 11. Read Status Register Sequence Diagram (SPI Mode)

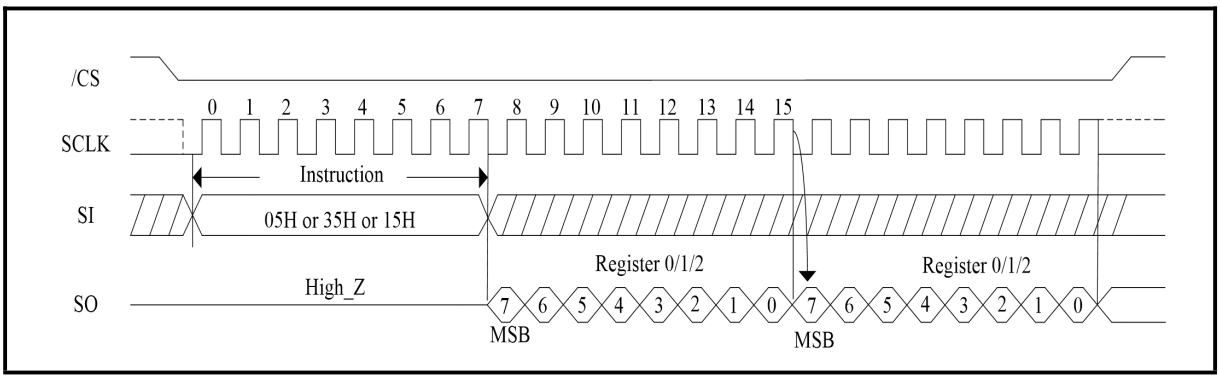
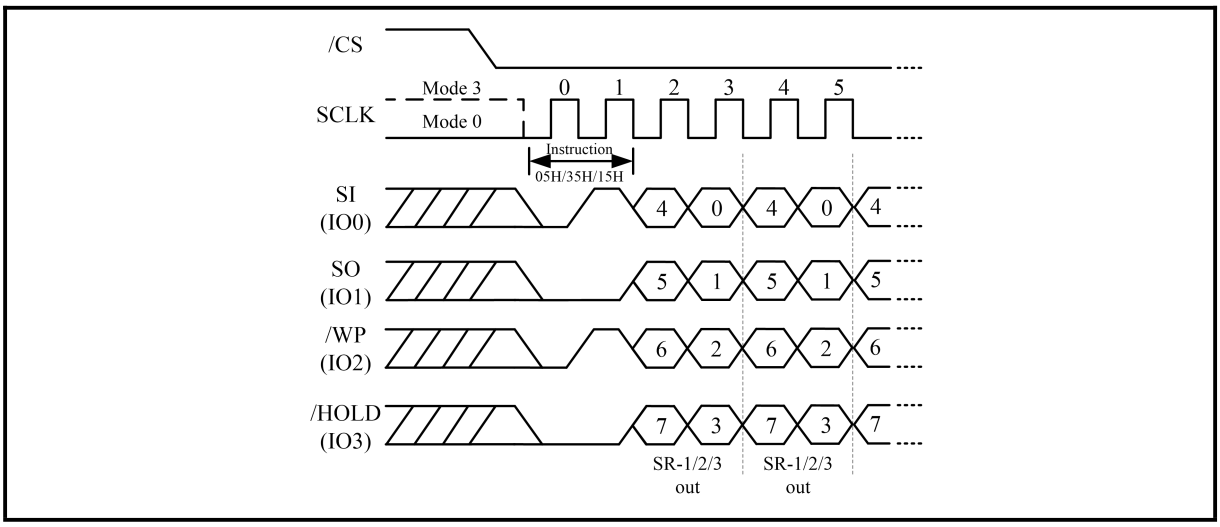


Figure 12. Read Status Register Sequence Diagram (QPI Mode)



7.1.5 Write Status Register (01H or 31H or 11H)

The Write Status Register instruction allows the Status Registers to be written. The Status Register-1 can be written by the Write Status Register 01h instruction; The Status Register-2 be written by the Write Status Register 01h or 31h instruction; Status Register-3 can be written by the Write Status Register 11h instruction. When the Write Status Register instruction 01h is followed by 1 byte data, the data will be written to Status Register-1. When the Write Status Register instruction 01h is followed by 2 bytes of data, the first byte data will be written to Status Register-1, and the second byte data will be written to Status Register-2; And Write Status Register instruction 31h or 11h can only follow 1 byte data, the data will be written to Status Register-2、Status Register-3 respectively. The writable Status Register bits include: SRP0, BP[4:0] in Status Register-1; CMP, LB[3:1], QE, SRP1 in Status Register- 2; DRV1, DRV0, Hold/RST in Status Register- 3. All other Status Register bit locations are read-only and will not be affected by the Write Status Register instruction. LB[3:1] are non-volatile OTP bits, once it is set to 1, it cannot be cleared to 0.

The Write Status Register instruction allows new values to be written to the Status Register. Before it can be accepted, a Write Enable or Write Enable For Volatile SR instruction must previously have been executed After the Write Enable instruction has been decoded and executed, the device sets the Write Enable Latch (WEL).

The Write Status Register instruction has no effect on S15 (SUS1), S10 (SUS2), S1 (WEL) and S0 (WIP) of the Status Register. /CS must be driven high after the 8 or 16 bit of the data byte has been latched in. If not, the Write Status Register (WRSR) instruction is not executed. As soon as /CS is driven high, the self-timed Write Status Register cycle (whose duration is tW) is initiated. While the Write Status Register cycle is in progress, the Status Register may still be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Write Status Register cycle, and is 0 when it is completed. When the cycle is completed, the Write Enable Latch (WEL) is reset.

The Write Status Register instruction allows the user to change the values of the Block Protect (BP4, BP3, BP2, BP1, and BP0) bits, to define the size of the area. The Write Status Register (WRSR) instruction also allows the user to set or reset the Status Register Protect (SRP1 and SRP0) bits in accordance with the Write Protect (/WP) signal. The Status Register Protect (SRP1 and SRP0) bits and Write Protect (/WP) signal allow the device to be put in the Hardware Protected Mode. The Write Status Register instruction is not executed once the Hardware Protected Mode is entered.

The sequence of issuing WRSR instruction is: /CS goes low→ sending WRSR instruction code→ Status Register data on SI→/CS goes high.

The /CS must go high exactly at the 8 bits or 16 bits data boundary; otherwise, the instruction will be rejected and not executed. The self-timed Write Status Register cycle time (tW) is initiated as soon as Chip Select (/CS) goes high. The Write in Progress (WIP) bit still can be checked during the Write Status Register cycle is in progress. The WIP is set 1 during the tW timing, and is set 0 when Write Status Register Cycle is completed, and the Write Enable Latch (WEL) bit is reset.

Figure 13. Write Status Register Sequence Diagram-01H 2byte (SPI Mode)

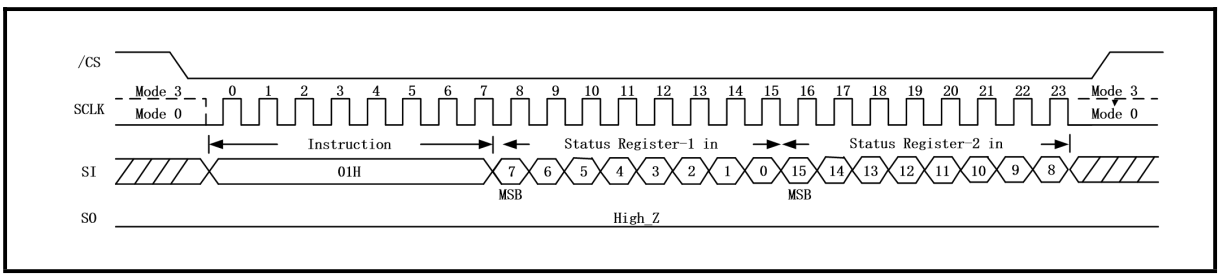


Figure 14. Write Status Register Sequence Diagram-01H 2byte (QPI Mode)

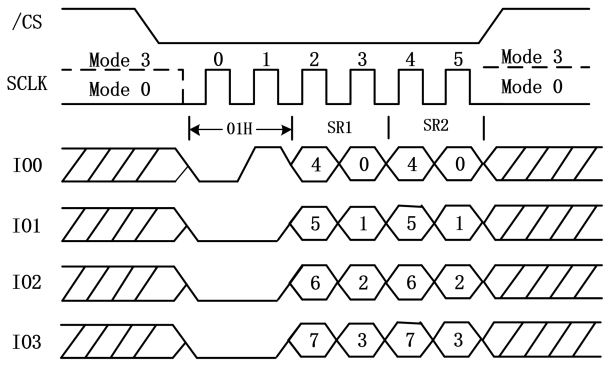


Figure 15. Write Status Register Sequence Diagram-01/31/11H 1byte (SPI Mode)

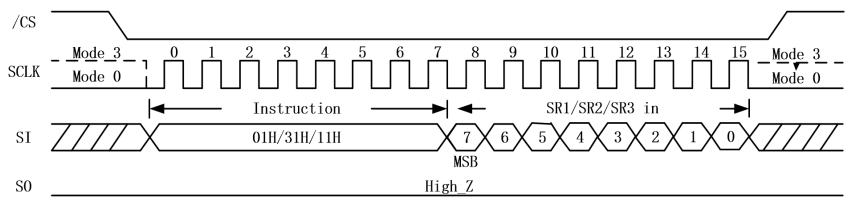
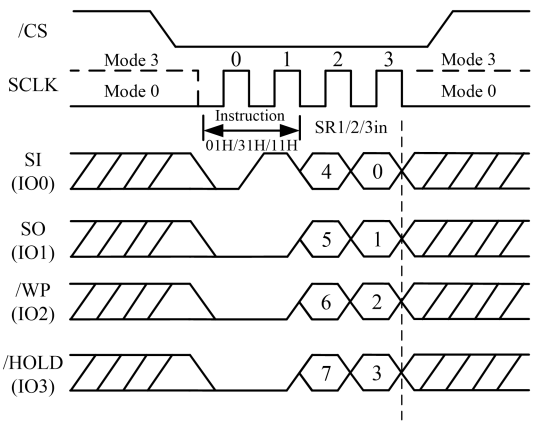


Figure 16. Write Status Register Sequence Diagram-01/31/11H 1byte (QPI Mode)



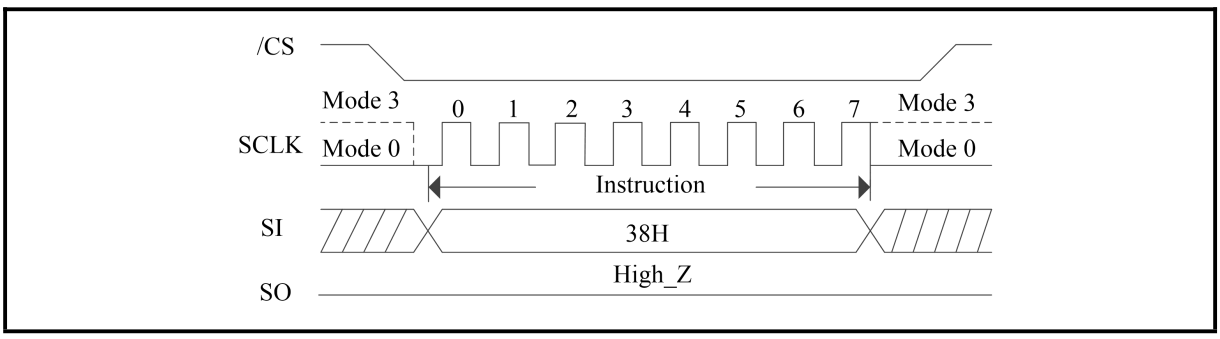
7.1.6 Enter QPI Mode (38H)

The BY25FQ32ES support both Standard/Dual/Quad Serial Peripheral Interface (SPI) and Quad Peripheral Interface (QPI). However, SPI mode and QPI mode cannot be used at the same time. “Enter QPI (38h)” instruction is the only way to switch the device from SPI mode to QPI mode.

Upon power-up, the default state of the device upon is Standard/Dual/Quad SPI mode. This provides full backward compatibility with earlier generations of BY Technology serial flash memories. See Instruction Set ***Table 9*** for all supported SPI instructions. In order to switch the device to QPI mode, the Quad Enable (QE) bit in Status Register-2 must be set to 1 first, and an “Enter QPI (38h)” instruction must be issued. If the Quad Enable (QE) bit is 0, the “Enter QPI (38h)” instruction will be ignored and the device will remain in SPI mode.

When the device is switched from SPI mode to QPI mode, the existing Write Enable and Program/Erase Suspend status, and the Wrap Length setting will remain unchanged.

Figure 17. Enter QPI Mode (SPI Mode)

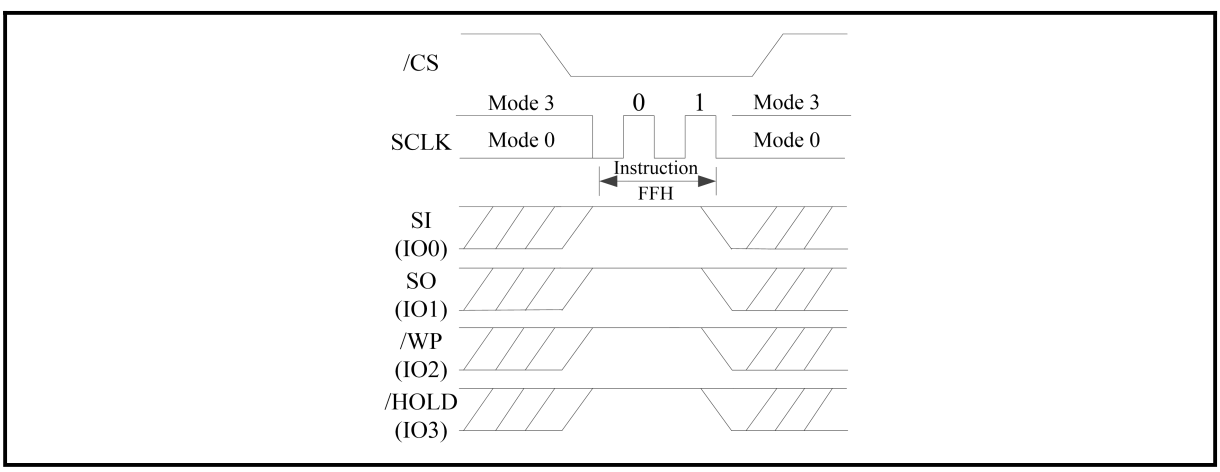


7.1.7 Exit QPI Mode (FFH)

In order to exit the QPI mode and return to the Standard/Dual/Quad SPI mode, an “Exit QPI (FFh)” instruction must be issued.

When the device is switched from QPI mode to SPI mode, the existing Write Enable Latch (WEL) and Program/Erase Suspend status, and the Wrap Length setting will remain unchanged.

Figure 18. Exit QPI Mode (QPI Mode)



7.1.8 Enable Reset (66H) and Reset Device (99H)

Because of the small package and the limitation on the number of pins, the BY25FQ32ES provides a software reset instruction instead of a dedicated RESET pin. Once the software reset instruction is accepted, any on-going internal operations will be terminated and the device will return to its default power-on state and lose all the current volatile settings, such as Volatile Status Register bits, Write Enable Latch (WEL) status, Program/Erase Suspend status, Continuous Read Mode bit setting (M7-M0) and Wrap Bit setting (W6-W4).

To avoid accidental reset, both “Enable Reset (66h)” and “Reset (99h)” instructions must be issued in sequence. Any other instructions other than “Reset (99h)” after the “Enable Reset (66h)” instruction will disable the “Reset Enable” state. A new sequence of “Enable Reset (66h)” and “Reset (99h)” is needed to reset the device. Once the Reset instruction is accepted by the device, the device will take approximately 300us to reset. During this period, no instruction will be accepted.

The Enable Reset (66h) and Reset (99h) instruction sequence is shown in ***Figure 19-Figure 20***.

Data corruption may happen if there is an on-going or suspended internal Erase or Program operation when Reset instruction sequence is accepted by the device. It is recommended to check the BUSY bit and the SUS bit in Status Register before issuing the Reset instruction sequence.

Figure 19. Enable Reset (66h) and Reset (99h) Instruction Sequence (SPI Mode)

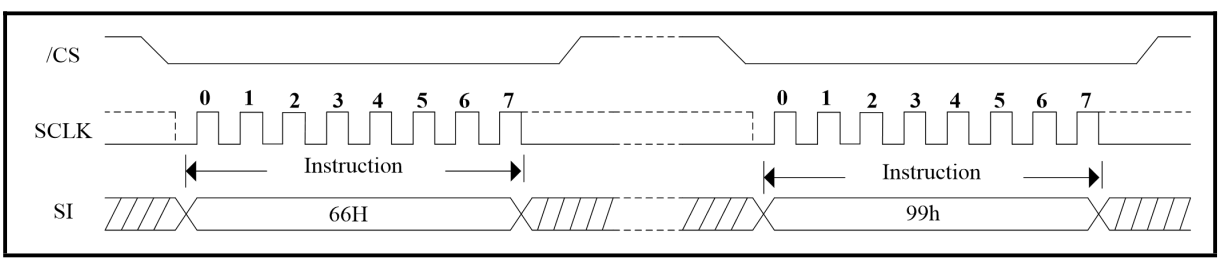
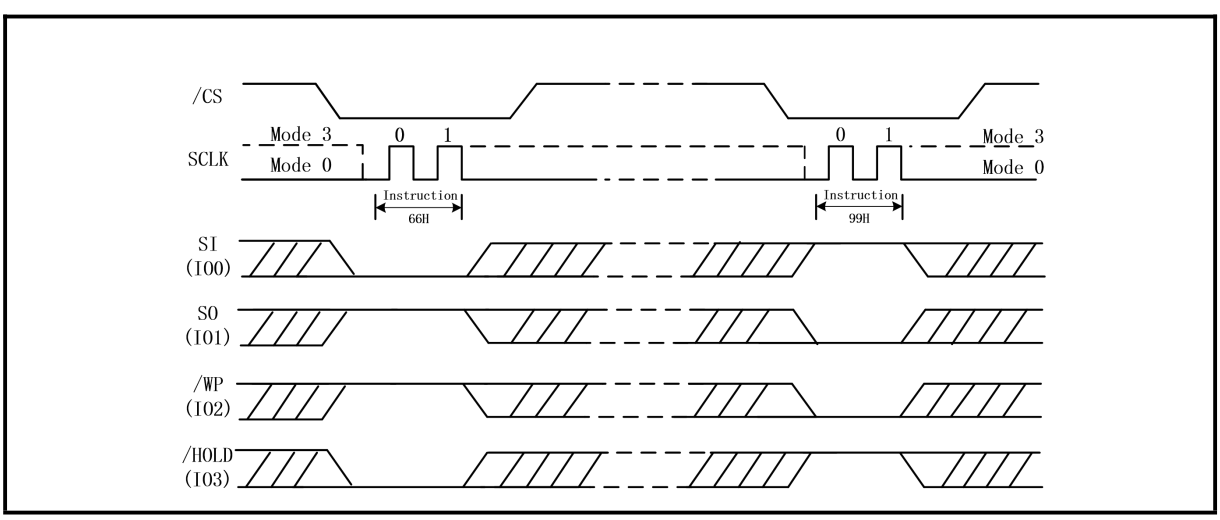


Figure 20. Enable Reset (66h) and Reset (99h) Instruction Sequence (QPI Mode)

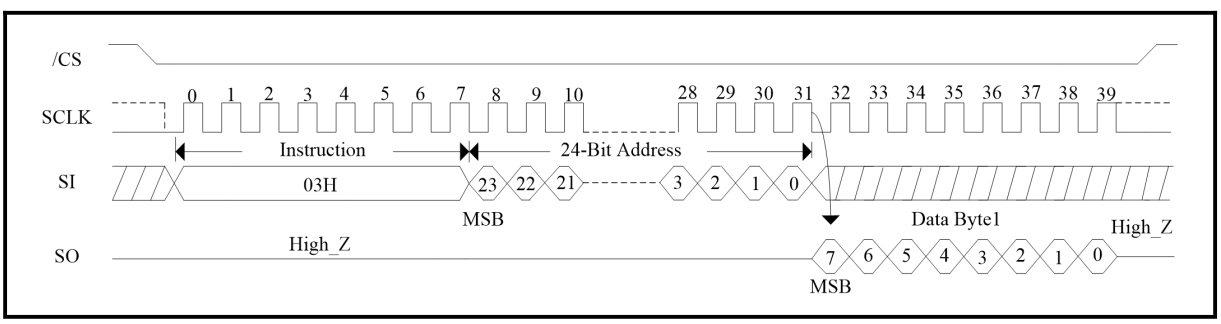


7.2 Read Instructions

7.2.1 Read Data (03H)

See ***Figure 21***, the Read Data Bytes (READ) instruction is followed by a 3-byte address (A23-A0), each bit being latched-in during the rising edge of SCLK. Then the memory content, at that address, is shifted out on SO, each bit being shifted out, at a Max frequency fR, during the falling edge of SCLK. The address is automatically incremented to the next higher address after each byte of data is shifted out allowing for a continuous stream of data. This means that the entire memory can be accessed with a single instruction as long as the clock continues. The instruction is completed by driving /CS high. The whole memory can be read with a single Read Data Bytes (READ) instruction. Any Read Data Bytes (READ) instruction, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

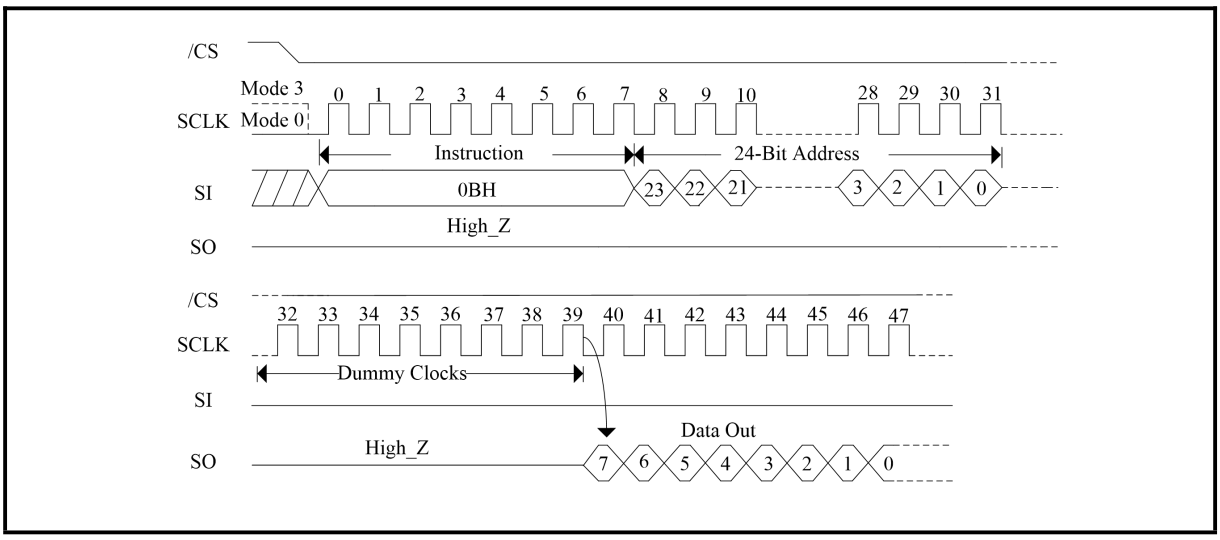
Figure 21. Read Data Bytes Sequence Diagram (SPI Mode only)



7.2.2 Fast Read (0BH)

See ***Figure 22***, the Read Data Bytes at Higher Speed (Fast Read) instruction is for quickly reading data out. It is followed by a 3-byte address (A23-A0) and a dummy byte, each bit being latched-in during the rising edge of SCLK. Then the memory content, at that address, is shifted out on SO, each bit being shifted out, at a Max frequency F_R, during the falling edge of SCLK. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out.

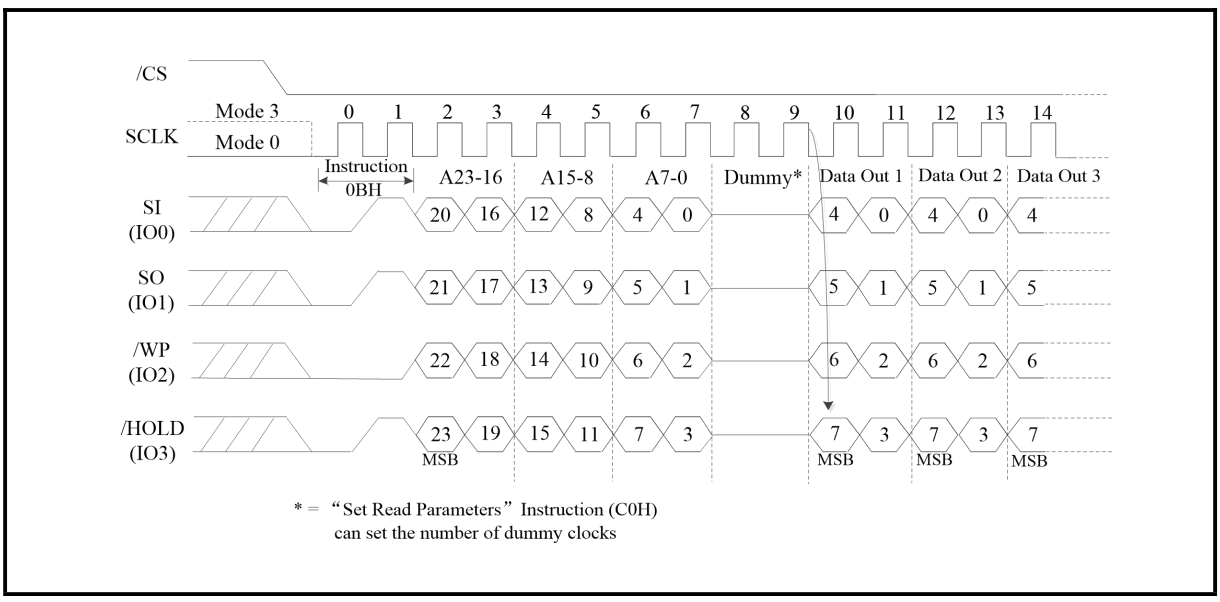
Figure 22. Fast Read Sequence Diagram (SPI Mode)



Fast Read (0Bh) in QPI Mode

The Fast Read instruction is also supported in QPI mode. When QPI mode is enabled, the number of dummy clocks is configured by the “Set Read Parameters (C0h)” instruction to accommodate a wide range of applications with different needs for either maximum Fast Read frequency or minimum data access latency. Depending on the Read Parameter Bits P[5:4] setting, the number of dummy clocks can be configured as either 4, 6, 8 or 10. The default number of dummy clocks upon power up or after a Reset instruction is 4.

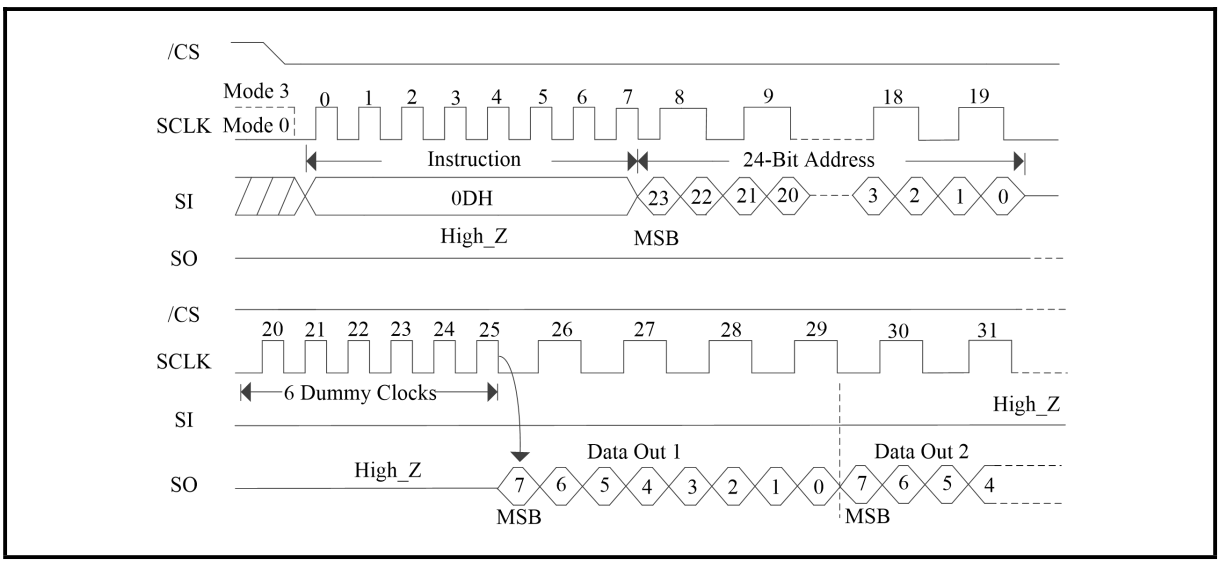
Figure 23. Fast Read Sequence Diagram (QPI Mode Mode)



7.2.3 DTR Fast Read (0DH)

The DTR Fast Read instruction is similar to the Fast Read instruction except that the 24/32-bit address input and the data output requires DTR (Double Transfer Rate) operation. This is accomplished by adding six “dummy” clocks after the 24-bit address as shown in ***Figure 24***. The dummy clocks allow the devices internal circuits additional time for setting up the initial address. During the dummy clocks the data value on the SO pin is a “don’t care”.

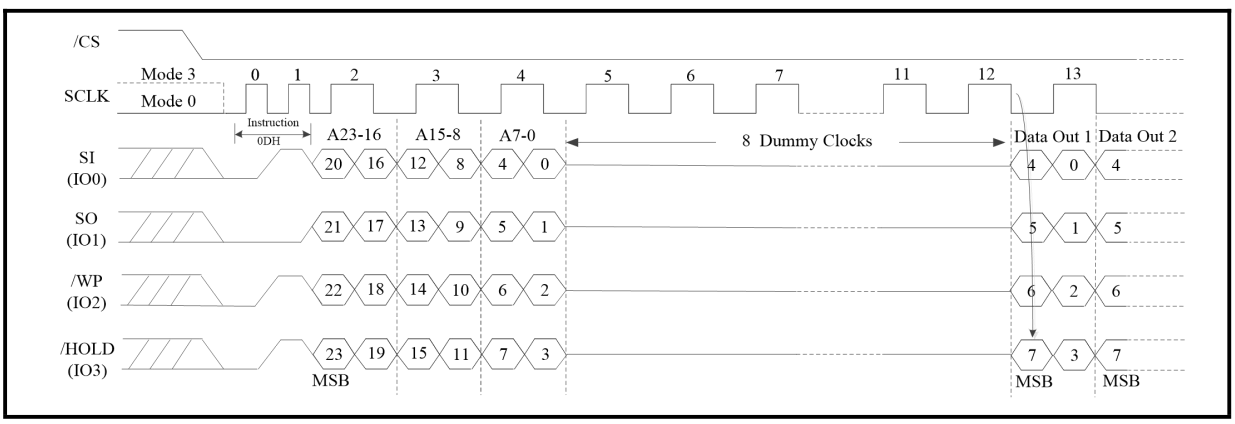
Figure 24. DTR Fast Read (SPI Mode)



DTR Fast Read (0Dh) in QPI Mode

The DTR Fast Read instruction is also supported in QPI mode.

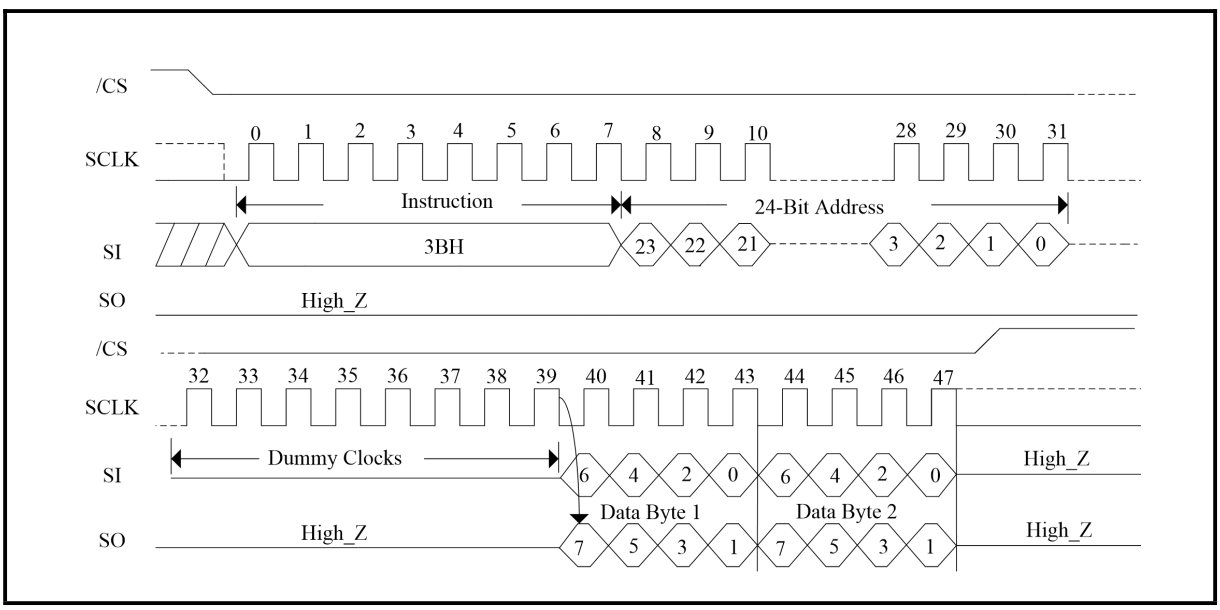
Figure 25. DTR Fast Read (QPI Mode)



7.2.4 Dual Output Fast Read (3BH)

See ***Figure 26***, the Dual Output Fast Read instruction is followed by 3-byte address (A23-A0) and a dummy byte, each bit being latched in during the rising edge of SCLK, then the memory contents are shifted out 2-bit per clock cycle from SI and SO. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out.

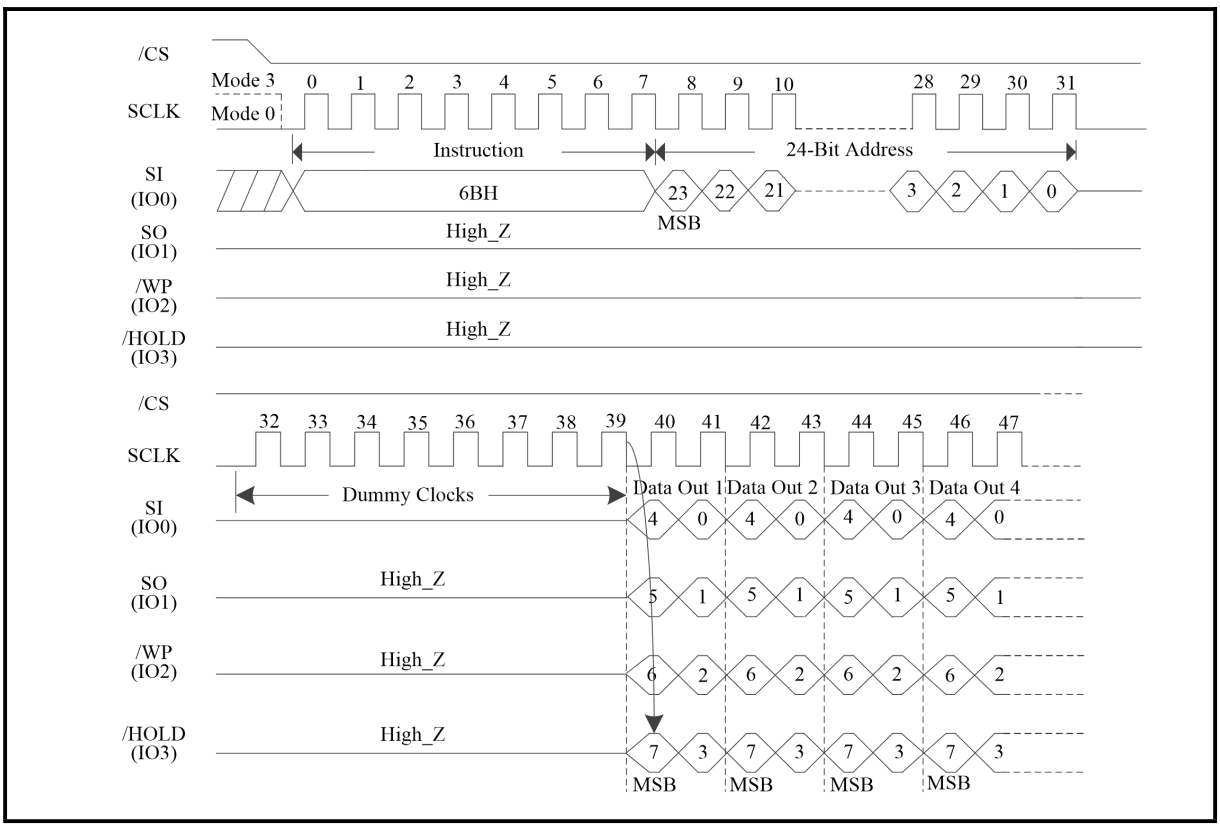
Figure 26. Dual Output Fast Read Sequence Diagram (SPI Mode only)



7.2.5 Quad Output Fast Read (6BH)

See ***Figure 27***, the Quad Output Fast Read instruction is followed by 3-byte address (A23-A0) and a dummy byte, each bit being latched in during the rising edge of SCLK, then the memory contents are shifted out 4-bit per clock cycle from IO3, IO2, IO1 and IO0. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The Quad Enable bit (QE) of Status Register must be set to enable.

Figure 27. Quad Output Fast Read Sequence Diagram (SPI Mode only)



7.2.6 Dual I/O Fast Read (BBH)

See ***Figure 28***, the Dual I/O Fast Read instruction is similar to the Dual Output Fast Read instruction but with the capability to input the 3-byte address (A23-0) and a "Continuous Read Mode" byte 2-bit per clock by SI and SO, each bit being latched in during the rising edge of SCLK, then the memory contents are shifted out 2-bit per clock cycle from SI and SO. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out.

Dual I/O Fast Read with "continuous Read Mode"

The Dual I/O Fast Read instruction can further reduce instruction overhead through setting the "continuous Read Mode" bits (M7-4) after the inputs 3-byte address A23-A0).If the "continuous Read Mode" bits(M5-4)=(1,0),then the next Dual I/O fast Read instruction (after CS/ is raised and then lowered) does not require the BBH instruction code. The instruction sequence is shown in the following ***Figure 28***. If the "continuous Read Mode" bits (M5-4) does not equal (1,0), the next instruction requires the first BBH instruction code, thus returning to normal operation. A "continuous Read Mode" Reset instruction can be used to reset (M5-4) before issuing normal instruction.

Figure 28. Dual I/O Fast Read Sequence Diagram (Initial instruction or previous (M5-4)≠(1,0) , SPI Mode only)

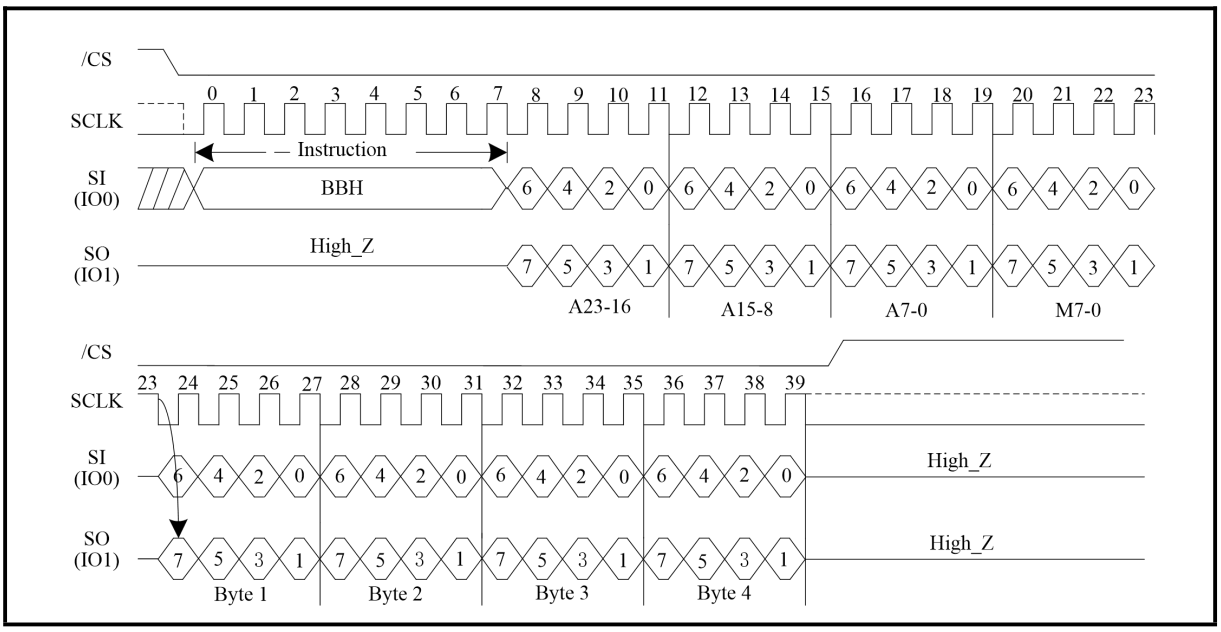
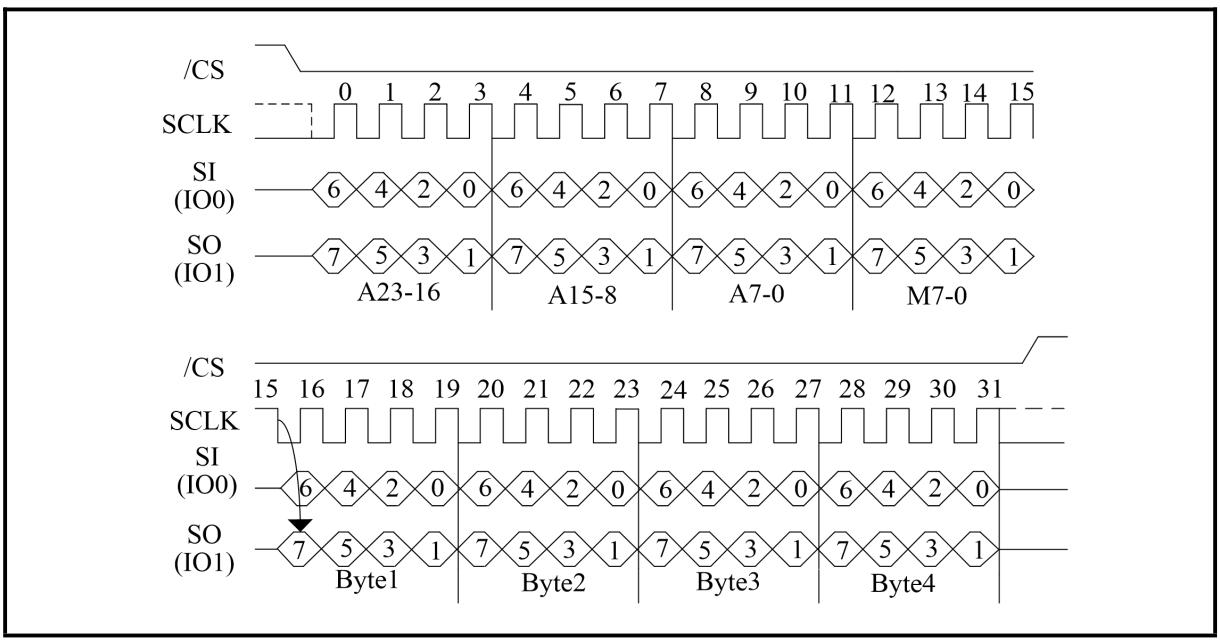


Figure 29. Dual I/O Fast Read Sequence Diagram (Previous instruction set (M5-4) =(1,0) , SPI Mode only)



7.2.7 DTR Fast Read Dual I/O (BDH)

The DTR Fast Read Dual I/O (BDh) instruction allows for improved random access while maintaining two IO pins, IO0 and IO1. It is similar to the Fast Read Dual Output (3Bh) instruction but with the capability to input the Address bits (A23-0) two bits per clock.

DTR Fast Read Dual I/O with "Continuous Read Mode"

The DTR Fast Read Dual I/O instruction can further reduce instruction overhead through setting the "Continuous Read Mode" bits (M7-0) after the input Address bits (A23-0), as shown in ***Figure 30***. The upper nibble of the (M7-4) controls the length of the next Fast Read Dual I/O instruction through the inclusion or exclusion of the first byte instruction code. The lower nibble bits of the (M3-0) are don't care ("x"). However, the IO pins should be high-impedance prior to the falling edge of the first data out clock.

If the "Continuous Read Mode" bits M5-4 = (1,0), then the next Fast Read Dual I/O instruction (after /CS is raised and then lowered) does not require the BDh instruction code, as shown in ***Figure 31***. This reduces the instruction sequence by eight clocks and allows the Read address to be immediately entered after /CS is asserted low. If the "Continuous Read Mode" bits M5-4 do not equal to (1,0), the next instruction (after /CS is raised and then lowered) requires the first byte instruction code, thus returning to normal operation.

Figure 30. DTR Fast Read Dual I/O (SPI Mode only; Initial instruction or previous M5-4≠10)

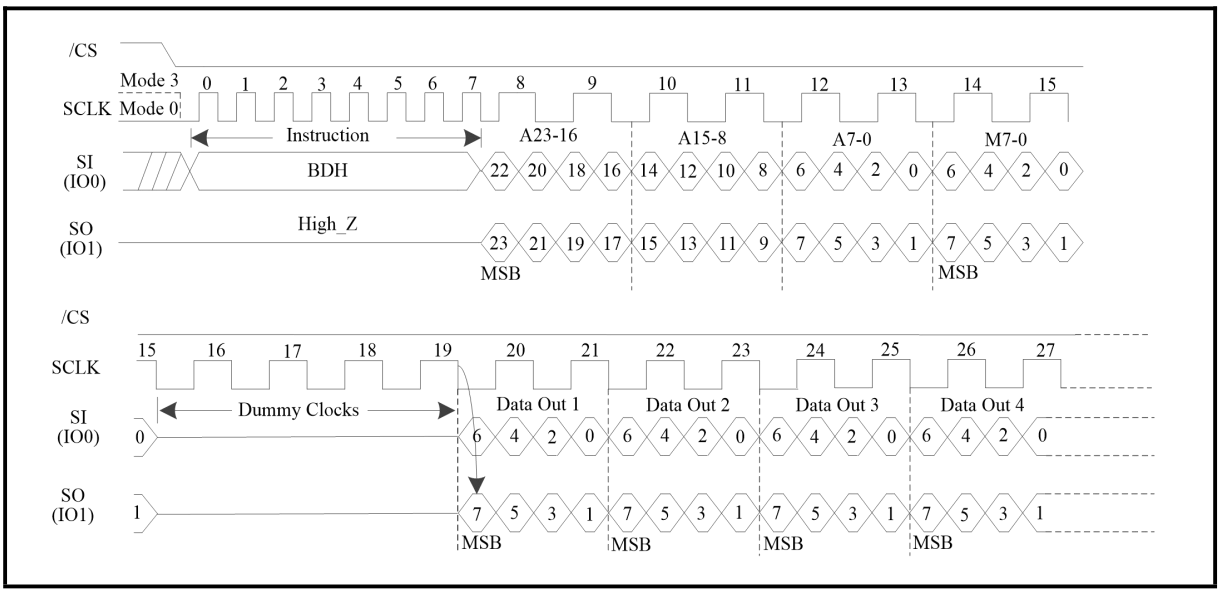
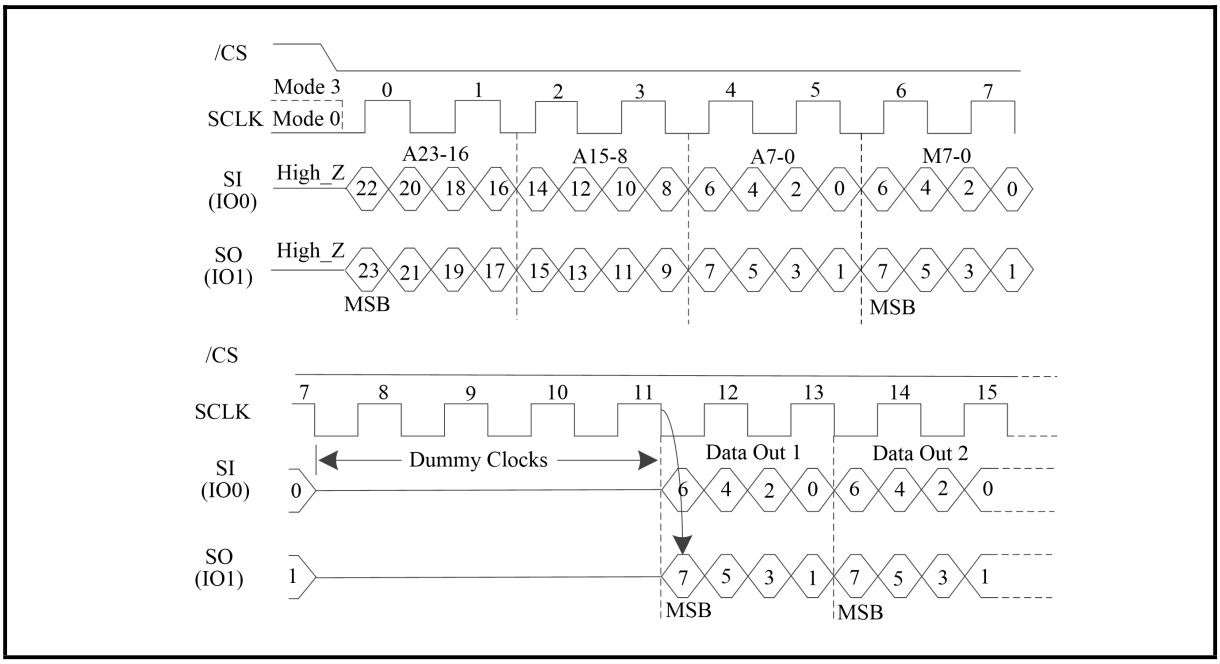


Figure 31. DTR Fast Read Dual I/O (SPI Mode only; Previous instruction set M5-4=10)



7.2.8 Quad I/O Fast Read (EBH)

See ***Figure 32-Figure 33***, the Quad I/O Fast Read instruction is similar to the Dual I/O Fast Read instruction but with the capability to input the 3-byte address (A23-0) and a "Continuous Read Mode" byte and 4-dummy clock 4-bit per clock by IO0, IO1, IO3, IO4, each bit being latched in during the rising edge of SCLK, then the memory contents are shifted out 4-bit per clock cycle from IO0, IO1, IO2, IO3. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The Quad Enable bit (QE) of Status Register must be set to enable for the Quad I/O Fast read instruction.

Quad I/O Fast Read with "Continuous Read Mode"

The Quad I/O Fast Read instruction can further reduce instruction overhead through setting the "Continuous Read Mode" bits (M7-0) after the input Address bits (A23-0), If the "Continuous Read Mode" bits (M5-4)= (1,0), then the next Fast Read Quad I/O instruction(after /CS is raised and then lowered) does not require the EBH instruction code. If the "Continuous Read Mode" bits M5-4 do not equal to (1,0), the next instruction requires the first EBH instruction code, thus returning to normal operation. A "Continuous Read Mode" Reset instruction can also be used to reset (M5-4) before issuing normal instruction.

Figure 32. Quad I/O Fast Read Sequence Diagram (SPI Mode; Initial instruction or previous (M5-4≠(1,0)))

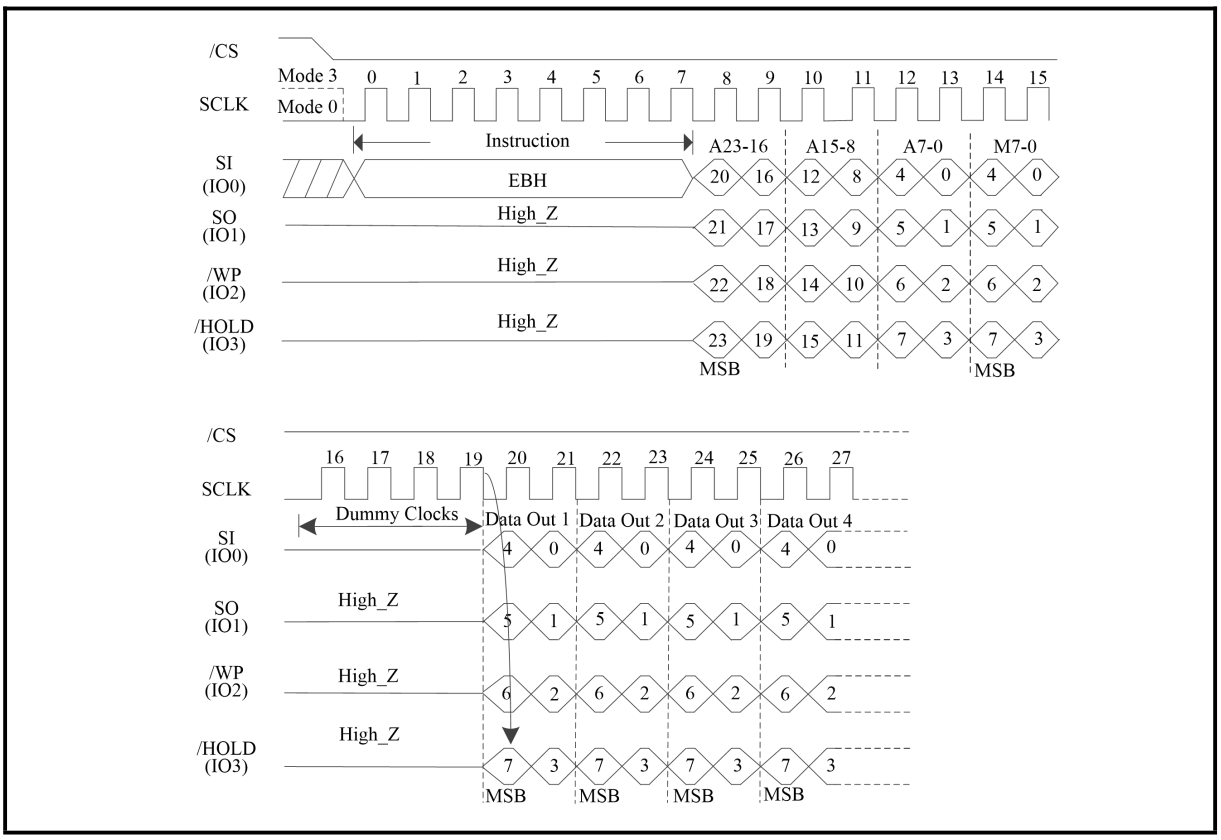
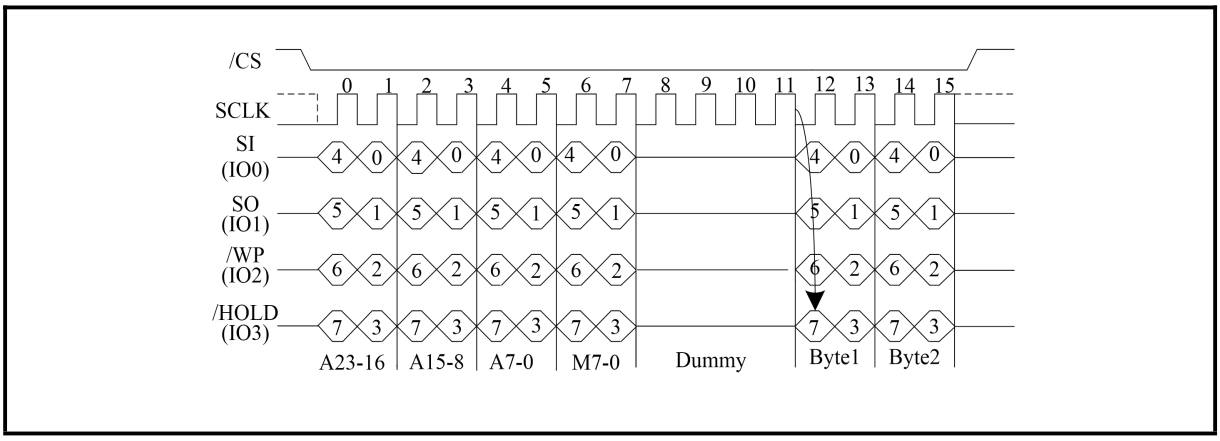


Figure 33. Quad I/O Fast Read Sequence Diagram (SPI Mode; Initial instruction or previous (M5-4=(1,0)))



Quad I/O Fast Read with "8/16/32/64-Byte Wrap Around"

The Quad I/O Fast Read instruction can also be used to access a specific portion within a page by issuing a "Set Burst with Wrap" (77H) instruction prior to EBH. The "Set Burst with Wrap" (77H) instruction can either enable or disable the "Wrap Around" feature for the following EBH instructions. When "Wrap Around" is enabled, the data being accessed can be limited to either an 8, 16, 32 or 64-byte section of a 256-byte page. The output data starts at the initial address specified in the instruction, once it reaches the ending boundary of the 8/16/32/64-byte section, the output will wrap around to the beginning boundary automatically until /CS is pulled high to terminate the instruction.

The Burst with Wrap feature allows applications that use cache to quickly fetch a critical address and then fill the cache afterwards within a fixed length (8/16/32/64-byte) of data without issuing multiple read instructions.

The "Set Burst with Wrap" instruction allows three "Wrap Bits", W6-4 to be set. The W4 bit is used to enable or disable the "Wrap Around" operation while W6-5 are used to specify the length of the wrap around section within a page.

Fast Read Quad I/O (EBh) in QPI Mode

The Fast Read Quad I/O instruction is also supported in QPI mode, as shown in ***Figure 34-Figure 35.*** When QPI mode is enabled, the number of dummy clocks is configured by the "Set Read Parameters (C0h)" instruction to accommodate a wide range of applications with different needs for either maximum Fast Read frequency or minimum data access latency. Depending on the Read Parameter Bits P[5:4] setting, the number of dummy clocks can be configured as either 4, 6, 8 or 10. The default number of dummy clocks upon power up or after a Reset instruction is 4. In QPI mode, the "Continuous Read Mode" bits M7-0 are also considered as dummy clocks. In the default setting, the data output will follow the Continuous Read Mode bits immediately.

"Continuous Read Mode" feature is also available in QPI mode for Fast Read Quad I/O instruction. Please refer to the description on previous pages.

"Wrap Around" feature is not available in QPI mode for Fast Read Quad I/O instruction. To perform a read operation with fixed data length wrap around in QPI mode, a dedicated "Burst Read with Wrap" (0Ch) instruction must be used.

Figure 34. Quad I/O Fast Read Sequence Diagram (QPI Mode Mode; Initial instruction or previous (M5-4≠(1,0)))

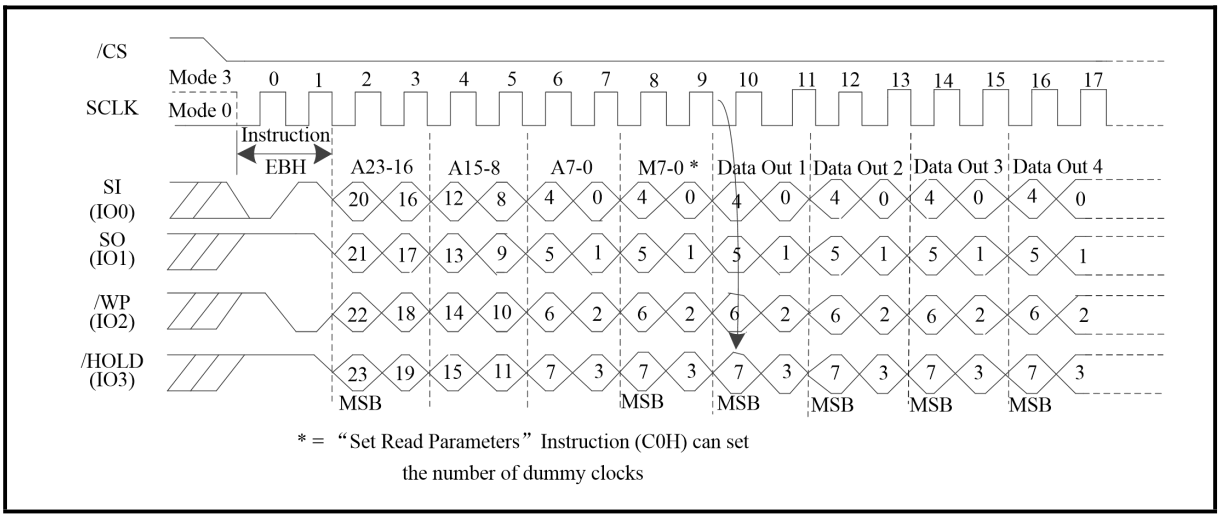
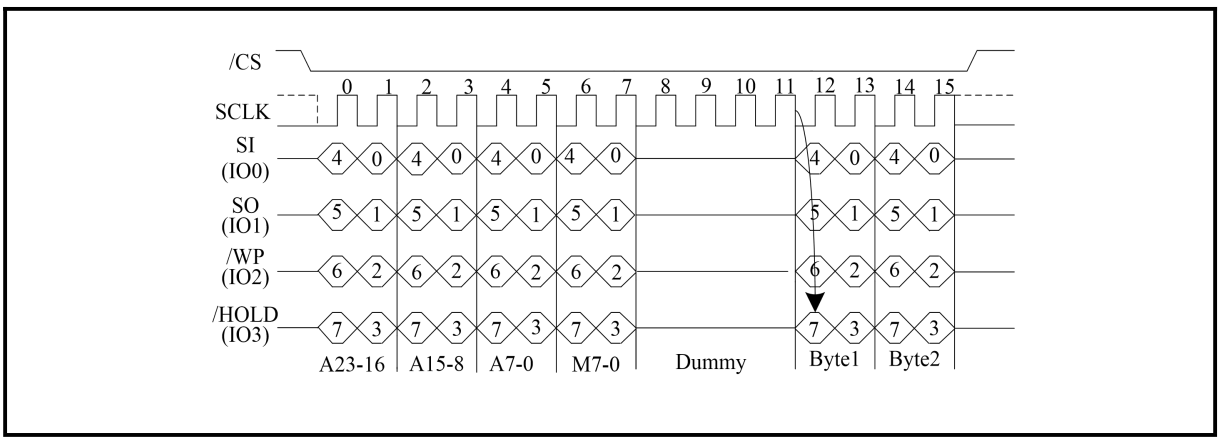


Figure 35. Quad I/O Fast Read Sequence Diagram (QPI Mode Mode; Initial instruction or previous (M5-4=(1,0)))



7.2.9 DTR Fast Read Quad I/O(EDH)

The DTR Fast Read Quad I/O (EDh) instruction is similar to the Fast Read Dual I/O (BBh) instruction except that address and data bits are input and output through four pins IO0, IO1, IO2 and IO3 and four Dummy clocks are required in SPI mode prior to the data output, as shown in ***Figure 36***. The Quad Enable bit (QE) of Status Register must be set to enable.

DTR Fast Read Quad I/O with "Continuous Read Mode"

The Fast Read Quad I/O instruction can further reduce instruction overhead through setting the "Continuous Read Mode" bits (M7-0) after the input Address bits (A23 -0). The upper nibble of the (M7-4) controls the length of the next Fast Read Quad I/O instruction through the inclusion or exclusion of the first byte instruction code. The lower nibble bits of the (M3-0) are don't care ("x"). However, the IO pins should be high-impedance prior to the falling edge of the first data out clock.

If the "Continuous Read Mode" bits M5-4 = (1,0), then the next Fast Read Quad I/O instruction (after /CS is raised and then lowered) does not require the EDh instruction code. This reduces the instruction sequence by eight clocks and allows the Read address to be immediately entered after /CS is asserted low. If the "Continuous Read Mode" bits M5-4 do not equal to (1,0), the next instruction (after /CS is raised and then lowered) requires the first byte instruction code, thus returning to normal operation.

Figure 36. DTR Fast Read Quad I/O (SPI Mode; Initial instruction or previous (M5-4≠(1,0)))

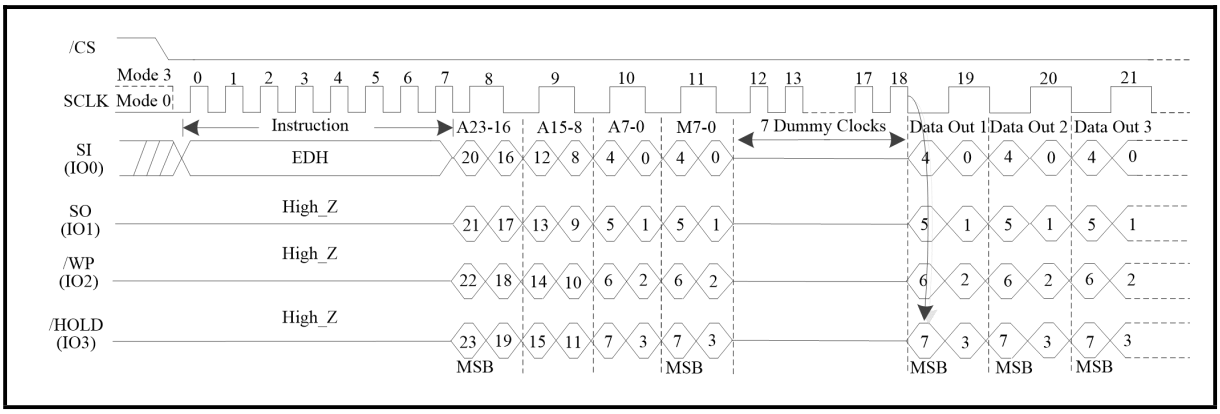
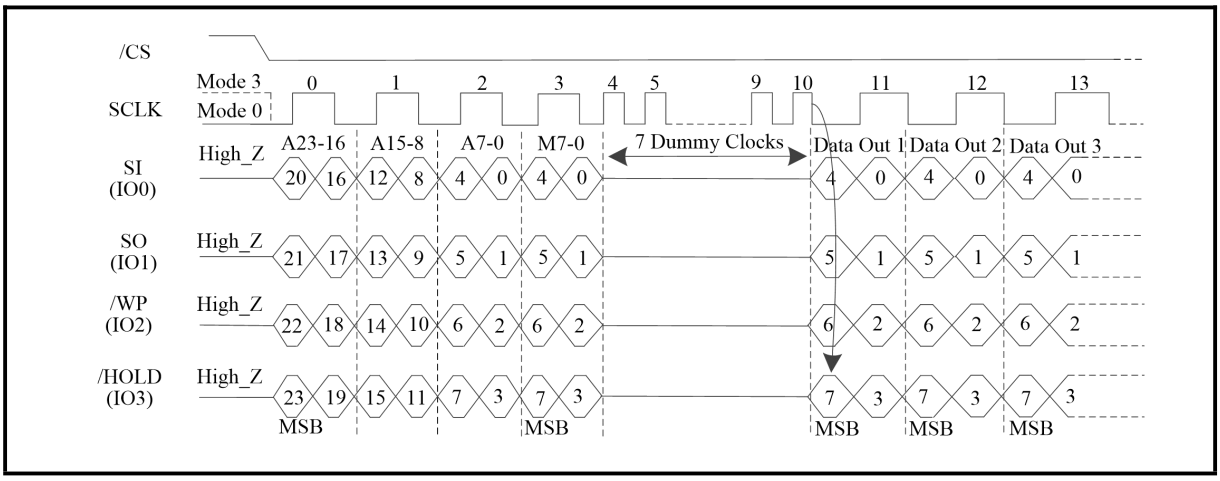


Figure 37. DTR Fast Read Quad I/O (SPI Mode; Initial instruction or previous (M5-4=(1,0)))



DTR Fast Read Quad I/O with "8/16/32/64-Byte Wrap Around" in Standard SPI mode

The Fast Read Quad I/O instruction can also be used to access a specific portion within a page by issuing a "Set Burst with Wrap" (77h) instruction prior to EDh. The "Set Burst with Wrap" (77h) instruction

can either enable or disable the “Wrap Around” feature for the following EDh instructions. When “Wrap Around” is enabled, the data being accessed can be limited to either an 8, 16, 32 or 64-byte section of a 256-byte page. The output data starts at the initial address specified in the instruction, once it reaches the ending boundary of the 8/16/32/64-byte section, the output will wrap around to the beginning boundary automatically until /CS is pulled high to terminate the instruction.

The Burst with Wrap feature allows applications that use cache to quickly fetch a critical address and then fill the cache afterwards within a fixed length (8/16/32/64-byte) of data without issuing multiple read instructions.

The “Set Burst with Wrap” instruction allows three “Wrap Bits”, W6-4 to be set. The W4 bit is used to enable or disable the “Wrap Around” operation while W6-5 are used to specify the length of the wrap around section within a page.

DTR Fast Read Quad I/O (EDh) in QPI Mode

The DTR Fast Read Quad I/O instruction is also supported in QPI mode, as shown in ***Figure 38***. In QPI mode, the “Continuous Read Mode” can further reduce instruction overhead through setting the “Continuous Read Mode” bits (M7-0) after the input Address bits (A23-0). Please refer to the description on previous pages. If the “Continuous Read Mode” bits (M5-4)= (1,0), then the next Fast Read Quad I/O instruction(after /CS is raised and then lowered) does not require the EDH instruction code, The instruction sequence is shown in the followed Figure. If the “Continuous Read Mode” bits M5-4 do not equal to (1,0), the next instruction requires the first EDH instruction code, thus returning to normal operation. A “Continuous Read Mode” Reset instruction can also be used to reset (M5-4) before issuing normal instruction.

Figure 38. DTR Fast Read Quad I/O (QPI Mode; Initial instruction or previous (M5-4≠(1,0)))

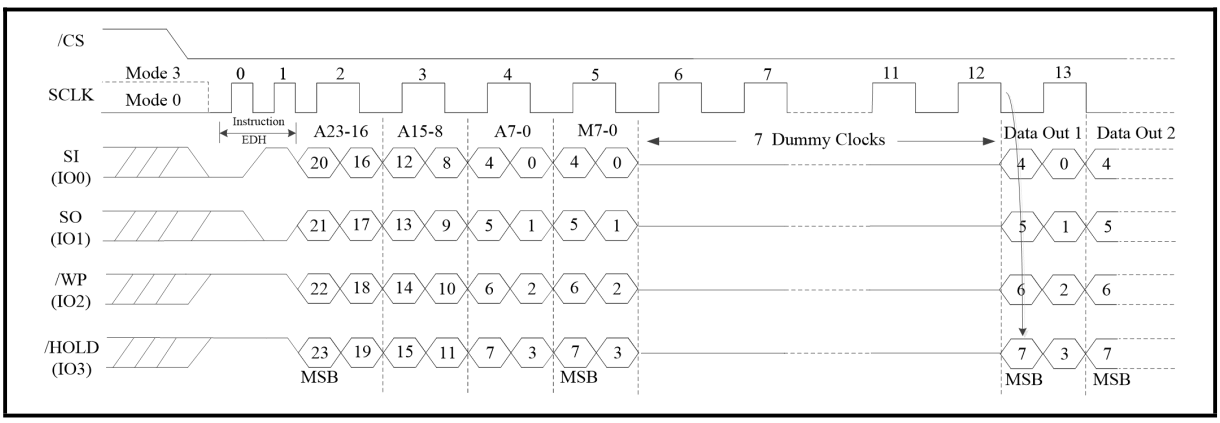
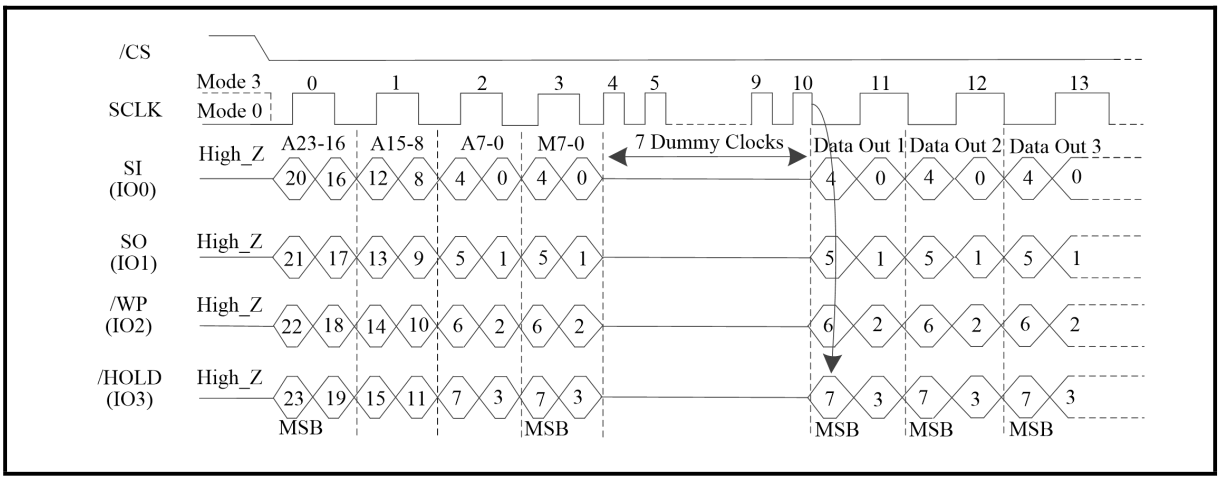


Figure 39. DTR Fast Read Quad I/O (QPI Mode; Initial instruction or previous (M5-4=(1,0)))



7.2.10 Quad I/O Word Fast Read (E7H)

The Quad I/O Word Fast Read instruction is similar to the Quad Fast Read instruction except that the lowest address bit (A0) must equal 0 and 2-dummy clock. The instruction sequence is shown in the followed ***Figure 40-Figure 41***, the first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The Quad Enable bit (QE) of Status Register (S9) must be set to enable for the Quad I/O Word Fast Read instruction. The Quad Enable bit (QE) of Status Register must be set to enable.

Quad I/O Word Fast Read with "Continuous Read Mode"

The Quad I/O Word Fast Read instruction can further reduce instruction overhead through setting the "Continuous Read Mode" bits (M7-0) after the input 3-byte Address bits (A23-0). If the "Continuous Read Mode" bits (M5-4) = (1, 0), then the next Quad I/O Fast Read instruction (after /CS is raised and then lowered) does not require the E7H instruction code, the instruction sequence is shown in the followed ***Figure 41***. If the "Continuous Read Mode" bits M5-4 do not equal to (1,0), the next instruction requires the first E7H instruction code, thus returning to normal operation. A "Continuous Read Mode" Reset instruction can also be used to reset (M5-4) before issuing normal instruction.

Figure 40. Quad I/O Word Fast Read Sequence Diagram (SPI Mode; Initial instruction or previous (M5-4)≠(1,0))

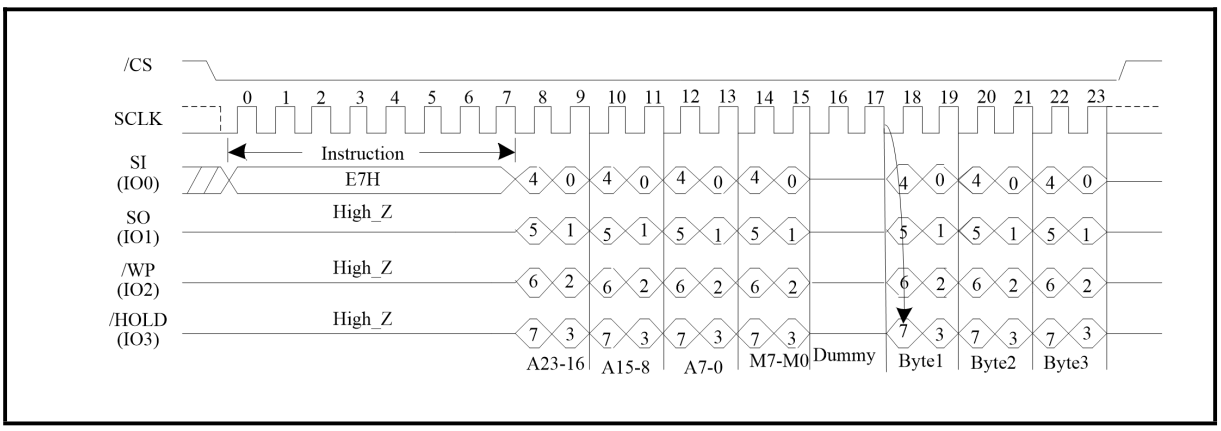
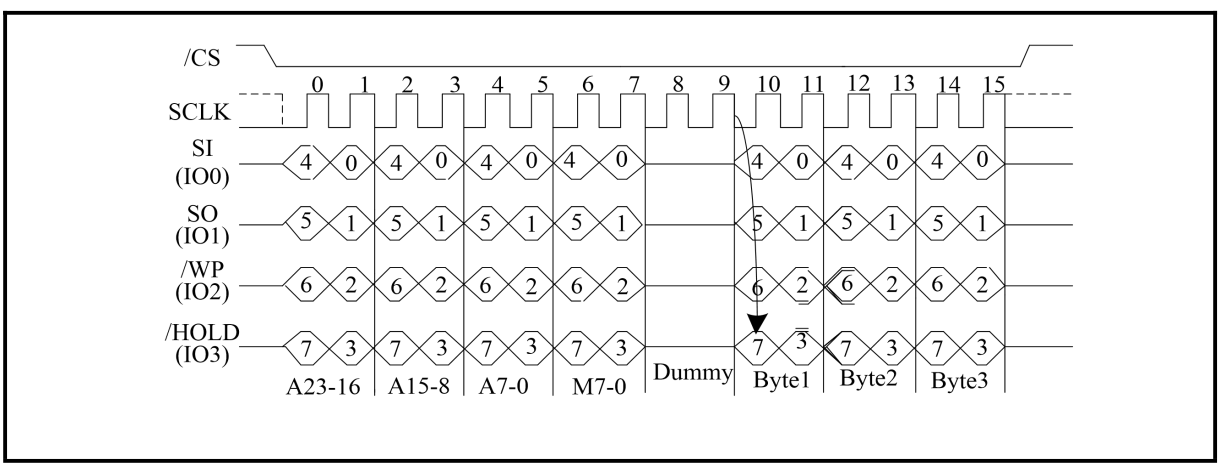


Figure 41. Quad I/O Word Fast Read Sequence Diagram (SPI Mode; Initial instruction or previous (M5-4)=(1,0))



Quad I/O Word Fast Read with "8/16/32/64-Byte Wrap Around" in standard SPI mode

The Quad I/O Fast Read instruction can also be used to access a specific portion within a page by issuing a "Set Burst with Wrap" (77H) instruction prior to E7H. The "Set Burst with Wrap" (77H) instruction can either enable or disable the "Wrap Around" feature for the following E7H instructions. When "Wrap Around" is enabled, the data being accessed can be limited to either an

8, 16, 32 or 64-byte section of a 256-byte page. The output data starts at the initial address specified in the instruction, once it reaches the ending boundary of the 8/16/32/64-byte section, the output will wrap around to the beginning boundary automatically until /CS is pulled high to terminate the instruction.

The Burst with Wrap feature allows applications that use cache to quickly fetch a critical address and then fill the cache afterwards within a fixed length (8/16/32/64-byte) of data without issuing multiple read instructions.

The “Set Burst with Wrap” instruction allows three “Wrap Bits”, W6-4 to be set. The W4 bit is used to enable or disable the “Wrap Around” operation while W6-5 are used to specify the length of the wrap around section within a page.

7.2.11 Set Burst with Wrap (77H)

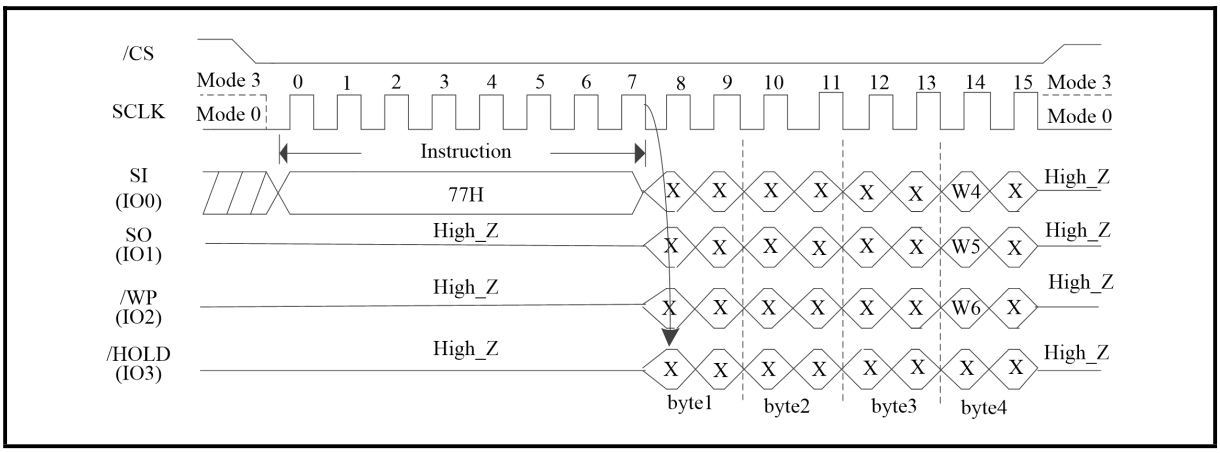
See ***Figure 42,*** The Set Burst with Wrap instruction is used in conjunction with “EBH”, “E7H” instructions to access a fixed length of 8/16/32/64-byte section within a 256-byte page, in standard SPI mode.

The Set Burst with Wrap instruction sequence:/CS goes low ->Send Set Burst with Wrap instruction ->Send24 Dummy bits ->Send 8 bits” Wrap bits”->/CS goes high.

If W6-4 is set by a Set Burst with Wrap instruction, all the following “EBH”, “E7H” instructions will use the W6-4 setting to access the 8/16/32/64-byte section within any page. To exit the “Wrap Around” function and return to normal read operation, another Set Burst with Wrap instruction should be issued to set W4=1. The default value of W4 upon power on is 1.

W6 , W5		W4 = 0		W4 =1 (DEFAULT)	
		Wrap Around	Wrap Length	Wrap Around	Wrap Length
0	0	Yes	8-byte	No	N/A
0	1	Yes	16-byte	No	N/A
1	0	Yes	32-byte	No	N/A
1	1	Yes	64-byte	No	N/A

Figure 42. Set Burst with Wrap Sequence Diagram (SPI Mode only)



7.2.12 Set Read Parameters (C0H)

In QPI mode, to accommodate a wide range of applications with different needs for either maximum read frequency or minimum data access latency, “Set Read Parameters (C0h)” instruction can be used to configure the number of dummy clocks for “0BH~5AH” instructions, as shown in ***Table 11***, and to configure the number of bytes of “Wrap Length” for the “0CH” instruction.

Table 11. Instructions that configurable dummy number

Mode	Instruction	
QPI	Fast Read	0Bh
	Fast Read Quad I/O	EBh
	Burst Read with Wrap	0Ch
	DTR Fast Read	0Dh
	DTR Fast Read Quad I/O	EDh
	DTR Burst Read with Wrap	0Eh
	Read Security Registers	48h
	Read Serial Flash Discoverable Parameter	5Ah

In Standard SPI mode, the “Set Read Parameters (C0h)” instruction is not accepted. The dummy clocks for various Fast Read instructions in Standard/Dual/Quad SPI mode are fixed, please refer to the Instruction ***Table 9*** for details. The “Wrap Length” is set by W5-4 bit in the “Set Burst with Wrap (77h)” instruction. This setting will remain unchanged when the device is switched from Standard SPI mode to QPI mode.

The default “Wrap Length” after a power up or a Reset instruction is 8 bytes, the default number of dummy clocks is 4. The number of dummy clocks is only programmable for “0BH~5AH” instructions in the QPI mode. Whenever the device is switched from SPI mode to QPI mode, the number of dummy clocks should be set again, prior to any “0BH~5AH” instructions.

Table 12. Configuration of the number of dummies for STR instructions

(W/O DQS)

P5 – P4	DUMMY CLOCKS	MAXIMUM READ FREQ. (VCC=2.7V~2.9V)	MAXIMUM READ FREQ. (VCC=3.0V~3.6V)	P1 – P0	WRAP LENGTH
0 0	4 (default)	66 MHz	66 MHz	0 0	8-byte
	14(1)	133 MHz	166MHz		
0 1	6	80 MHz	104MHz	0 1	16-byte
1 0	8	104MHz	133 MHz	1 0	32-byte
1 1	10	133 MHz	166 MHz	1 1	64-byte

(WITH DQS)

P5 – P4	DUMMY CLOCKS	MAXIMUM READ FREQ. (VCC=2.7V~2.9V)	MAXIMUM READ FREQ. (VCC=3.0V~3.6V)	P1 – P0	WRAP LENGTH
0 0	4 (default)	66 MHz	66 MHz	0 0	8-byte
	14(1)	133 MHz	166MHz		
0 1	6	80 MHz	104MHz	0 1	16-byte

1 0	8	104MHz	133 MHz		1 0	32-byte
1 1	10	133 MHz	166 MHz		1 1	64-byte

Note:

1. The 14 dummy is available. Please contact BY Technology.

Table 13. Configuration of the number of dummies for DTR instructions

(W/O DQS)

P5 – P4	DUMMY CLOCKS	MAXIMUM READ FREQ. (VCC=2.7V~2.9V)	MAXIMUM READ FREQ. (VCC=3.0V~3.6V)	P1 – P0	WRAP LENGTH
0 0	6	66 MHz	66 MHz	0 0	8-byte
	16(1)	104 MHz	104MHz		
0 1	8	84 MHz	84 MHz	0 1	16-byte
1 0	10	104 MHz	104MHz	1 0	32-byte
1 1	12	104 MHz	104MHz	1 1	64-byte

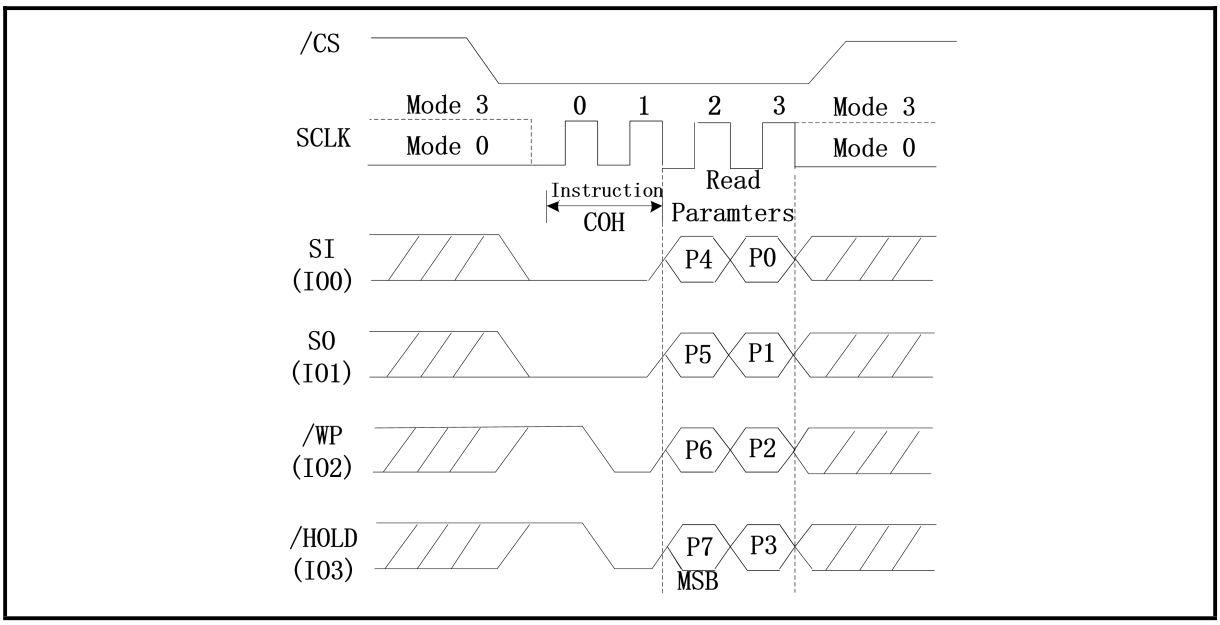
(WITH DQS)

P5 – P4	DUMMY CLOCKS	MAXIMUM READ FREQ. (VCC=2.7V~2.9V)	MAXIMUM READ FREQ. (VCC=3.0V~3.6V)	P1 – P0	WRAP LENGTH
0 0	6	66 MHz	66 MHz	0 0	8-byte
	16(1)	104 MHz	133MHz		
0 1	8	84 MHz	84 MHz	0 1	16-byte
1 0	10	104 MHz	104MHz	1 0	32-byte
1 1	12	104 MHz	133MHz	1 1	64-byte

Note:

1. The 14 dummy is available. Please contact BY Technology.

Figure 43. Burst Read with Wrap (QPI Mode only)

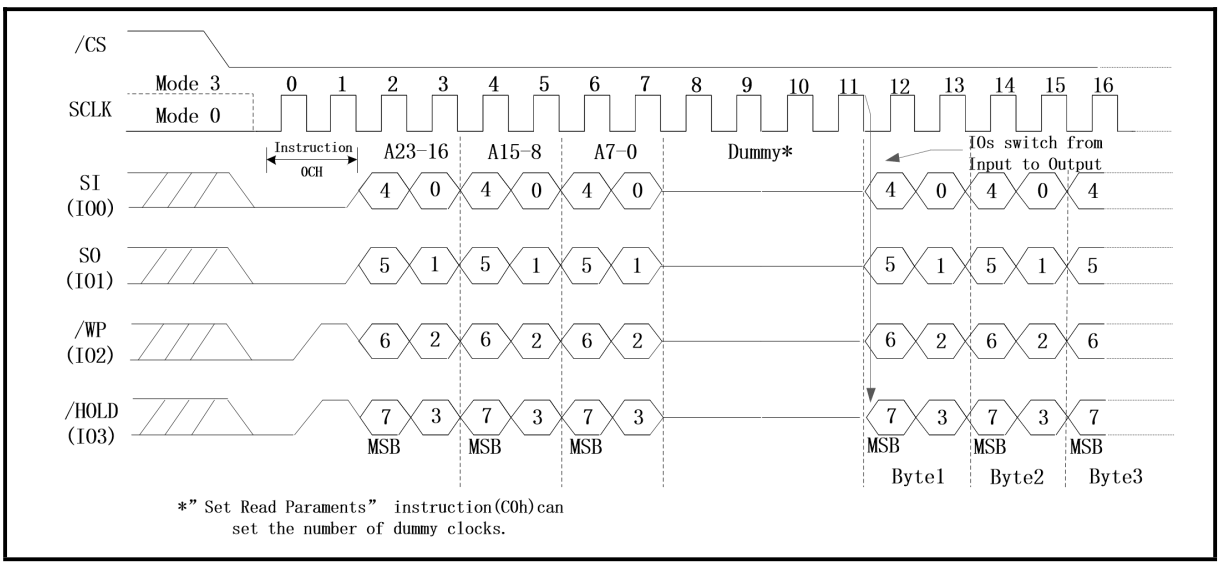


7.2.13 Burst Read with Wrap (0CH)

The “Burst Read with Wrap (0Ch)” instruction provides an alternative way to perform the read operation with “Wrap Around” in QPI mode. The instruction is similar to the “Fast Read (0Bh)” instruction in QPI mode, except the addressing of the read operation will “Wrap Around” to the beginning boundary of the “Wrap Length” once the ending boundary is reached.

The “Wrap Length” and the number of dummy clocks can be configured by the “Set Read Parameters (C0h)” instruction

Figure 44. Burst Read with Wrap (QPI Mode only)

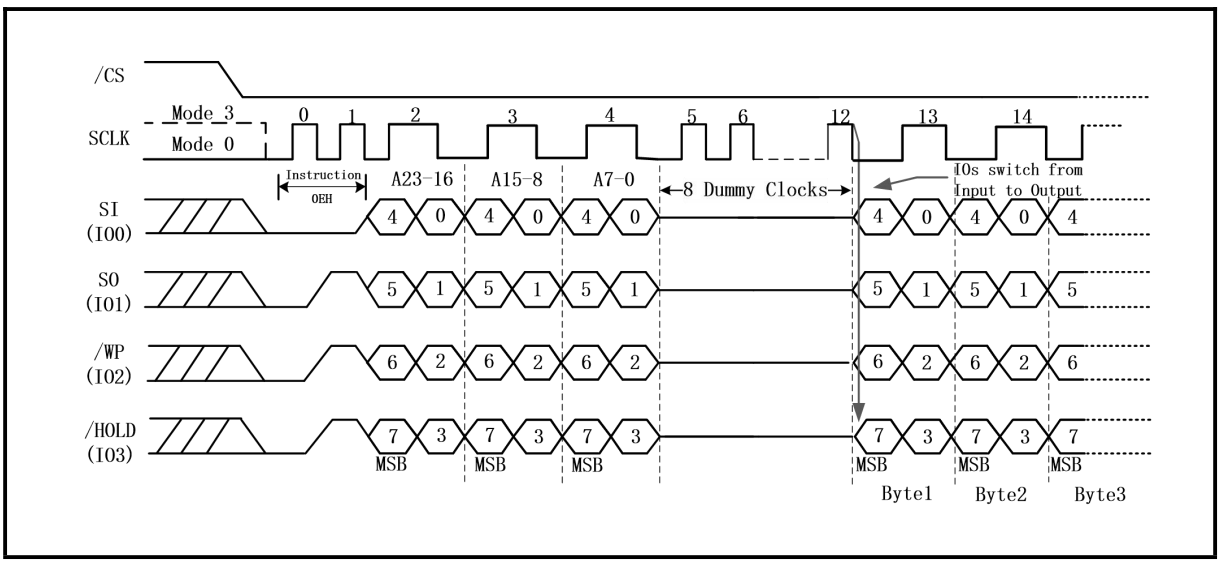


7.2.14 DTR Burst Read with Wrap (0EH)

The “DTR Burst Read with Wrap (0Eh)” instruction provides an alternative way to perform the read operation with “Wrap Around” in QPI mode. The instruction is similar to the “Fast Read (0Bh)” instruction in QPI mode, except the addressing of the read operation will “Wrap Around” to the beginning boundary of the “Wrap Length” once the ending boundary is reached.

The “Wrap Length” can be configured by the “Set Read Parameters (C0h)” instruction.

Figure 45. DTR Burst Read with Wrap (QPI Mode only)



7.3 ID and Security Instructions

7.3.1 Read Manufacture ID/ Device ID (90H)

See ***Figure 46-Figure 47***, The Read Manufacturer/Device ID instruction is an alternative to the Release from Power-Down/Device ID instruction that provides both the JEDEC assigned Manufacturer ID and the specific Device ID.

The instruction is initiated by driving the /CS pin low and shifting the instruction code “90H” followed by a 24-bit address (A23-A0) of 000000H. If the 24-bit address is initially set to 000001H, the Device ID will be read first.

Figure 46. Read Manufacture ID/ Device ID Sequence Diagram (SPI Mode)

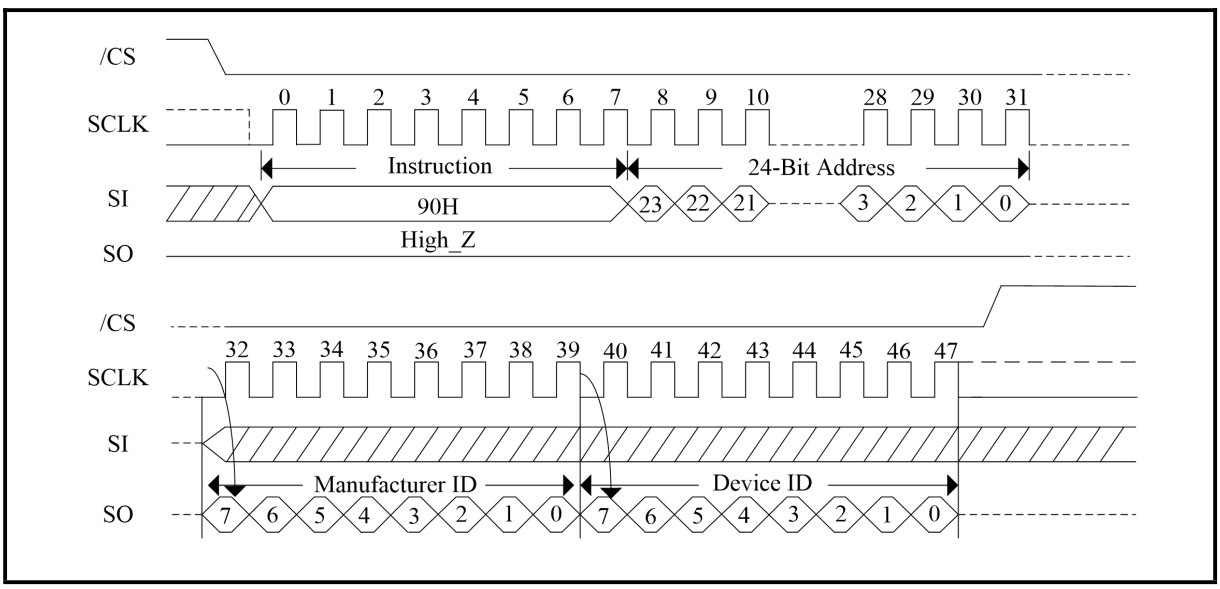
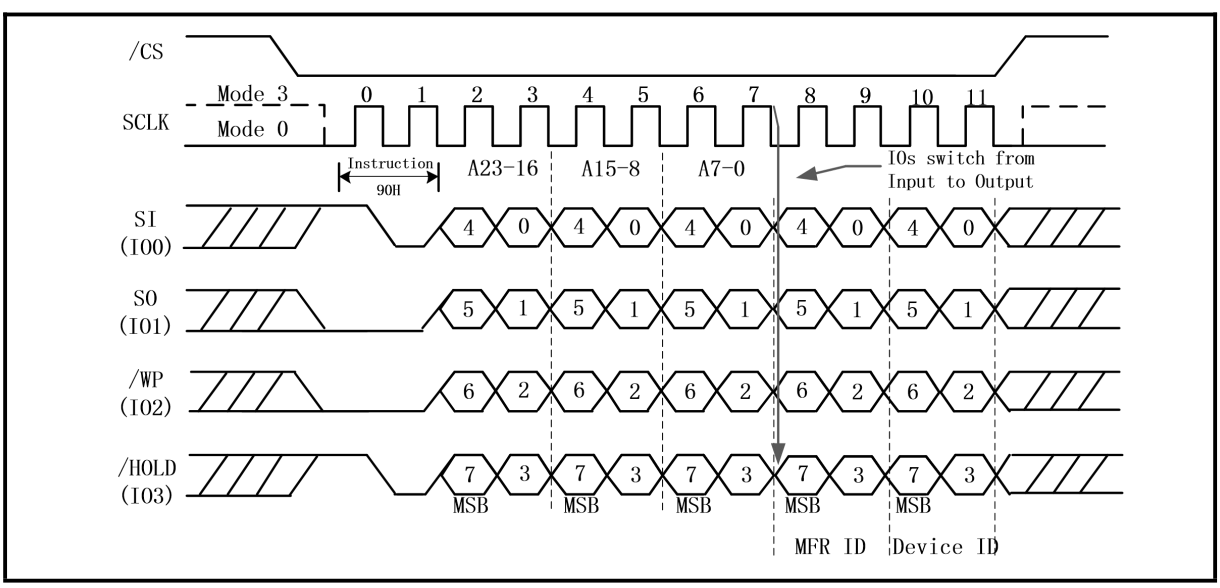


Figure 47. Read Manufacture ID/ Device ID Sequence Diagram (QPI Mode)

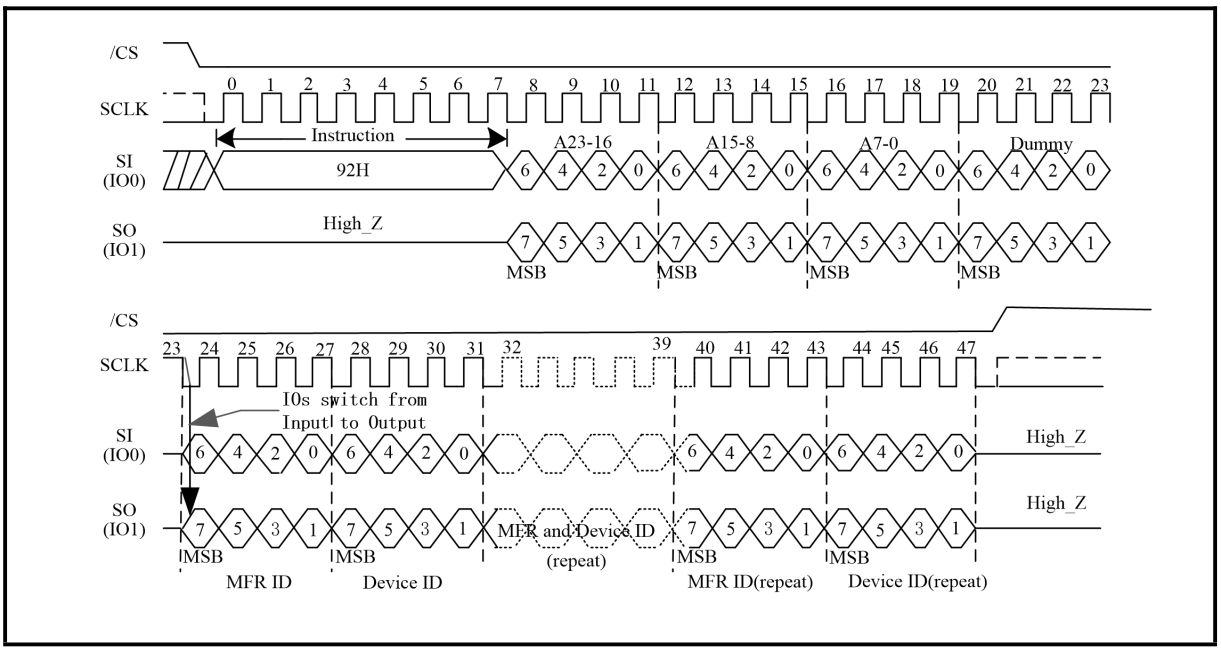


7.3.2 Dual I/O Read Manufacture ID/ Device ID (92H)

See ***Figure 48***, the Dual I/O Read Manufacturer/Device ID instruction is an alternative to the Release from Power-Down/Device ID instruction that provides both the JEDEC assigned Manufacturer ID and the specific Device ID by Dual I/O.

The instruction is initiated by driving the /CS pin low and shifting the instruction code “92H” followed by a 24bit address (A23-A0) of 000000H. If the 24-bit address is initially set to 000001H, the Device ID will be read first.

Figure 48. Dual I/O Read Manufacture ID/ Device ID Sequence Diagram (SPI Mode)

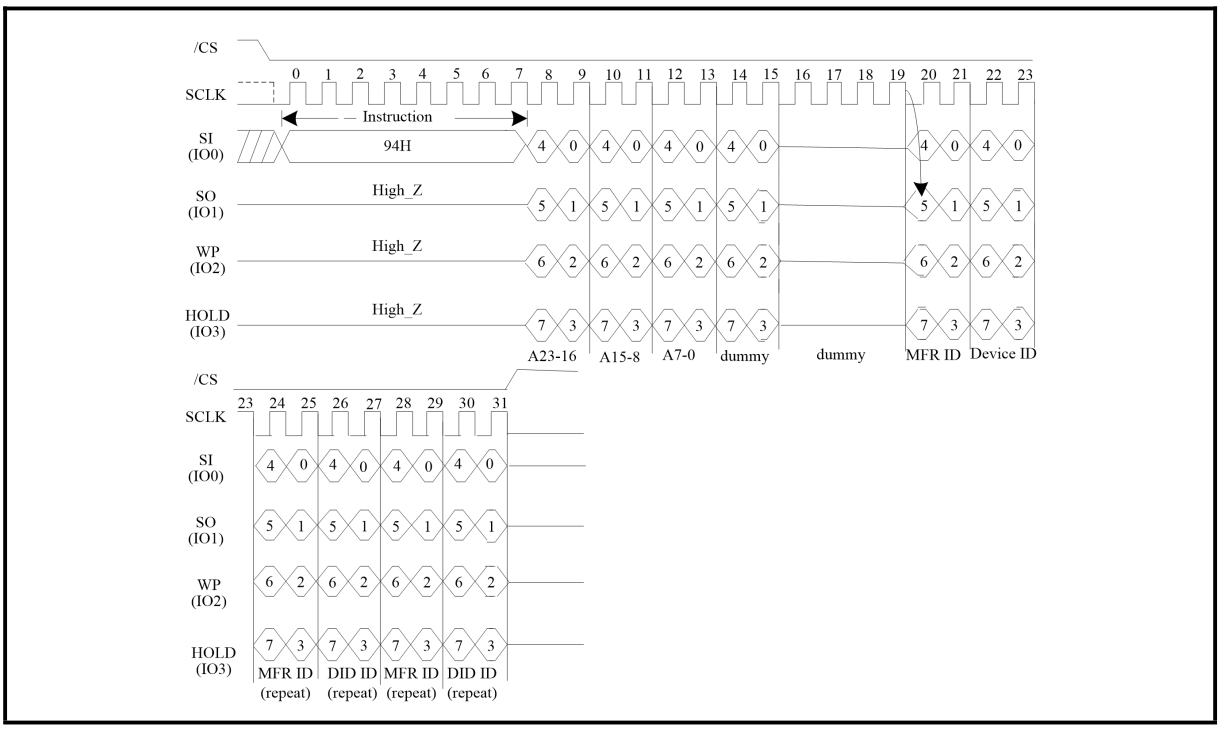


7.3.3 Quad I/O Read Manufacture ID/ Device ID (94H)

See ***Figure 50***, the Quad I/O Read Manufacturer/Device ID instruction is an alternative to the Release from Power-Down/Device ID instruction that provides both the JEDEC assigned Manufacturer ID and the specific Device ID by quad I/O. The Quad Enable bit (QE) of Status Register must be set to enable.

The instruction is initiated by driving the /CS pin low and shifting the instruction code “94H” followed by a 24-bit address (A23-A0) of 000000H and 6 dummy clocks. If the 24-bit address is initially set to 000001H, the Device ID will be read first.

Figure 49. Quad I/O Read Manufacture ID/ Device ID Sequence Diagram (SPI Mode)



7.3.4 Read JEDEC ID (9FH)

The JEDEC ID instruction allows the 8-bit manufacturer identification to be read, followed by two bytes of device identification. The device identification indicates the memory type in the first byte, and the memory capacity of the device in the second byte. JEDEC ID instruction while an Erase or Program cycle is in progress, is not decoded, and has no effect on the cycle that is in progress. The JEDEC ID instruction should not be issued while the device is in Deep Power-Down Mode.

See ***Figure 50-Figure 51***, the device is first selected by driving /CS to low. Then, the 8-bit instruction code for the instruction is shifted in. This is followed by the 24-bit device identification, stored in the memory, being shifted out on Serial Data Output, each bit being shifted out during the falling edge of Serial Clock. The JEDEC ID instruction is terminated by driving /CS to high at any time during data output. When /CS is driven high, the device is put in the Standby Mode. Once in the Standby Mode, the device waits to be selected, so that it can receive, decode and execute instructions.

Figure 50. JEDEC ID Sequence Diagram (SPI Mode)

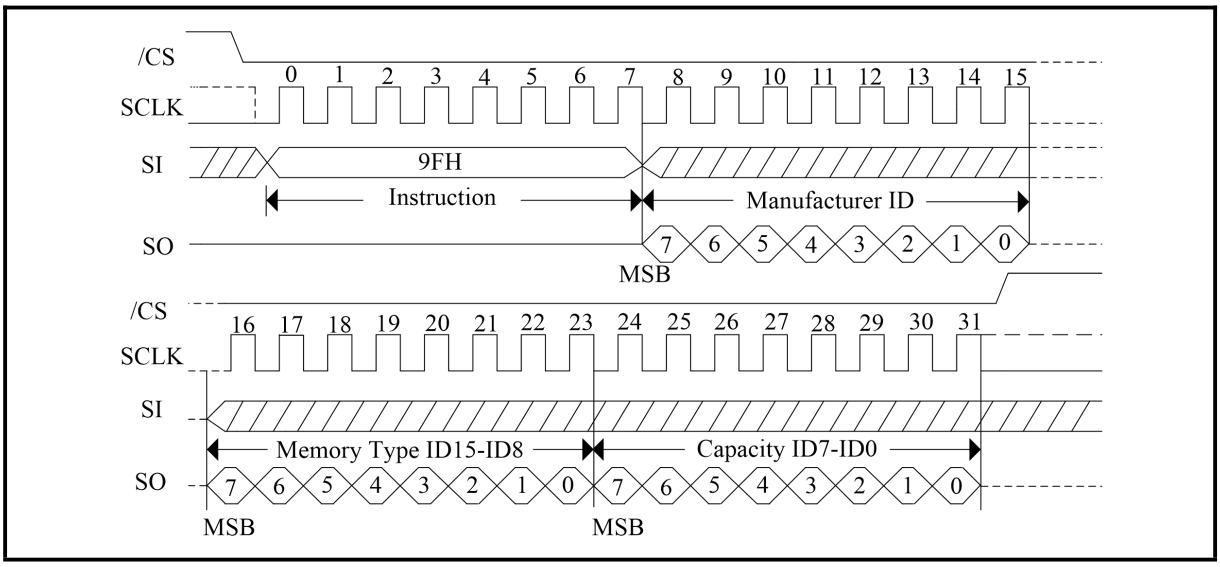
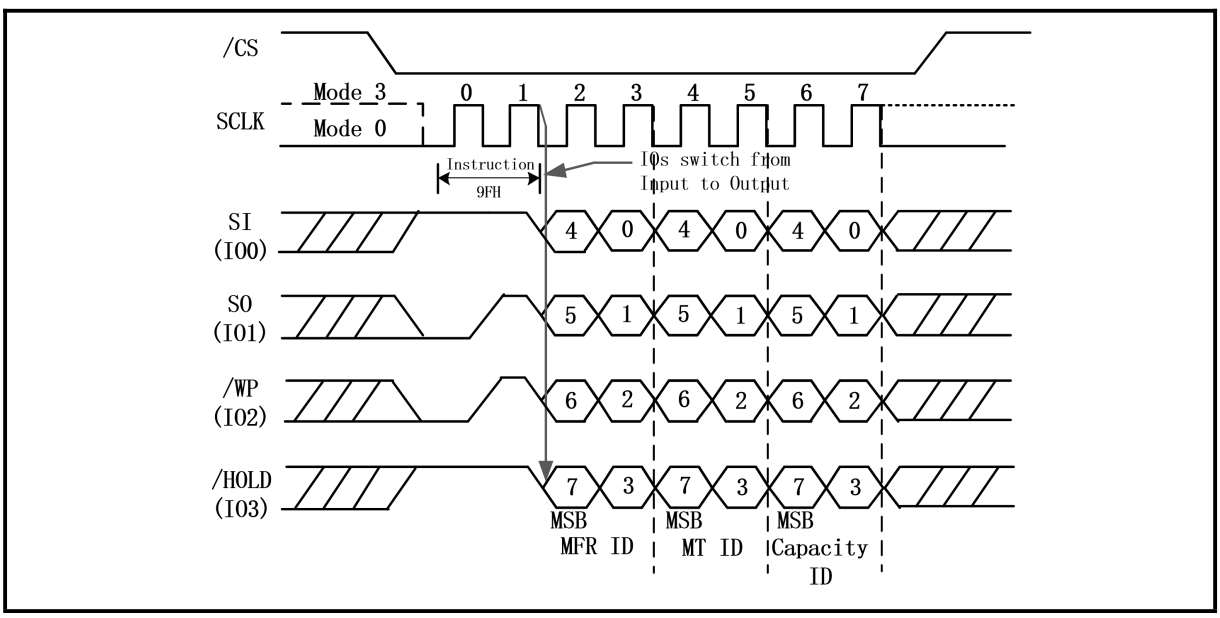


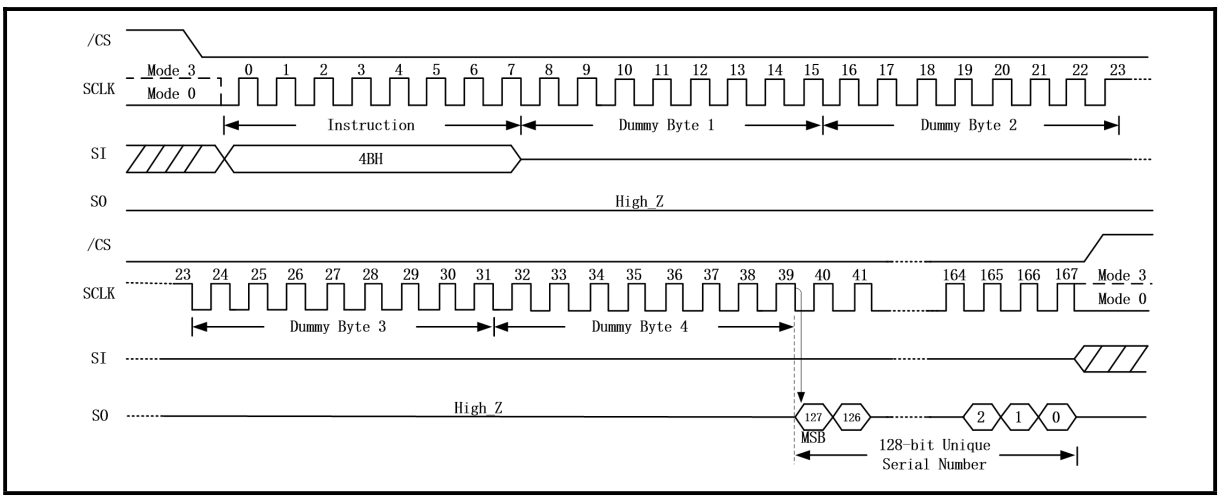
Figure 51. JEDEC ID Sequence Diagram (QPI Mode)



7.3.5 Read Unique ID Number (4Bh)

The Read Unique ID Number instruction accesses a factory-set read-only 128-bit number that is unique to each BY25FQ32ES device. The ID number can be used in conjunction with user software methods to help prevent copying or cloning of a system. The Read Unique ID instruction is initiated by driving the /CS pin low and shifting the instruction code “4Bh” followed by four or five bytes of dummy clocks in SPI mode.

Figure 52. Read Unique ID Sequence Diagram (SPI Mode only)



7.3.6 Deep Power-Down (B9H)

Although the standby current during normal operation is relatively low, standby current can be further reduced with the Deep Power-down instruction. The lower power consumption makes the Deep Power-down (DPD) instruction especially useful for battery powered applications (*see ICC1 and ICC2*). The instruction is initiated by driving the /CS pin low and shifting the instruction code "B9h" as shown in ***Figure 53-Figure 54***

The /CS pin must be driven high after the eighth bit has been latched. If this is not done the Deep Power down instruction will not be executed. After /CS is driven high, the power-down state will entered within the time duration of tDP. While in the power-down state only the Release from Deep Power-down/Device ID instruction, software reset sequence or hardware reset sequence, which restores the device to normal operation, will be recognized. All other Instructions are ignored. This includes the Read Status Register instruction, which is always available during normal operation. Ignoring all but one instruction also makes the Power Down state a useful condition for securing maximum write protection. The device always powers-up in the normal operation with the standby current of ICC1.

Figure 53. Deep Power-Down Sequence Diagram (SPI Mode)

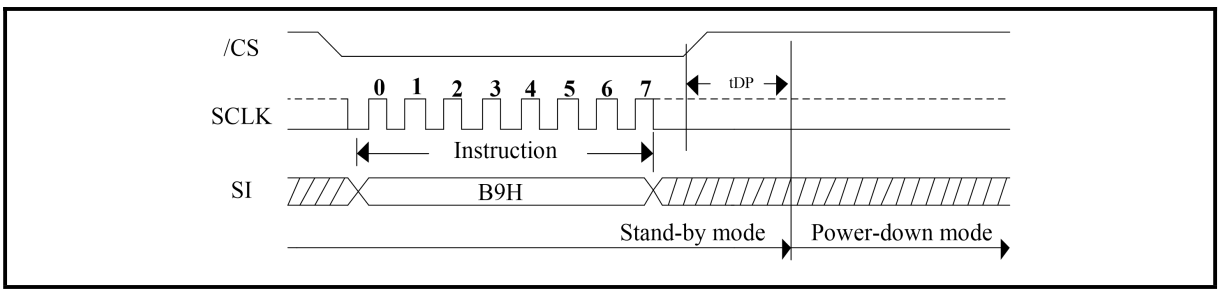
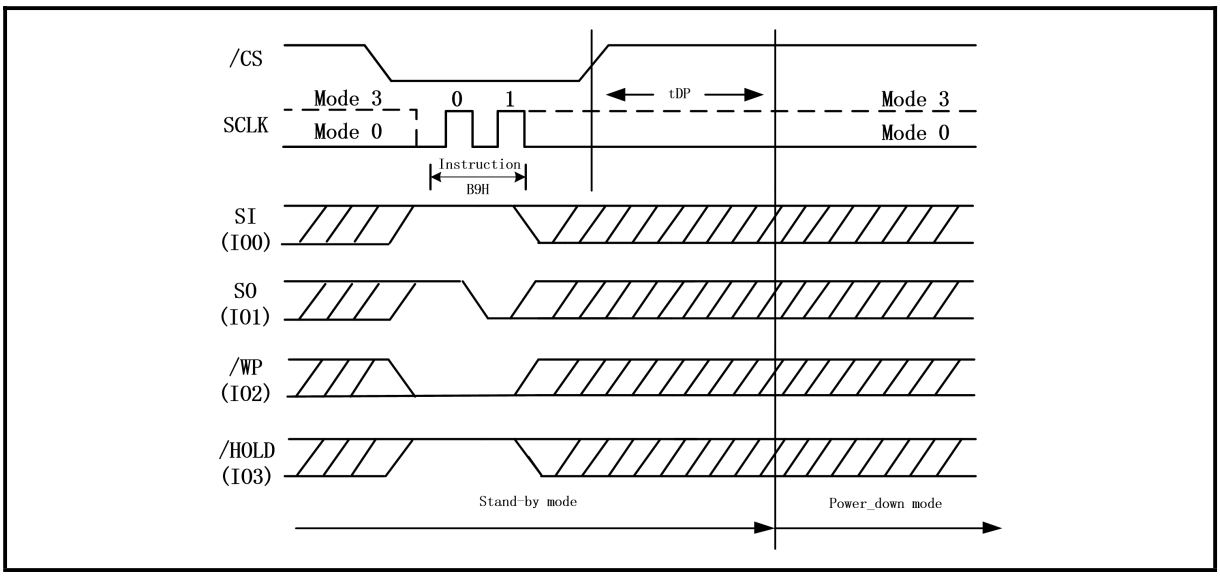


Figure 54. Deep Power-Down Sequence Diagram (QPI Mode)



7.3.7 Release from Deep Power-Down/Read Device ID (ABH)

The Release from Power-Down or Device ID instruction is a multi-purpose instruction. It can be used to release the device from the Power-Down state or obtain the devices electronic identification (ID) number.

See ***Figure 55-Figure 56***, to release the device from the Power-Down state, the instruction is issued by driving the /CS pin low, shifting the instruction code “ABH” and driving /CS high Release from Power-Down will take the time duration of tRES1 (See *AC Characteristics*) before the device will resume normal operation and other instruction are accepted. The /CS pin must remain high during the tRES1 time duration.

When used only to obtain the Device ID while not in the Power-Down state, the instruction is initiated by driving the /CS pin low and shifting the instruction code “ABH” followed by 3-dummy byte. The Device ID bits are then shifted out on the falling edge of SCLK with most significant bit (MSB) first as shown in ***Figure 57-Figure 58***. The Device ID value for the BY25FQ32ES is listed in Manufacturer and Device Identification table. The Device ID can be read continuously. The instruction is completed by driving /CS high.

When used to release the device from the Power-Down state and obtain the Device ID, the instruction is the same as previously described, and shown in ***Figure 57-Figure 58***, except that after /CS is driven high it must remain high for a time duration of tRES2 (See *AC Characteristics*). After this time duration the device will resume normal operation and other instruction will be accepted. If the Release from Power-Down/Device ID instruction is issued while an Erase, Program or Write cycle is in process (when WIP equal 1) the instruction is ignored and will not have any effects on the current cycle.

Figure 55. Release Power-Down Sequence Diagram (SPI Mode)

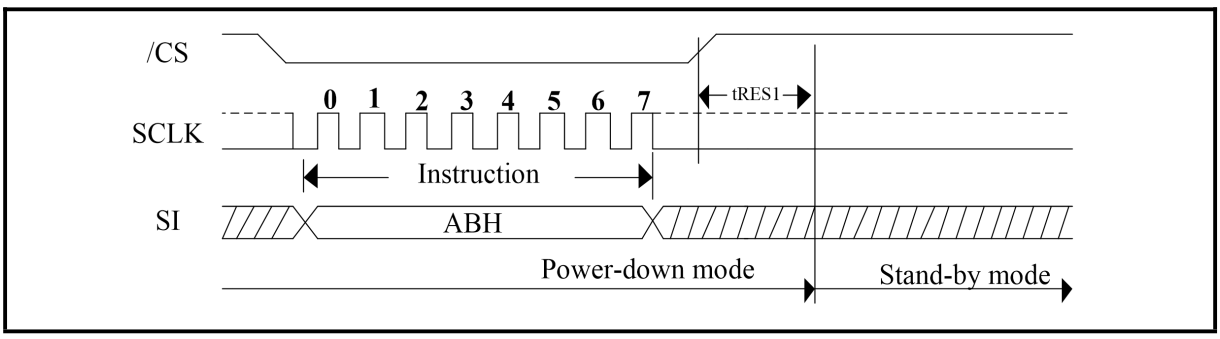


Figure 56. Release Power-Down Sequence Diagram (QPI Mode)

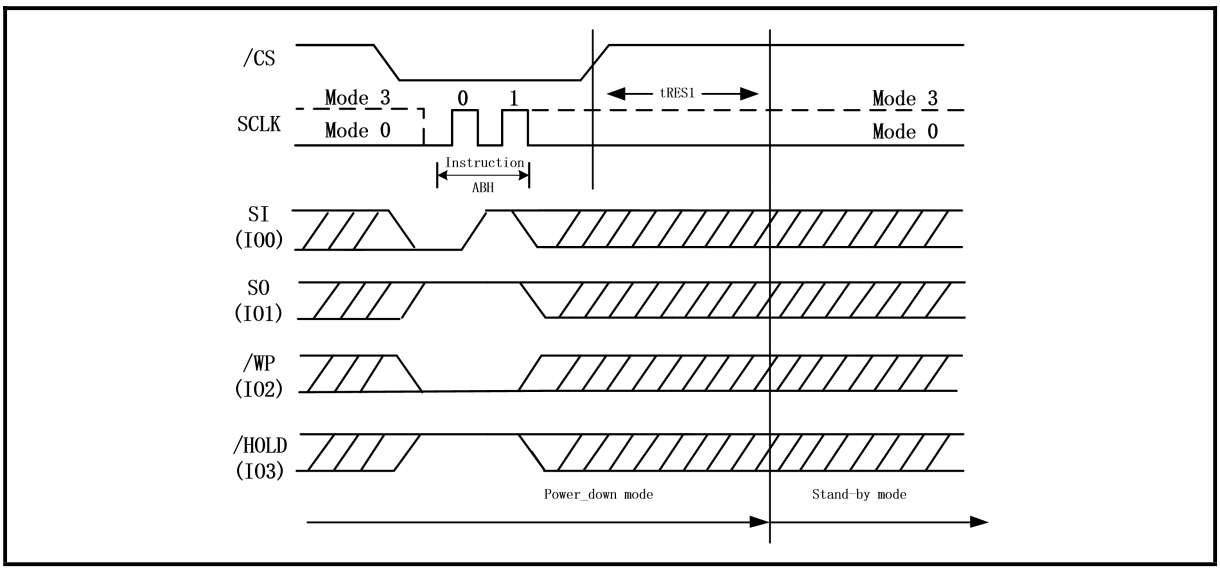


Figure 57. Release Power-Down/Read Device ID Sequence Diagram (SPI Mode)

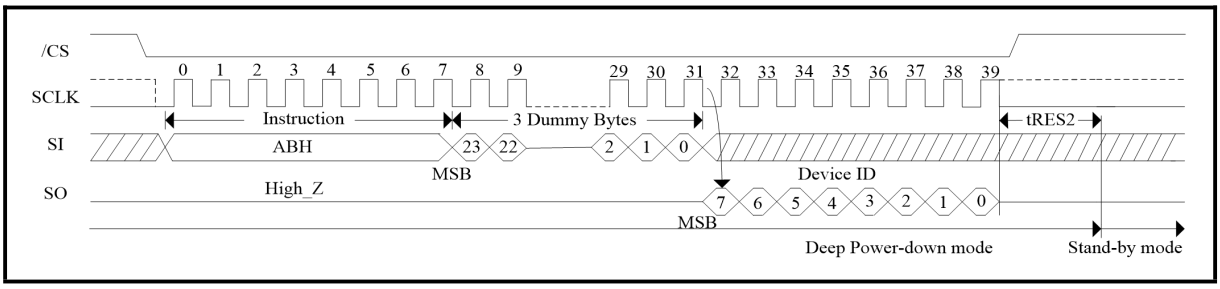
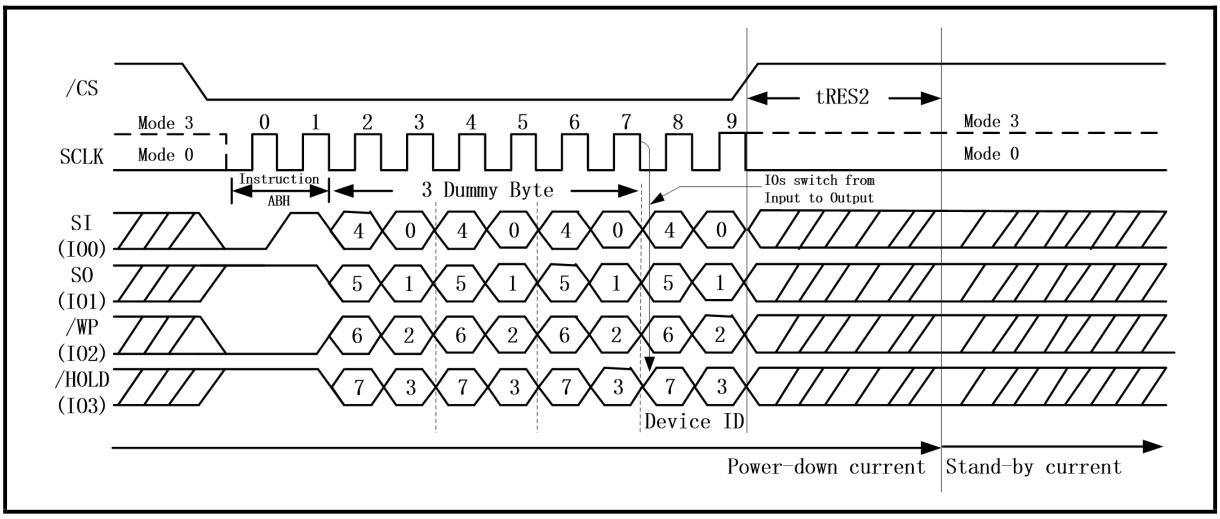


Figure 58. Release Power-Down/Read Device ID Sequence Diagram (QPI Mode)



7.3.8 Read Security Registers (48H)

See ***Figure 59-Figure 60***, the instruction is followed by a 3byte address (A23-A0) and the dummy byte. In QPI mode, the number of dummy can be configured by the "C0h" instruction. Each bit being latched-in during the rising edge of SCLK. Then the memory content, at that address, is shifted out on SO, each bit being shifted out, at a Max frequency F_R, during the falling edge of SCLK. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. Once the A9-A0 address reaches the last byte of the register (Byte 3FFH), it will reset to 000H, the instruction is completed by driving /CS high.

ADDRESS	A23-A16	A15-12	A11-10	A9-0
Security Register #1	00H	0 0 0 1	0 0	Byte Address
Security Register #2	00H	0 0 1 0	0 0	Byte Address
Security Register #3	00H	0 0 1 1	0 0	Byte Address

Figure 59. Read Security Registers instruction Sequence Diagram (SPI Mode)

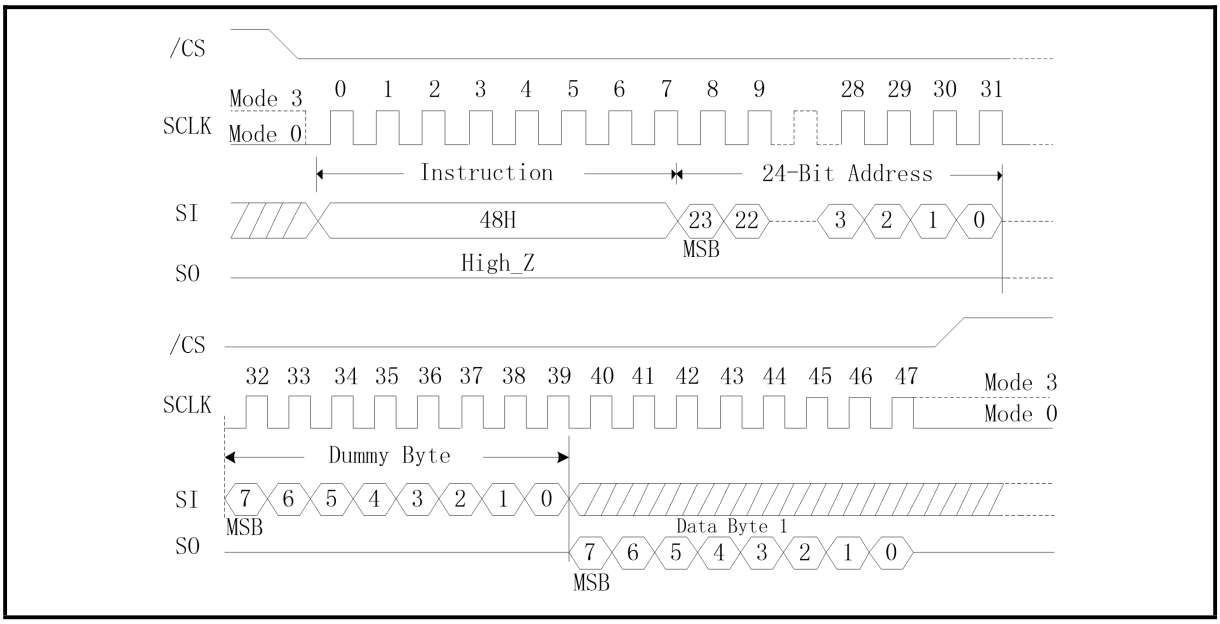
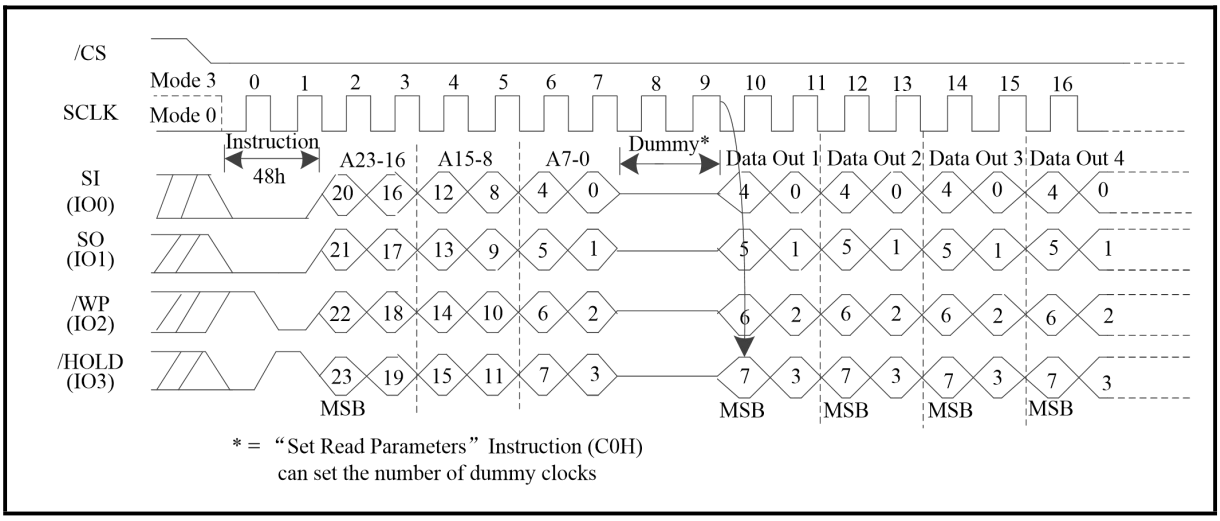


Figure 60. Read Security Registers instruction Sequence Diagram (QPI Mode)



7.3.9 Erase Security Registers (44H)

The BY25FQ32ES provides three 1024-byte Security Registers which can be erased and programmed individually. These registers may be used by the system manufacturers to store security and other important information separately from the main memory array.

See ***Figure 61-Figure 62***, the Erase Security Registers instruction is similar to Block/Sector Erase instruction. A Write Enable instruction must previously have been executed to set the Write Enable Latch bit.

The Erase Security Registers instruction sequence: /CS goes low sending Erase Security Registers instruction /CS goes high. /CS must be driven high after the eighth bit of the instruction code has been latched in otherwise the Erase Security Registers instruction is not executed. As soon as /CS is driven high, the self-timed Erase Security Registers cycle (whose duration is tSE) is initiated. While the Erase Security Registers cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Erase Security Registers cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch bit is reset. The Security Registers Lock Bit (LB) in the Status Register can be used to OTP protect the security registers. Once the LB bit is set to 1, the Security Registers will be permanently locked; the Erase Security Registers instruction will be ignored.

ADDRESS	A23-A16	A15-12	A11-10	A9-0
Security Register #1	00H	0 0 0 1	0 0	Byte Address
Security Register #2	00H	0 0 1 0	0 0	Byte Address
Security Register #3	00H	0 0 1 1	0 0	Byte Address

Figure 61. Erase Security Registers instruction Sequence Diagram (SPI Mode)

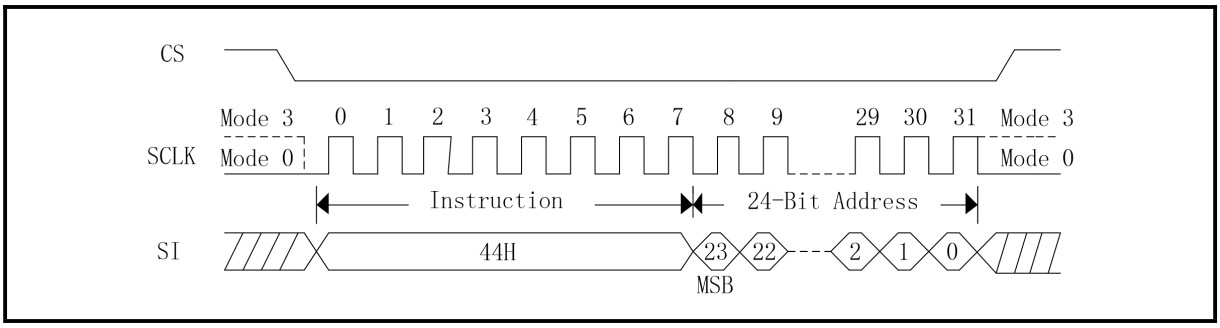
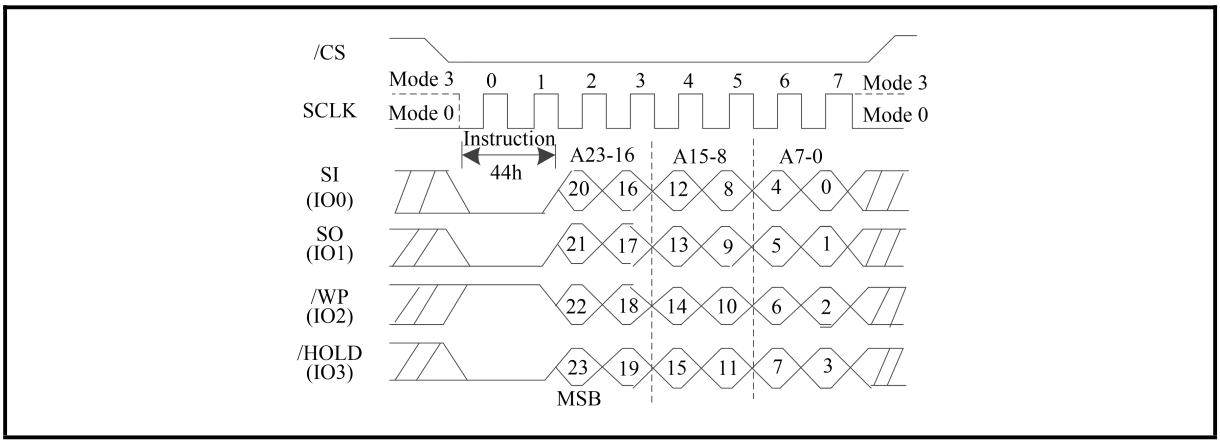


Figure 62. Erase Security Registers instruction Sequence Diagram (QPI Mode)



7.3.10 Program Security Registers (42H)

See ***Figure 63-Figure 64***, the Program Security Registers instruction is similar to the Page Program instruction. It allows from one byte to 1024 bytes of security register data to be programmed by four times (one time program 256 bytes). A Write Enable instruction must previously have been executed to set the Write Enable Latch bit before sending the Program Security Registers instruction. The Program Security Registers instruction is entered by driving /CS Low, followed by the instruction code (42H), 3-byte address and at least one data byte on SI. As soon as /CS is driven high, the self-timed Program Security Registers cycle (whose duration is tPP) is initiated. While the Program Security Registers cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Program Security Registers cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch bit is reset.

If the Security Registers Lock Bit (LB3/LB2/LB1) is set to 1, the Security Registers will be permanently locked. Program Security Registers instruction will be ignored.

ADDRESS	A23-A16	A15-12	A11-10	A9-0
Security Register #1	00H	0 0 0 1	0 0	Byte Address
Security Register #2	00H	0 0 1 0	0 0	Byte Address
Security Register #3	00H	0 0 1 1	0 0	Byte Address

Figure 63. Program Security Registers instruction Sequence Diagram (SPI Mode)

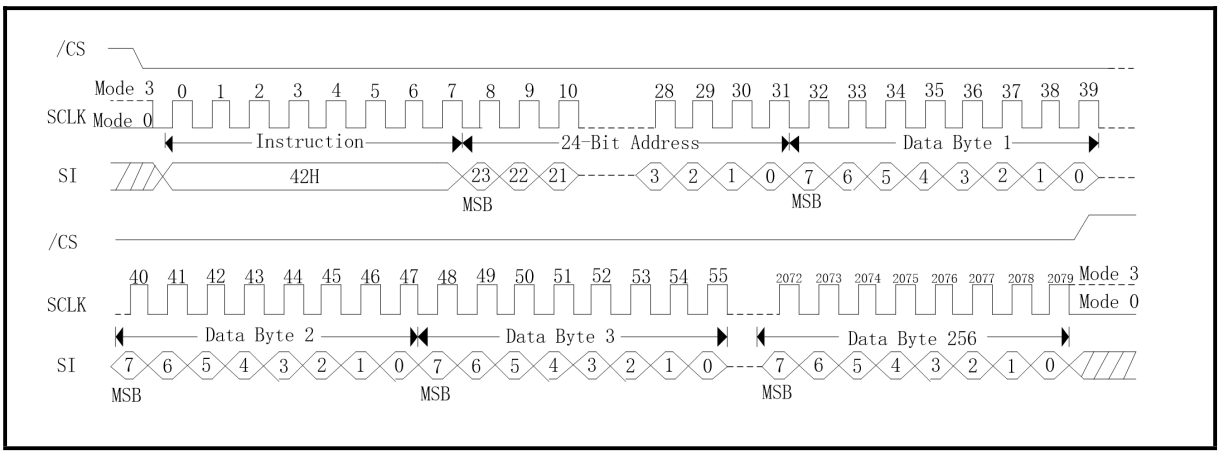
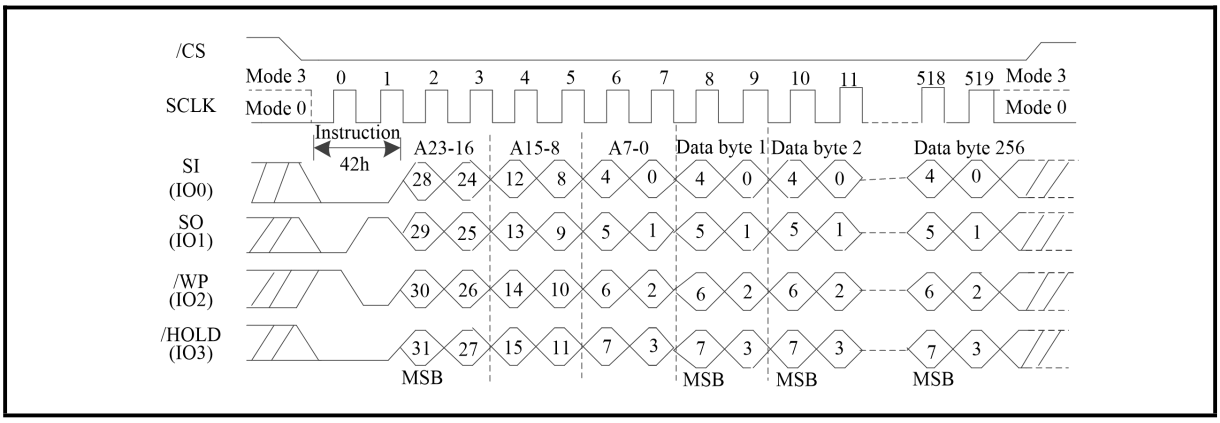


Figure 64. Program Security Registers instruction Sequence Diagram (QPI Mode)



7.3.11 Read Serial Flash Discoverable Parameter (5AH)

See ***Figure 65-Figure 66,*** The Serial Flash Discoverable Parameter (SFDP) standard provides a consistent method of describing the functional and feature capabilities of serial flash devices in a standard set of internal parameter tables. These parameter tables can be interrogated by host system software to enable adjustments needed to accommodate divergent features from multiple vendors. The concept is similar to the one found in the Introduction of JEDEC Standard, JESD68 on CFI. SFDP is a standard of JEDEC Standard No.216.

The Read SFDP instruction is initiated by driving the /CS pin low and shifting the instruction code "5Ah" followed by a 24-bit address (A23-A0) into the SI pin, regardless of the 3-byte or 4-byte Address Mode. Eight "dummy" clocks are also required in SPI mode. In QPI mode，the number of dummy clocks can be configured by the "Set Read Parameters (C0h)" instruction.

Figure 65. Read Serial Flash Discoverable Parameter instruction Sequence Diagram (SPI Mode)

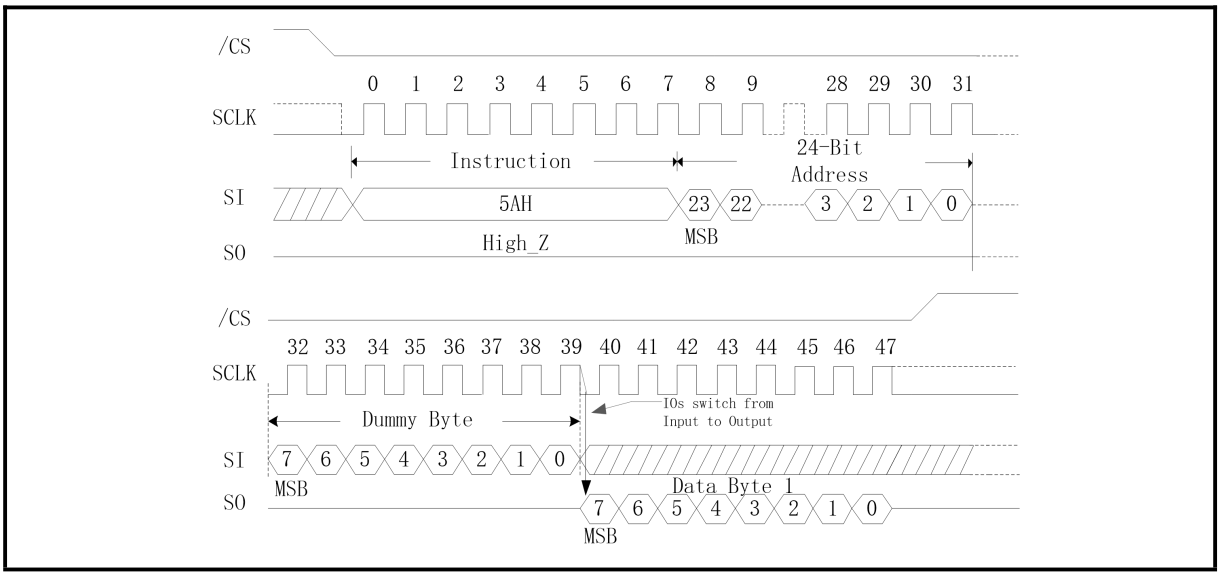
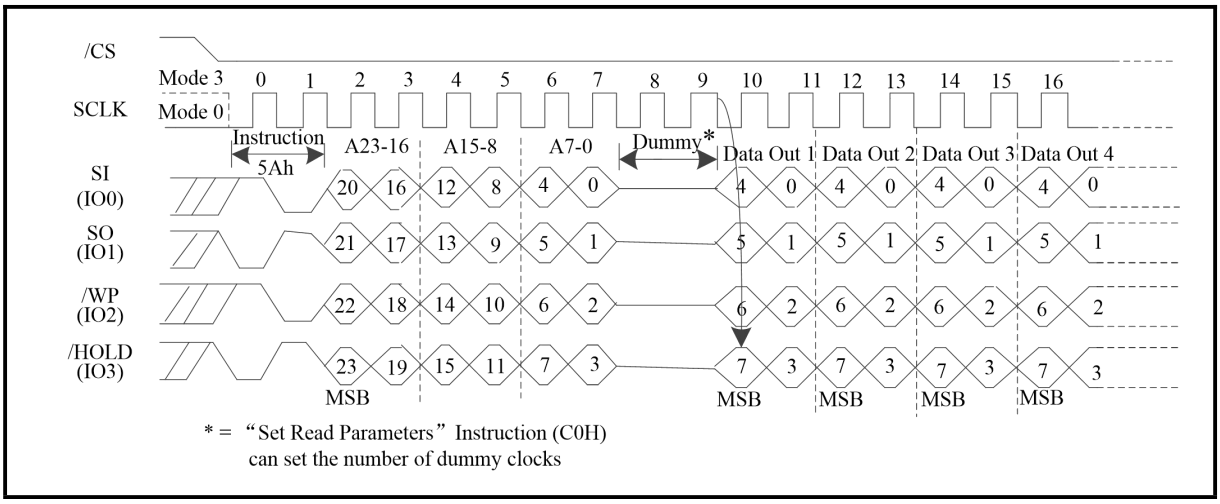


Figure 66. Read Serial Flash Discoverable Parameter instruction Sequence Diagram (QPI Mode)



7.4 Program and Erase Instructions

7.4.1 Page Program (02H)

The Page Program instruction is for programming the memory. A Write Enable instruction must previously have been executed to set the Write Enable Latch bit before sending the Page Program instruction.

See ***Figure 67***, the Page Program instruction is entered by driving /CS Low, followed by the instruction code, 3-byte address and at least one data byte on SI. If the 8 least significant address bits (A7-A0) are not all zero, all transmitted data that goes beyond the end of the current page are programmed from the start address of the same page (from the address whose 8 least significant bits (A7-A0) are all zero). /CS must be driven low for the entire duration of the sequence. The Page Program instruction sequence: /CS goes low-> sending Page Program instruction ->3-byte address on SI ->at least 1 byte data on SI-> /CS goes high.

If more than 256 bytes are sent to the device, previously latched data are discarded and the last 256 data bytes are guaranteed to be programmed correctly within the same page. If less than 256 data bytes are sent to device, they are correctly programmed at the requested addresses without having any effects on the other bytes of the same page. /CS must be driven high after the eighth bit of the last data byte has been latched in; otherwise the Page Program instruction is not executed.

As soon as /CS is driven high, the self-timed Page Program cycle (whose duration is tPP) is initiated. While the Page Program cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Page Program cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch bit is reset.

A Page Program instruction applied to a page which is protected by the Block Protect (BP4, BP3, BP2, BP1, BP0) bits (see ***Table 6-Table 7***) are not executed.

Figure 67. Page Program Sequence Diagram (SPI Mode)

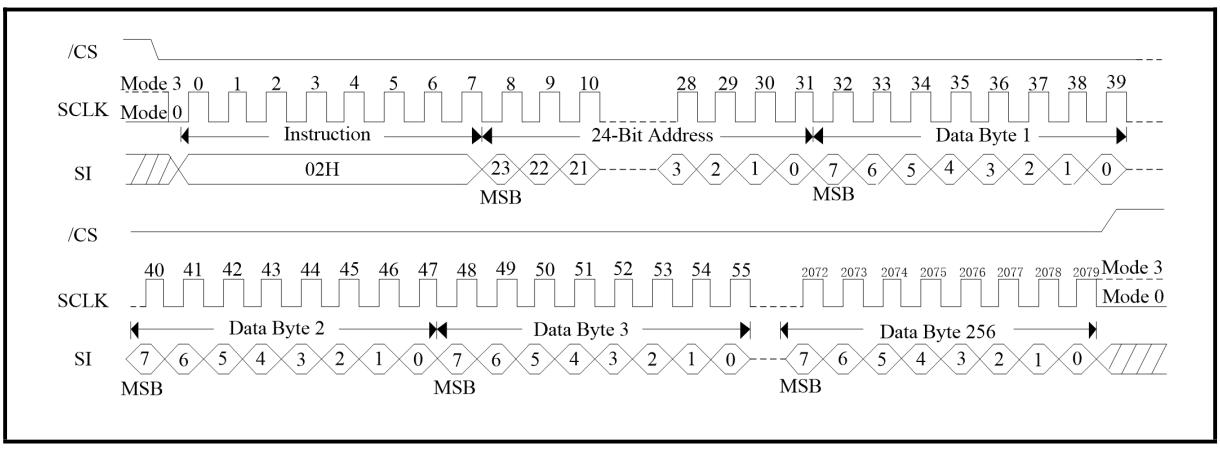
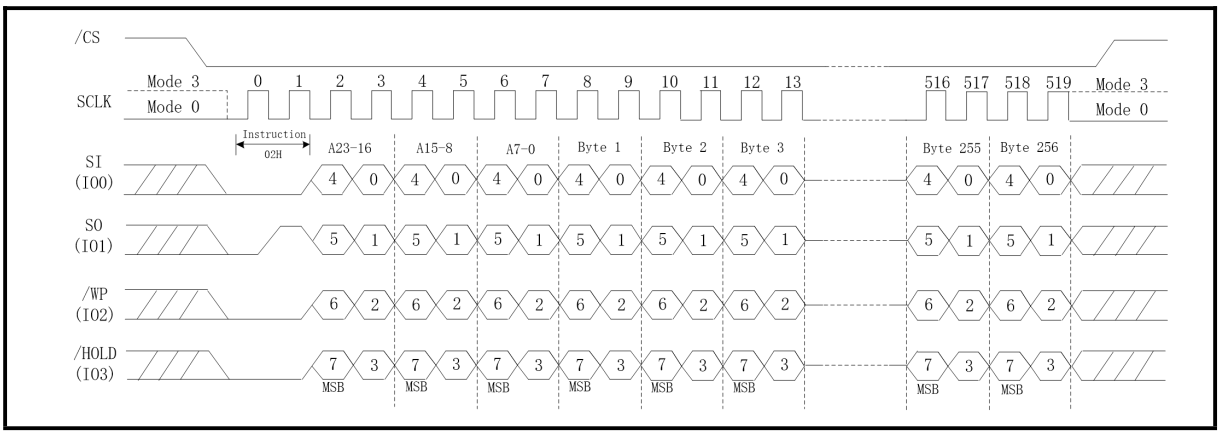


Figure 68. Page Program Sequence Diagram (QPI Mode)



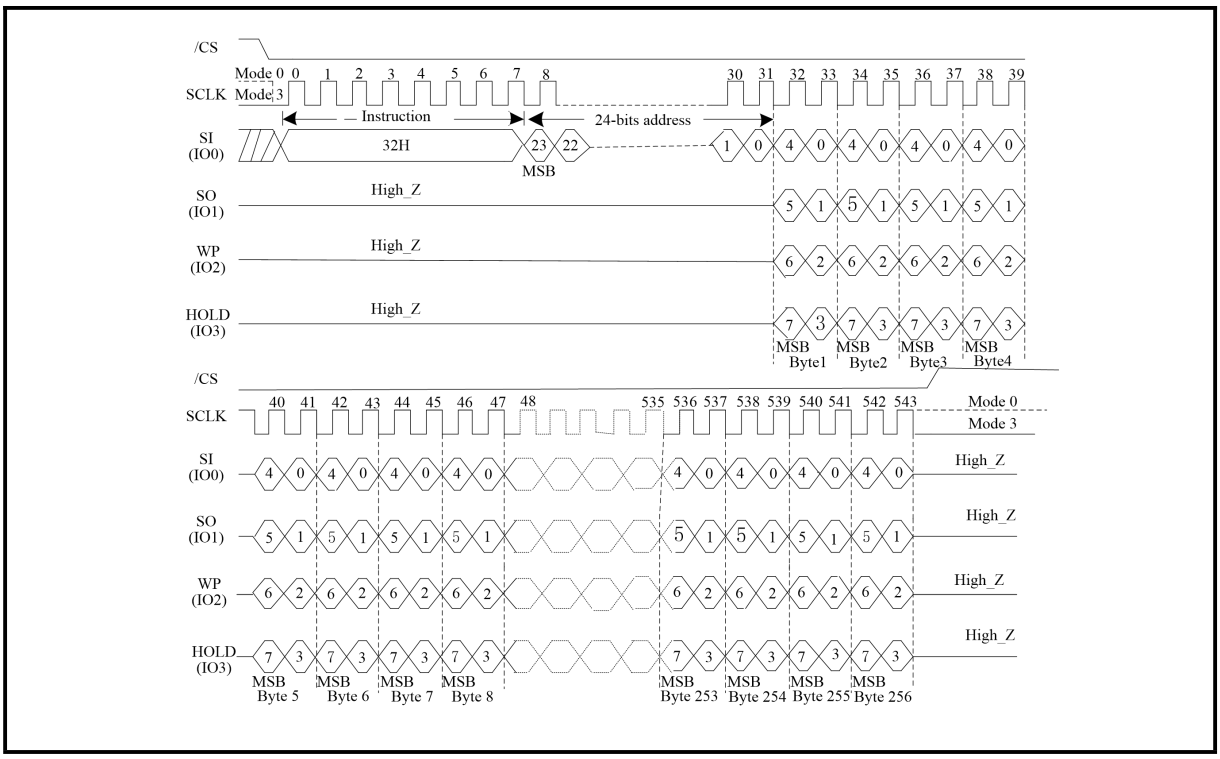
7.4.2 Quad Page Program (32H)

The Quad Page Program instruction is for programming the memory using for pins: IO0, IO1, IO2 and IO3. To use Quad Page Program the Quad enable in status register Bit9 must be set (QE=1). A Write Enable instruction must previously have been executed to set the Write Enable Latch bit before sending the Page Program instruction. The Quad Page Program instruction is entered by driving /CS Low, followed by the instruction code (32H), three address bytes and at least one data byte on IO pins. The Quad Enable bit (QE) of Status Register must be set to enable.

The instruction sequence is shown in ***Figure 69***. If more than 256 bytes are sent to the device, previously latched data are discarded and the last 256 data bytes are guaranteed to be programmed correctly within the same page. If less than 256 data bytes are sent to device, they are correctly programmed at the requested addresses without having any effects on the other bytes of the same page. /CS must be driven high after the eighth bit of the last data byte has been latched in; otherwise the Quad Page Program instruction is not executed.

As soon as /CS is driven high, the self-timed Quad Page Program cycle (whose duration is tPP) is initiated. While the Quad Page Program cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Quad Page Program cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch bit is reset. A Quad Page Program instruction applied to a page which is protected by the Block Protect (BP4, BP3, BP2, BP1, BP0) bits (see ***Table 6-Table 7***) is not executed

Figure 69. Quad Page Program Sequence Diagram (SPI Mode only)



7.4.3 Sector Erase (20H)

The Sector Erase instruction is for erasing the all data of the chosen sector. A Write Enable instruction must previously have been executed to set the Write Enable Latch bit. The Sector Erase instruction is entered by driving /CS low, followed by the instruction code, and 3-address byte on SI. Any address inside the sector is a valid address for the Sector Erase instruction. /CS must be driven low for the entire duration of the sequence.

See ***Figure 70***, The Sector Erase instruction sequence: /CS goes low-> sending Sector Erase instruction-> 3-byte address on SI ->/CS goes high. /CS must be driven high after the eighth bit of the last address byte has been latched in; otherwise the Sector Erase instruction is not executed. As soon as /CS is driven high, the self-timed Sector Erase cycle (whose duration is tSE) is initiated. While the Sector Erase cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Sector Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch bit is reset. A Sector Erase instruction applied to a sector which is protected by the Block Protect (BP4, BP3, BP2, BP1, BP0) bits (see ***Table 6-Table 7***) is not executed.

Figure 70. Sector Erase Sequence Diagram (SPI Mode)

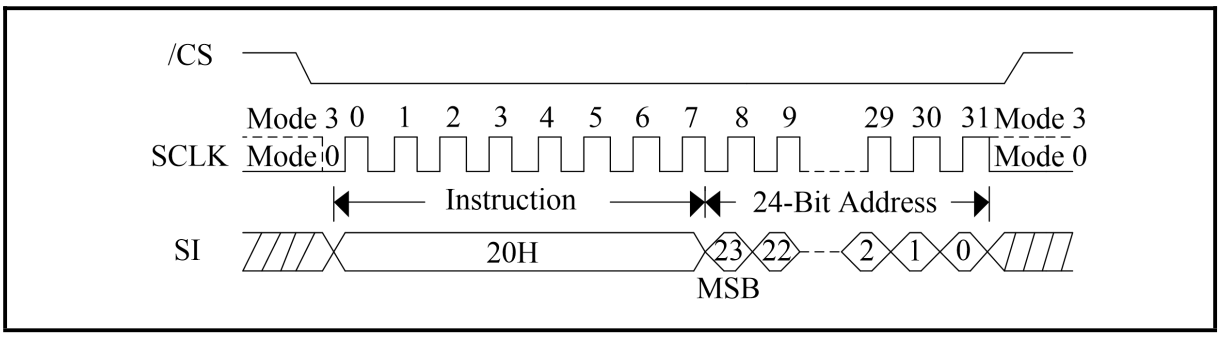
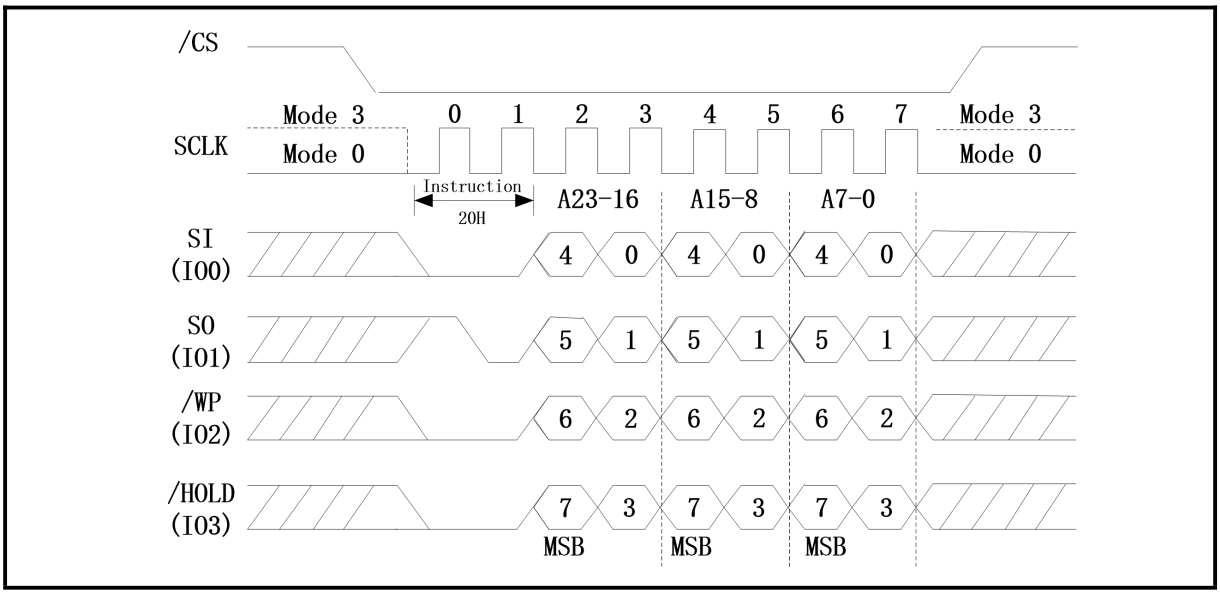


Figure 71. Sector Erase Sequence Diagram (QPI Mode/3-Byte Address Mode)



7.4.4 32KB Block Erase (52H)

The 32KB Block Erase instruction is for erasing the all data of the chosen block. A Write Enable instruction must previously have been executed to set the Write Enable Latch bit. The 32KB Block Erase instruction is entered by driving /CS low, followed by the instruction code, and 3-byte address on SI. Any address inside the block is a valid address for the 32KB Block Erase instruction. /CS must be driven low for the entire duration of the sequence.

See ***Figure 72***, the 32KB Block Erase instruction sequence: /CS goes low ->sending 32KB Block Erase instruction ->3-byte address on SI ->/CS goes high. /CS must be driven high after the eighth bit of the last address byte has been latched in; otherwise the 32KB Block Erase instruction is not executed. As soon as /CS is driven high, the self-timed Block Erase cycle (whose duration is tBE) is initiated. While the Block Erase cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Block Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch bit is reset. A 32KB Block Erase instruction applied to a block which is protected by the Block Protect (BP4, BP3, BP2, BP1, BP0) bits (see ***Table 6-Table 7***) is not executed.

Figure 72. 32KB Block Erase Sequence Diagram (SPI Mode)

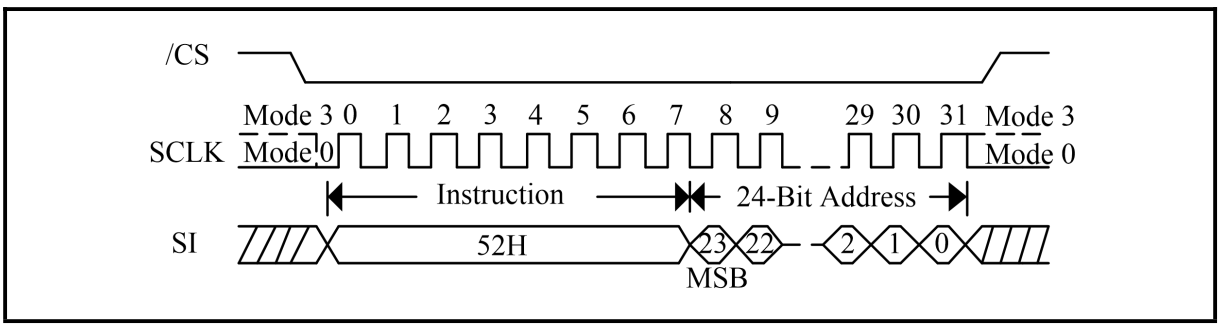
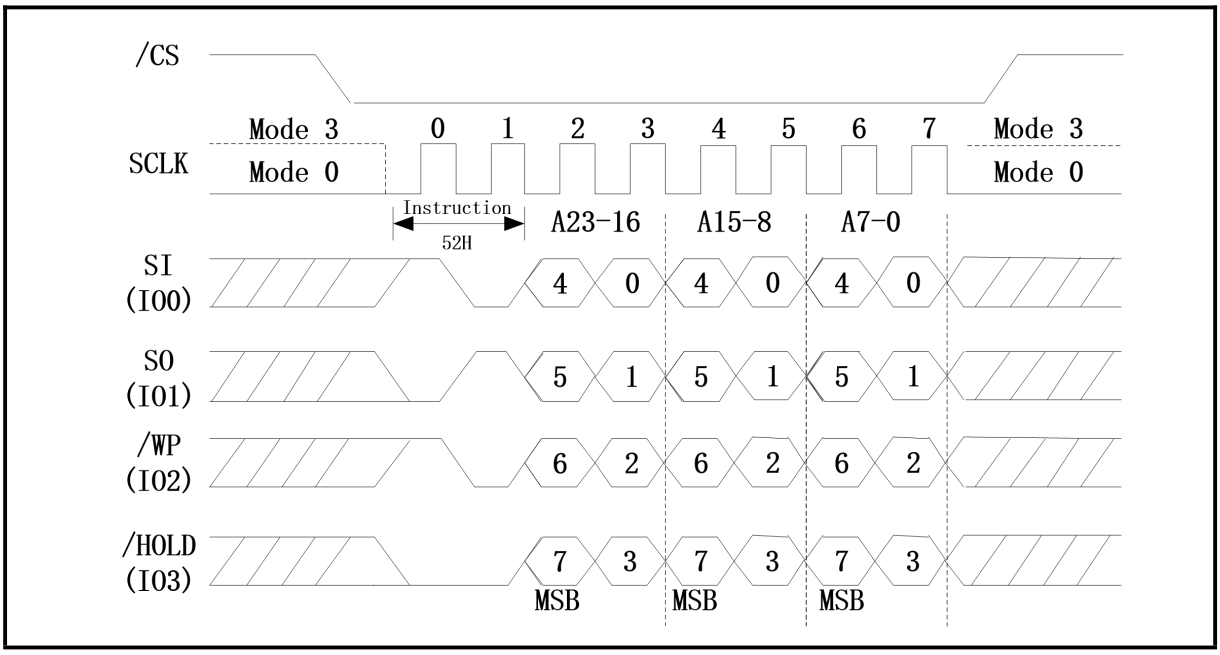


Figure 73. 32KB Block Erase Sequence Diagram (QPI Mode)



7.4.5 64KB Block Erase (D8H)

The 64KB Block Erase instruction is for erasing the all data of the chosen block. A Write Enable instruction must previously have been executed to set the Write Enable Latch bit. The 64KB Block Erase instruction is entered by driving /CS low, followed by the instruction code, and 3-byte address on SI. Any address inside the block is a valid address for the 64KB Block Erase instruction. /CS must be driven low for the entire duration of the sequence.

See ***Figure 74***, the 64KB Block Erase instruction sequence: /CS goes low sending 64KB Block Erase instruction 3-byte address on SI /CS goes high. /CS must be driven high after the eighth bit of the last address byte has been latched in; otherwise the 64KB Block Erase instruction is not executed. As soon as /CS is driven high, the self-timed Block Erase cycle (whose duration is tBE) is initiated. While the Block Erase cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Block Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch bit is reset. A 64KB Block Erase instruction applied to a block which is protected by the Block Protect (BP4, BP3, BP2, BP1, BP0) bits (see ***Table 6-Table 7***) is not executed.

Figure 74. 64KB Block Erase Sequence Diagram (SPI Mode)

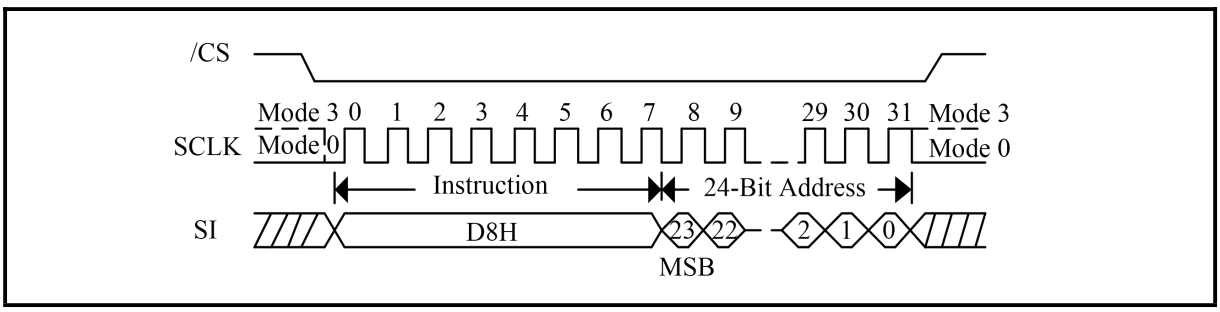
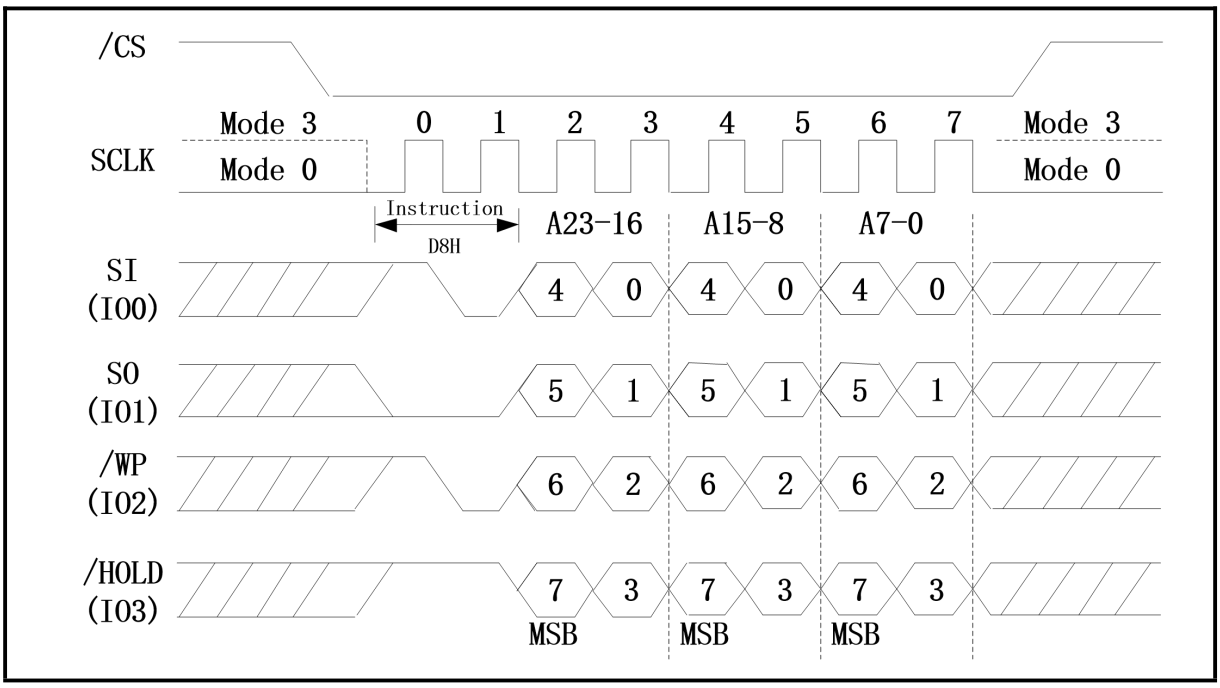


Figure 75. 64KB Block Erase Sequence Diagram (QPI Mode)



7.4.6 Chip Erase (60/C7H)

The Chip Erase instruction sets all memory within the device to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Chip Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the /CS pin low and shifting the instruction code “C7h” or “60h”. The Chip Erase instruction sequence is shown in ***Figure 76***.

The /CS pin must be driven high after the eighth bit has been latched. If this is not done the Chip Erase instruction will not be executed. After /CS is driven high, the self-timed Chip Erase instruction will commence for a time duration of tCE. While the Chip Erase cycle is in progress, the Read Status Register instruction may still be accessed to check the status of the WIP bit.

The WIP bit is a 1 during the Chip Erase cycle and becomes a 0 when finished and the device is ready to accept other Instructions again. After the Chip Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Chip Erase instruction is executed only if all Block Protect (BP2, BP1, and BP0) bits are 0.The Chip Erase instruction is ignored if one or more sectors are protected.

Figure 76. Chip Erase Sequence Diagram (SPI Mode)

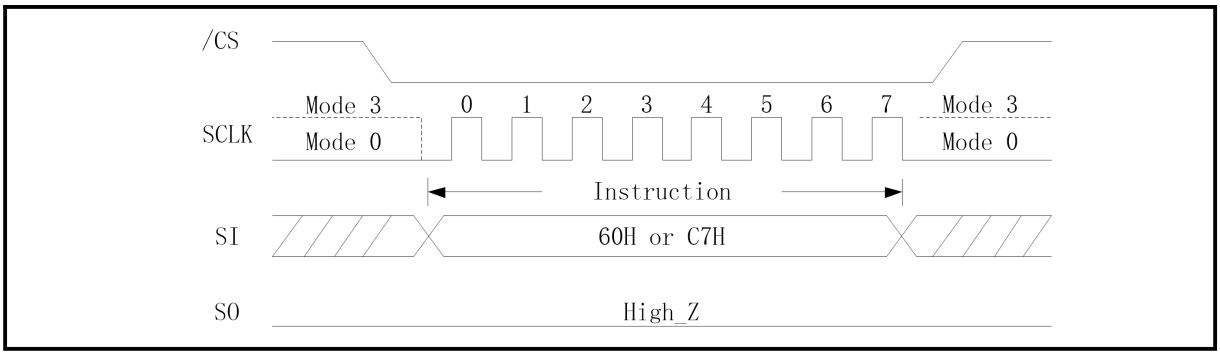
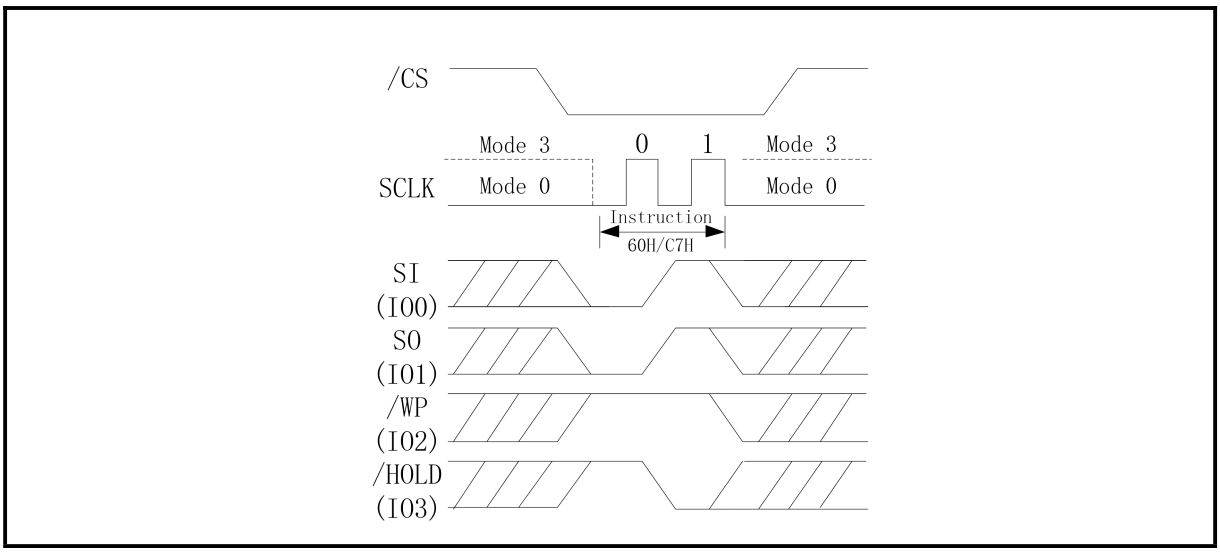


Figure 77. Chip Erase Sequence Diagram (QPI Mode)



7.4.7 Program/Erase Suspend (75H)

The Program/Erase Suspend instruction “75h” allows the system to interrupt a Page Program or a Sector/32K/64K Block Erase operation (The time between the Program/Erase instruction and the Program/Erase Suspend instruction is tPS/tES). After the program operation has entered the suspended state, the memory array can be read except for the page being programmed. And after the erase operation has entered the suspended state, the memory array can be read or programed except for the sector/32kb block/64kb block being erased. Write status register operation can't be suspended. The Program/Erase Suspend instruction sequence is shown in ***Figure 78***.

Table 14. Readable Area of Memory While a Program Operation is Suspended

Suspended operation	Readable Region Of Memory Array
Page Program	All but the Page being programmed
Quad Page Program	All but the Page being programmed

Table 15. Readable or Programmable Area of Memory While an Erase Operation is Suspended

Suspended operation	Readable Region or Programmable Of Memory Array
Erase(4KB)	All but the Sector being Erased
Block Erase(32KB)	All but the 32kb Block being Erased
Block Erase(64KB)	All but the 64kb Block being Erased

When the Serial NOR Flash receives the Suspend instruction, there is a latency of tPSL or tESL before the Write Enable Latch (WEL) bit clears to “0” and the SUS2 or SUS1 sets to “1”, after which the device is ready to accept one of the instructions listed in "Table Acceptable Instructions During Program/Erase Suspend after tPSL/tESL" (e.g. FAST READ). Refer to " AC Characteristics" for tPSL and tESL timings. "Table Acceptable instructions During Suspend (tPSL/tESL not required)" lists the Instructions for which the tPSL and tESL latencies do not apply. For example, “05h”, “66h” and “99h” can be issued at any time after the Suspend instruction.

Status Register bit 15 (SUS2) and bit 10 (SUS1) can be read to check the suspend status. The SUS2 (Program Suspend Bit) sets to “1” when a program instruction is suspended. The SUS1 (Erase Suspend Bit) sets to “1” when an erase operation is suspended. The SUS2 or SUS1 clears to “0” when the program or erase instruction is resumed.

Table 16. Acceptable instructions During Program/Erase Suspend after tPSL/tESL

Instruction Name	Instruction code	Suspend Type	
		Program Suspend	Erase Suspend
Write Enable	06h	*	*
Write Disable	04h	*	*
Read Data	03h	*	*
Fast Read	0Bh	*	*
Dual Output Fast Read	3Bh	*	*
Quad Output Fast Read	6Bh	*	*
Dual I/O Fast Read	BBh	*	*
Quad I/O Fast Read	EBh	*	*
Quad I/O Word Fast Read	E7h	*	*
Set Burst with Wrap	77h	*	*

Instruction Name	Instruction code	Suspend Type	
		Program Suspend	Erase Suspend
Read Mftr./Device ID	90h	*	*
Dual IO Read Mftr./Device ID	92h	*	*
Quad IO Read Mftr./Device ID	94h	*	*
Read JEDEC ID	9Fh	*	*
Read Unique ID Number	4Bh	*	*
Release Powen-down/Device ID	ABh	*	*
Read Securty Registers	48h	*	*
Read SFDP	5Ah	*	*
Page Program	02h		*
Quad Page Program	32h		*
Program/Erase Resume	7Ah	*	*

Table 17. Acceptable Instructions During Suspend（tPSL/tESL not required）

Instruction Name	Instruction code	Suspend Type	
		Program Suspend	Erase Suspend
Read Status Register-1	05H	*	*
Read Status Register-2	35H	*	*
Read Status Register-3	15H	*	*
Enable Reset	66H	*	*
Reset Device	99H	*	*

tPSL: Program Suspend Latency; tESL: Erase Suspend Latency.

Figure 78. Program/Erase Suspend Instruction Sequence (SPI Mode)

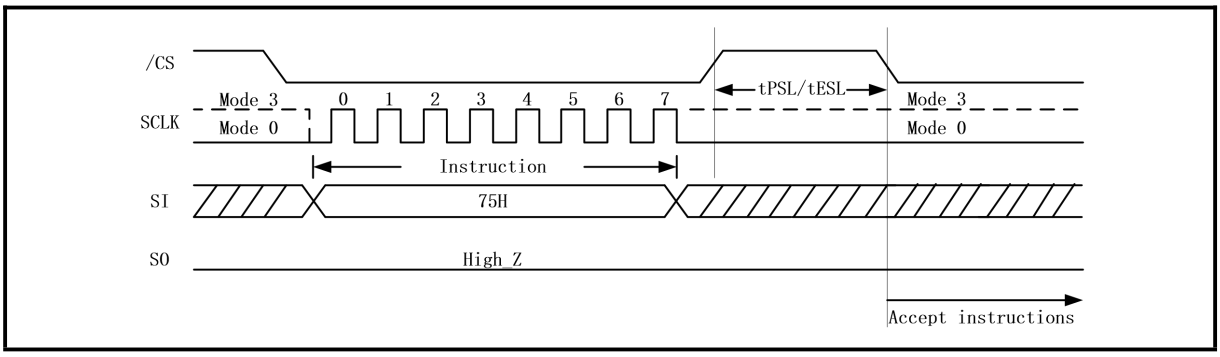
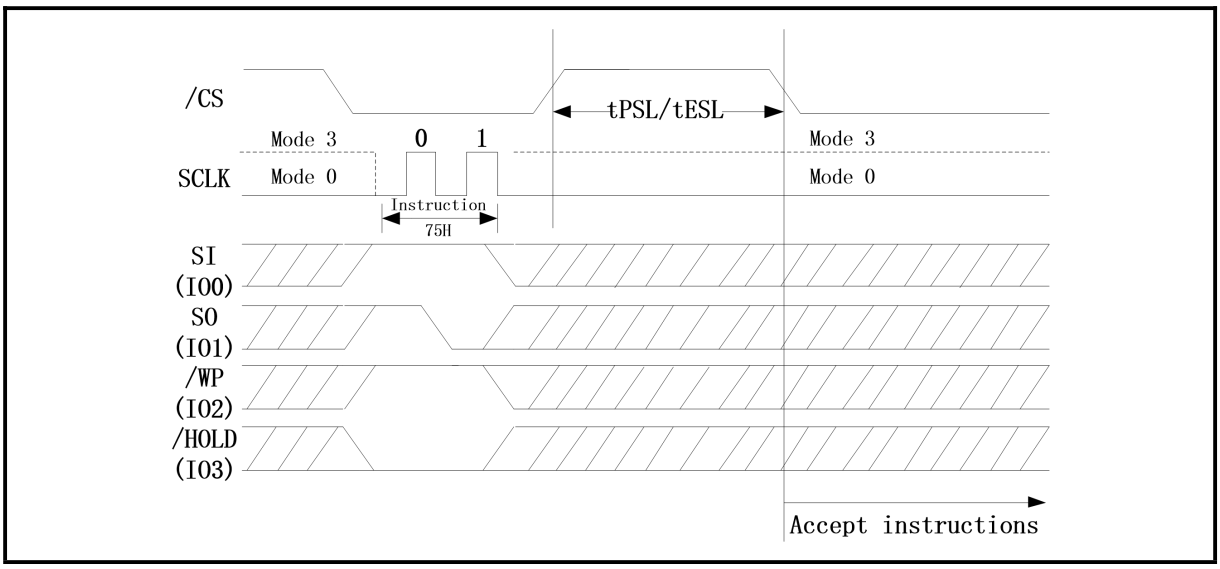


Figure 79. Program/Erase Suspend Instruction Sequence (QPI Mode)

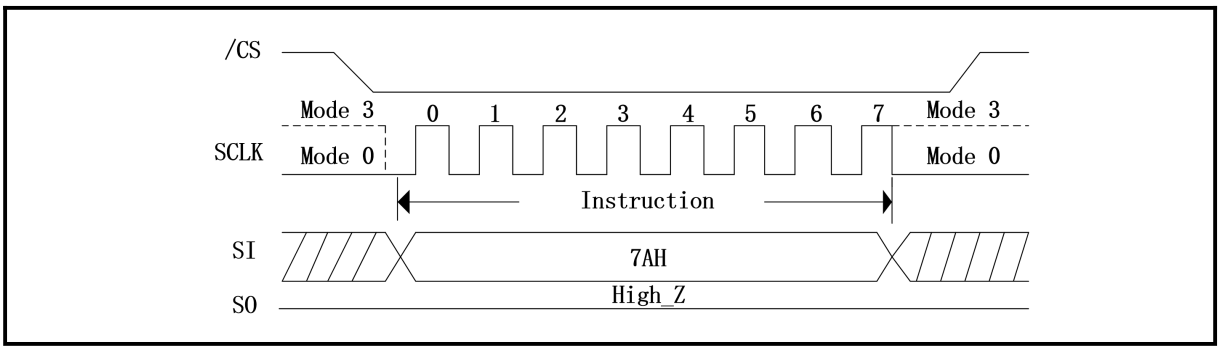


7.4.8 Program/Erase Resume (7AH)

The Program/Erase Resume instruction “7Ah” must be written to resume the Sector or Block Erase operation or the Page Program operation after an Program/Erase Suspend. The Resume instruction “7AH” will be accepted by the device only if the SUS bit in the Status Register equals to 1 and the WIP bit equals to 0.

After the Resume instruction is issued the SUS bit will be cleared from 1 to 0 immediately, the WIP bit will be set from 0 to 1 within 200 ns and the Sector or Block will complete the erase operation or the page will complete the program operation. If the SUS bit equals to 0 or the WIP bit equals to 1, the Resume instruction “7Ah” will be ignored by the device. The Program/Erase Resume instruction sequence is shown in ***Figure 80***.

Figure 80. Program/Erase Resume Instruction Sequence (SPI Mode)



8. ELECTRICAL CHARACTERISTICS

8.1 Absolute Maximum Ratings(1)

Parameter	Symbol	Conditions	Range	Unit.
Supply Voltage	VCC		–0.6 to 4.0	V
Voltage Applied to Any Pin	V_{IO}	Relative to Ground	–0.5 to VCC+0.4	V
Transient Voltage on any Pin	V_{IOT}	<20nS Transient Relative to Ground	–2.0V to VCC+2.0V	V
Storage Temperature	T_{STG}		–65 to +150	°C

Notes:

1. This device has been designed and tested for the specified operation ranges. Proper operation outside of these levels is not guaranteed. Exposure to absolute maximum ratings may affect device reliability. Exposure beyond absolute maximum ratings may cause permanent damage.

8.2 Operating Ranges

Parameter	Symbol	Conditions	Spec		Unit.
			Min	Max	
Supply Voltage	VCC		2.7	3.6	V
Temperature Operating	TA	Industrial	–40	+85	°C

8.3 Latch Up Characteristics

Parameter	Min	Max
Input Voltage Respect To VSS On I/O Pins	-1.0V	VCC+1.0V
VCC Current	-100mA	100mA

8.4 Power-up and Power-Down Timing

Symbol	Parameter	Min	Typ.	Max	Unit.
tVSL	VCC(min) To /CS Low	0.8			ms
V_{WI}	Write Inhibit Threshold Voltage V_{WI}	2.0		2.5	V
tVR	VCC rise time (from 0V to VCCmin)		1	6000 (1)	μs/V
tPWD	VCC brown-out low time	300			μs
V_{PWDMAX}	Maximum VCC brown-out			0.7	V

Notes:
1. 30000 μs/V at -10°C to 85°C.

Figure 81. Power-up Timing and Voltage Levels

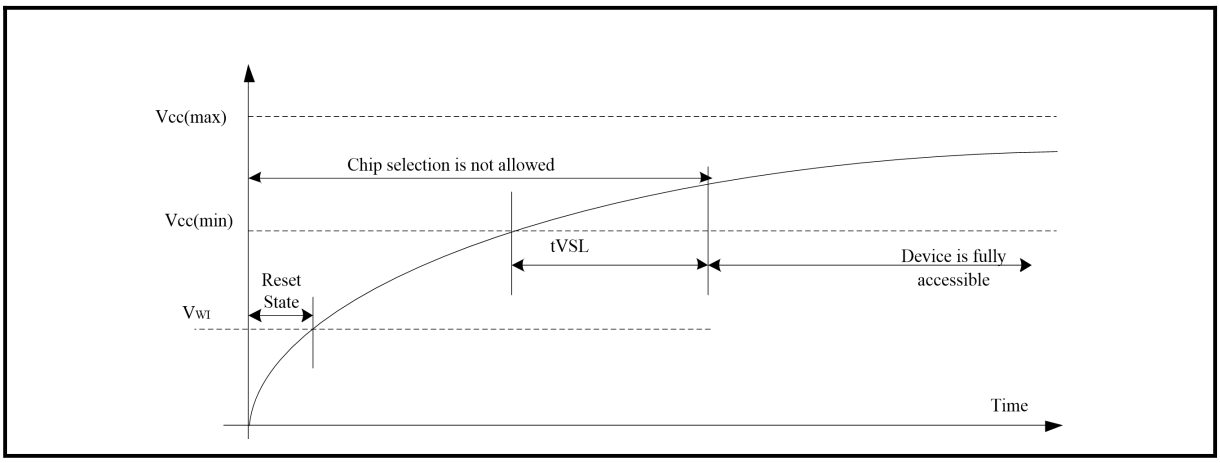
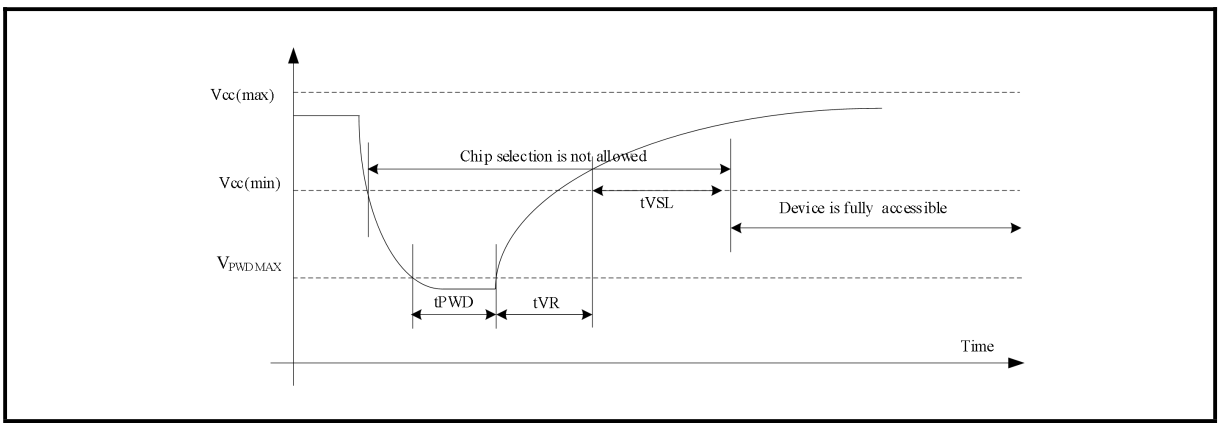


Figure 82. Power-Down Timing and Voltage Drop



8.5 DC Electrical Characteristics

(T= -40℃~85℃, VCC=2.7~3.6V)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
ILI	Input Leakage Current				±2	μA
ILO	Output Leakage Current				±2	μA
ICC1	Standby Current	/CS=VCC, VIN=VCC or VSS		9	40	μA
ICC2	Deep Power-Down Current	/CS=VCC, VIN=VCC or VSS		1	8	μA
ICC3	Operating Current: (Read)	SCLK=0.1VCC/ 0.9VCC, at 120MHz,Q=Open(*1,*,2*4 I/O)		7	15	mA
		SCLK=0.1VCC/ 0.9VCC, at 80MHz,Q=Open(*1,*,2*4 I/O)		6	12	mA
ICC4	Operating Current(Page Program)	/CS=VCC		6	12	mA
ICC5	Operating Current(WRSR)	/CS=VCC		7	12	mA
ICC6	Operating Current(Sector Erase)	/CS=VCC		7	12	mA
ICC7	Operating Current(Block Erase)	/CS=VCC		7	12	mA
ICC8	Operating Current (Chip Erase)	/CS=VCC		7	12	mA
VIL	Input Low Voltage		-0.5		0.2VCC	V
VIH	Input High Voltage		0.8VCC		VCC+0.4	V
VOL	Output Low Voltage	IOL =100μA			0.4	V
VOH	Output High Voltage	IOH =-100μA	VCC-0.2			V

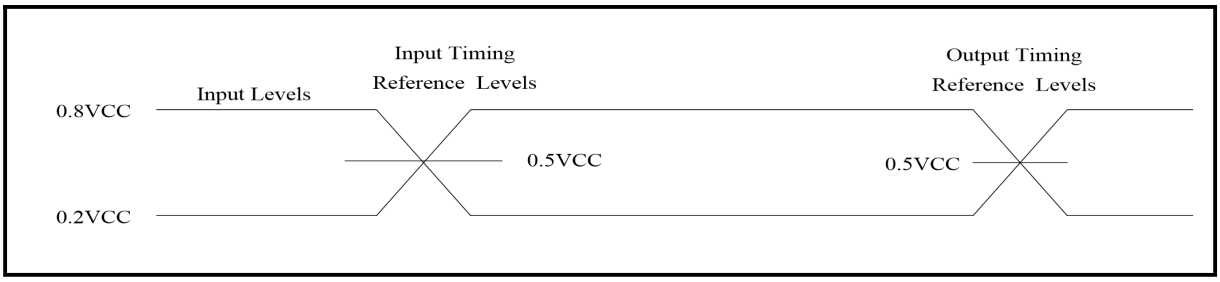
Notes:

1. Typical value at TA = 25℃, VCC = 3.3V.
2. Value guaranteed by design and/or characterization, not 100% tested in production.

8.6 AC Measurement Conditions

Symbol	Parameter	Min	Tpy.	Max	Unit.	Conditions
CL	Load Capacitance			30	pF	
TR, TF	Input Rise And Fall time			5	ns	
VIN	Input Pause Voltage	0.2VCC to 0.8VCC			V	
IN	Input Timing Reference Voltage	0.5VCC			V	
OUT	Output Timing Reference Voltage	0.5VCC			V	

Figure 83. AC Measurement I/O Waveform



8.7 AC Electrical Characteristics

(T= -40℃~85℃, VCC=2.7~3.6V)

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fc	Clock frequency for all instructions, except Read Data instruction (R=3.0~3.6V)	DC.		120/133 R	MHz
F_R	Clock frequency for Read Array instructions (0BH, 3BH) (R=3.0~3.6V)			133/166 R	MHz
F_R	Clock frequency for Read Array instructions (6BH) (R=3.0~3.6V)			120/133 R	MHz
F_R	Clock frequency for Read Array instructions (E7H)			84/104 R	MHz
F_R	Clock frequency for Read Array instructions (BBH, BCH, EBH, ECH)	Please refer to DC bit and Set Read Parameters (C0H)			MHz
F_R	Clock freq. for DTR instructions (0DH, BDH, EDH, 0EH)	Please refer to DC bit and Set Read Parameters (C0H)			MHz
fR	Clock freq. for Read Array instructions (03H)			88	MHz
tCLH	Serial Clock High Time	4			ns
tCLL	Serial Clock Low Time	4			ns
tCLCH	Serial Clock Rise Time (Slew Rate)	0.1(1)			V/ns
tCHCL	Serial Clock Fall Time (Slew Rate)	0.1(1)			V/ns
tSLCH	/CS Active Setup Time	5			ns
tCHSH	/CS Active Hold Time	5			ns
tSHCH	/CS Not Active Setup Time	5			ns
tCHSL	/CS Not Active Hold Time	5			ns
tSHSL	/CS High Time (read/write)	20			ns
tSHQZ	Output Disable Time			6	ns
tCLQX	Output Hold Time	0			ns
tDVCH	Data In Setup Time	2			ns
tCHDX	Data In Hold Time	2			ns
tHLCH	/Hold Low Setup Time (relative to Clock)	5			ns
tHHCH	/Hold High Setup Time (relative to Clock)	5			ns
tCHHL	/Hold High Hold Time (relative to Clock)	5			ns
tCHHH	/Hold Low Hold Time (relative to Clock)	5			ns
tHLQZ	/Hold Low To High-Z Output			6	ns
tHHQX	/Hold Low To Low-Z Output			6	ns
tCLQV	Clock Low To Output Valid (C_L=30pF)			7	ns
	Clock Low To Output Valid (C_L=10pF)			5	ns

tQSV	Clock transient to DQS valid time	Align to tCLQV	ns		
tDQSQ	SIO Valid Skew Related to DQS (SOP 16, 12pF)			0.6	ns
tQHS	SIO Hold Skew Factor (SOP 16, 12pF)			0.6	ns
tWHSL	Write Protect Setup Time Before /CS Low	20			ns
tSHWL	Write Protect Hold Time After /CS High	100			ns
tDP	/CS High To Deep Power-Down Mode			1	μs
tRES1	/CS High To Standby Mode Without Electronic Signature Read			20	μs
tRES2	/CS High To Standby Mode With Electronic Signature Read			20	μs
tESL	Erase Suspend Latency(3)			40	μs
tPSL	Program Suspend Latency(3)			30	μs
tPRS	Latency between Program Resume and next Suspend(4)	1	100		μs
tERS	Latency between Erase Resume and next Suspend(5)	1	100		μs
tRST	/CS High To Next Instruction After Reset in standby/read			1	μs
	/CS High To Next Instruction After Reset (except standby/read)			50	μs
tW	Write Status Register Cycle Time		2	30(2)	ms
tBP1	Byte Program Time (First Byte) (6)		90	300	μs
tBP2	Additional Byte Program Time (After First Byte) (6)		1.5	12	μs
tPP	Page Programming Time		0.16	1.2	ms
tSE	Sector Erase Time		25	400	ms
tBE	Block Erase Time(32K Bytes/64K Bytes)		0.06/ 0.12	2/4	S
tCE	Chip Erase Time		8	60	S

Notes:

1. Typical value at TA = 25℃.
2. Value guaranteed by design and/or characterization, not 100% tested in production.
3. Latency time is required to complete Erase/Program Suspend operation until WIP bit is "0".
4. For tPRS. minimum timing must be observed before issuing the next program suspend command. However, a period equal to or longer than the typical timing is required in order for the program operation to make progress.
5. For tERS, minimum timing must be observed before issuing the next erase suspend command. However, a period equal to or longer than the typical timing is required in order for the erase operation to make progress.
6. For multiple bytes after first byte within a page, tBPn = tBP1 + tBP2 * N, where N is the number of bytes programmed.

Figure 84. Serial input Timing

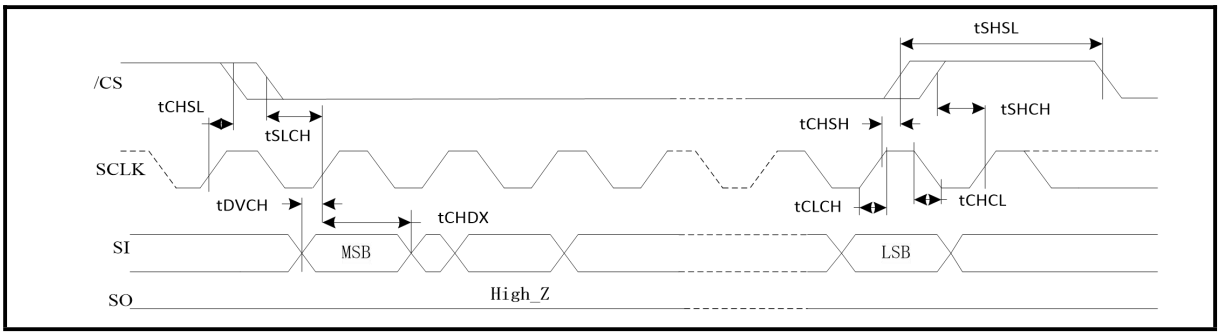


Figure 85. Output Timing

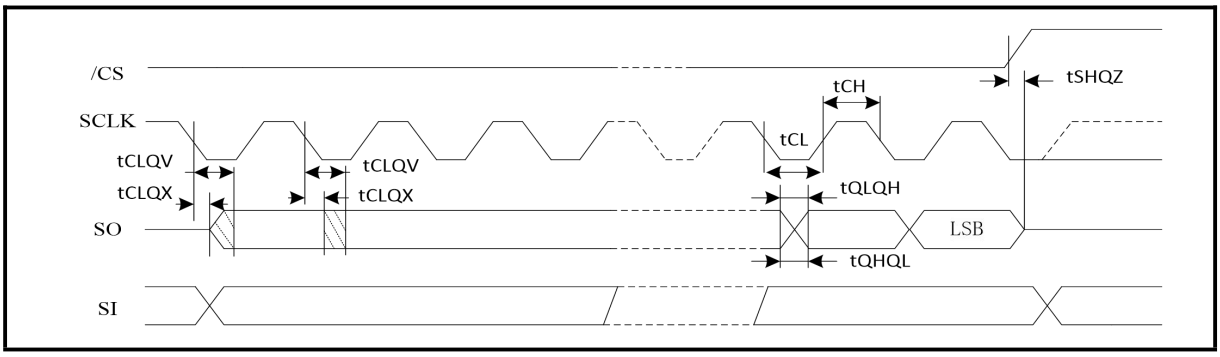


Figure 86. Hold Timing

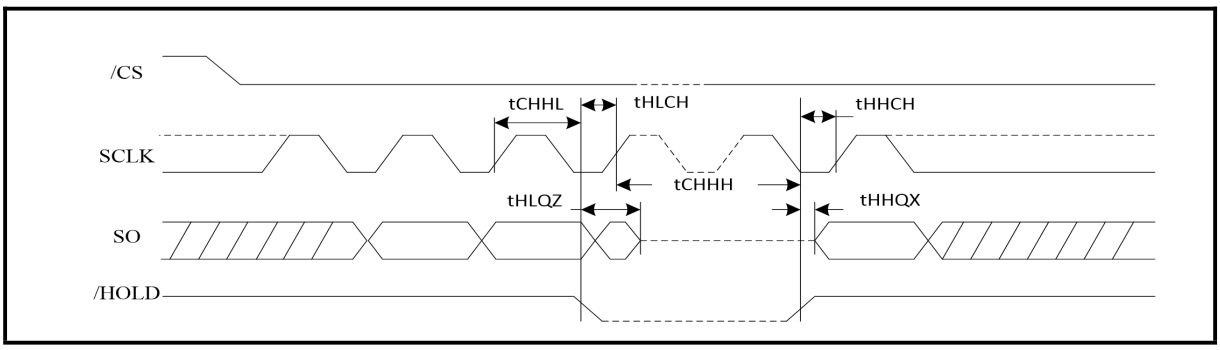


Figure 87. /WP Timing

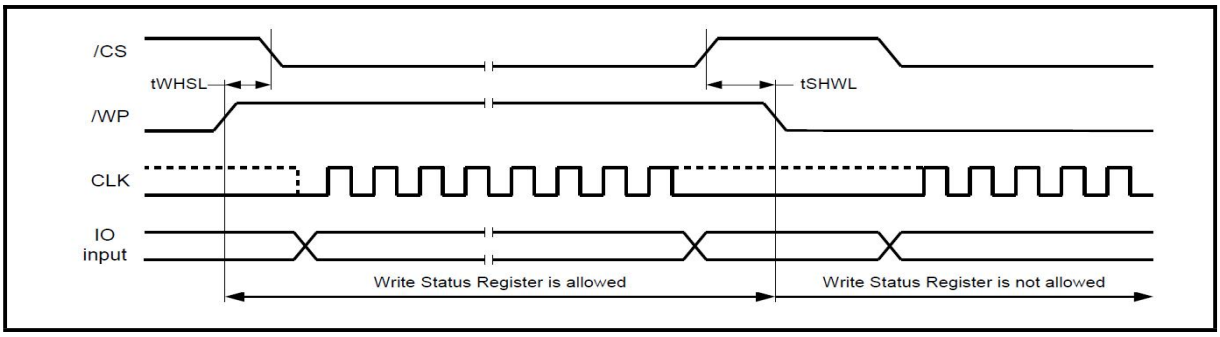


Figure 88. DQS Output Timing (DTR)

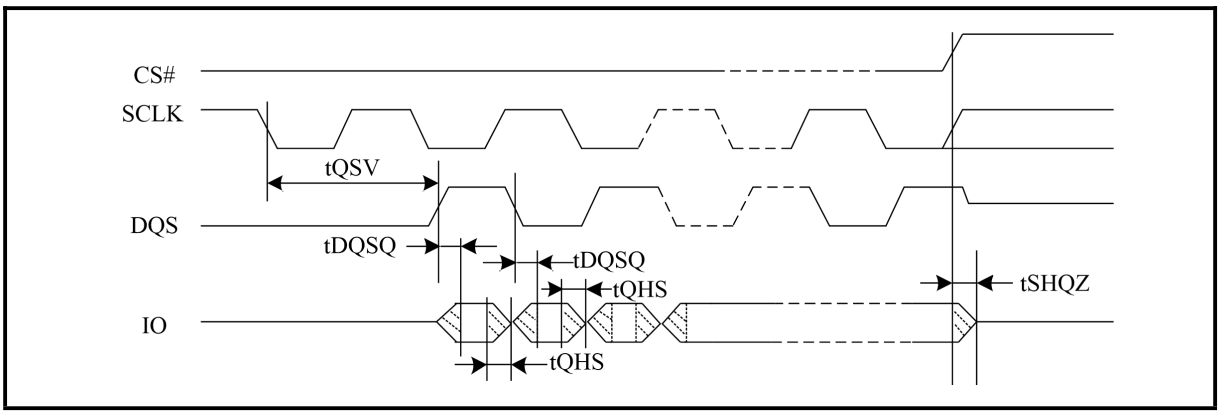
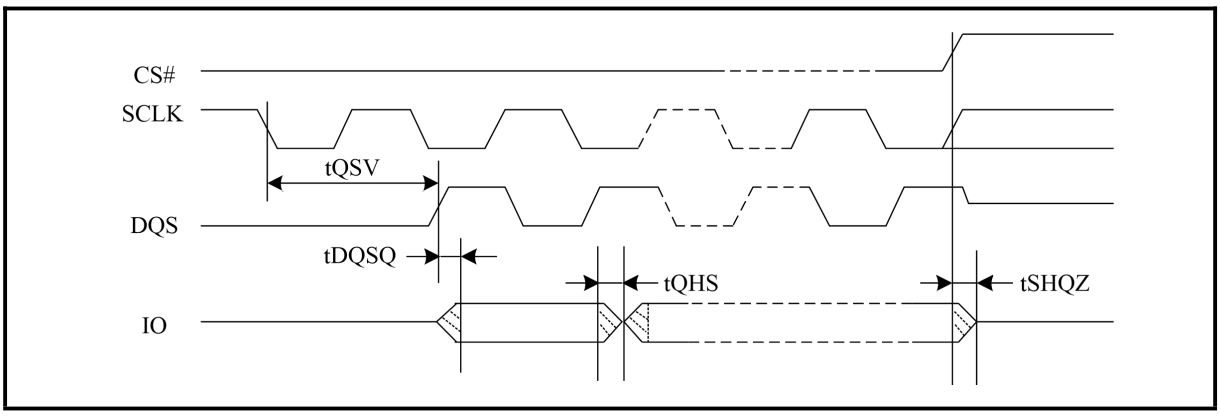
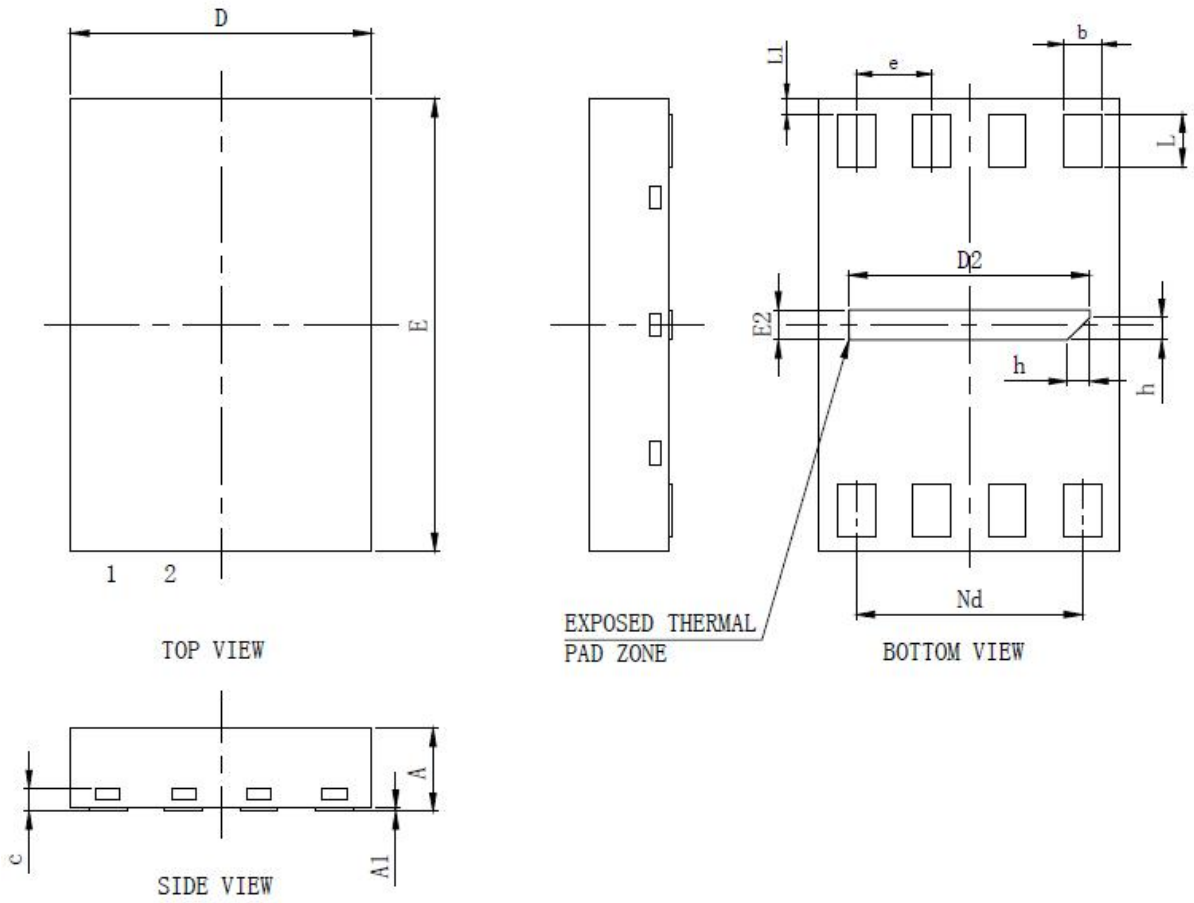


Figure 89. DQS Output Timing (Non DTR)



9. PACKAGE INFORMATION

9.1 Package 8-pad USON8 2*3mm(0.55mm)



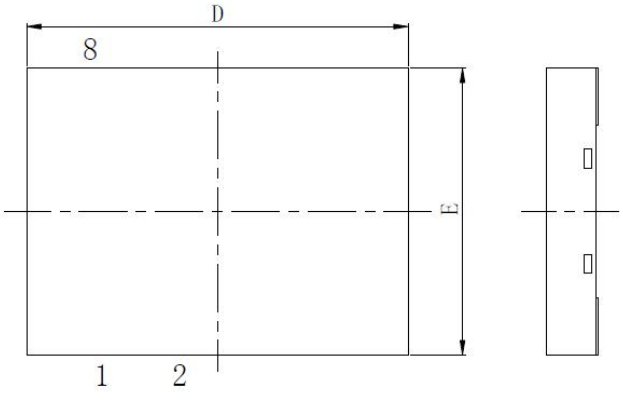
Dimensions

Symbol / Unit		A	A1	b	c	D	D2	e	Nd	E	E2	L	L1	h
mm	Min	0.50	0	0.20	0.10	1.90	1.50	0.50BSC	1.50BSC	2.90	0.10	0.30	0.05	0.05
	Nom	0.55	0.02	0.25	0.15	2.00	1.60			3.00	0.20	0.35	0.10	0.15
	Max	0.60	0.05	0.30	0.20	2.10	1.70			3.10	0.30	0.40	0.15	0.25

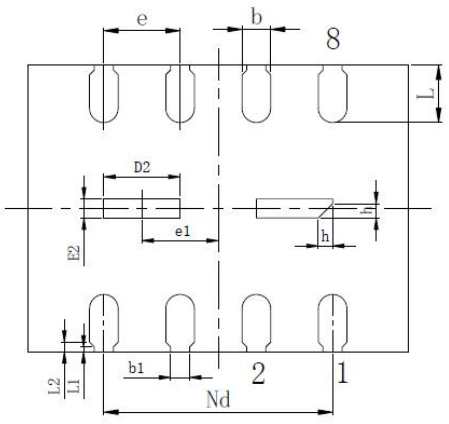
Note:

1、 The exposed metal pad area on the bottom of the package is floating.

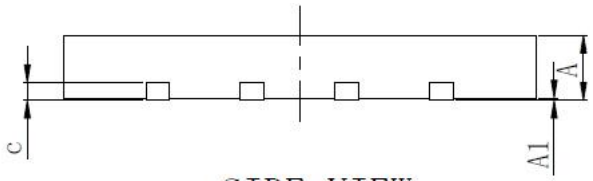
9.2 Package 8-pad USON8 4*3mm



TOP VIEW



BOTTOM VIEW



SIDE VIEW

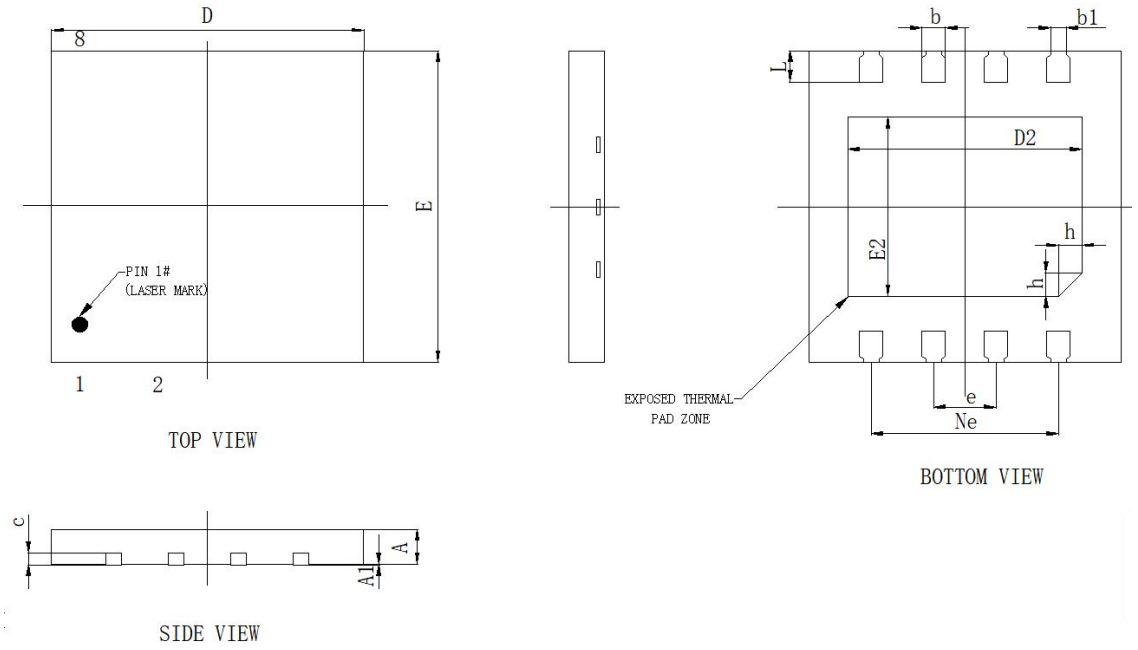
Dimensions

Symbol / Unit		A	A1	b	b1	c	D	Nd	e	e1	E	D2	E2	L	L1	L2	h
mm	Min	0.45	0	0.25	0.20 REF	0.10	3.90	2.40 BSC	0.80 BSC	0.80 BSC	2.90	0.70	0.10	0.55	0.50 REF	0.10 REF	0.10
	Nom	0.50	0.02	0.30		0.15	4.00				3.00	0.80	0.20	0.60			0.15
	Max	0.55	0.05	0.35		0.20	4.10				3.10	0.90	0.30	0.65			0.20

Note:

1. The exposed metal pad area on the bottom of the package is floating.

9.3 Package 8-pad USON8 4*4mm



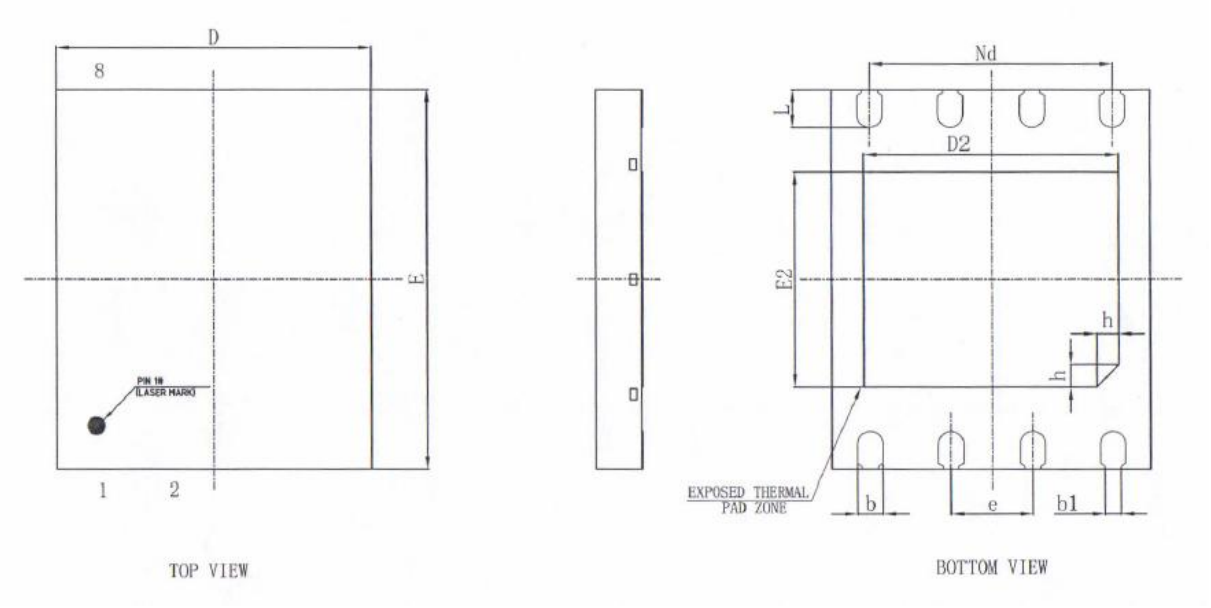
Dimensions

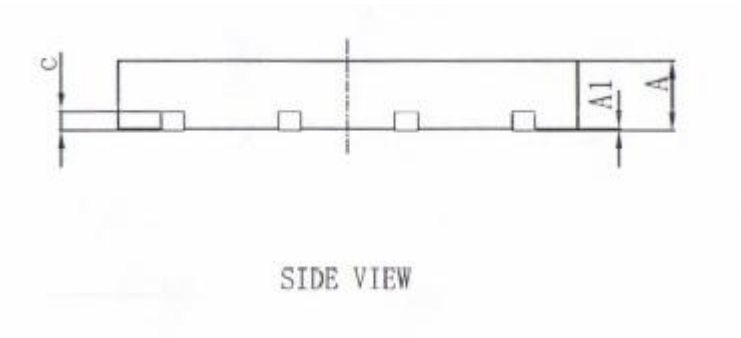
Symbol / Unit		A	A1	b	b1	c	D	Ne	e	E	D2	E2	L	h
mm	Min	0.45	0	0.25	0.15	0.10	3.90	2.40BSC	0.80BSC	3.90	2.90	2.20	0.35	0.25
	Nom	0.50	0.02	0.30	0.20	0.15	4.00			4.00	3.00	2.30	0.40	0.30
	Max	0.55	0.05	0.35	0.25	0.20	4.10			4.10	3.10	2.40	0.45	0.35

Note:

1. The exposed metal pad area on the bottom of the package is floating.

9.4 Package 8-pad WSON8 5*6mm





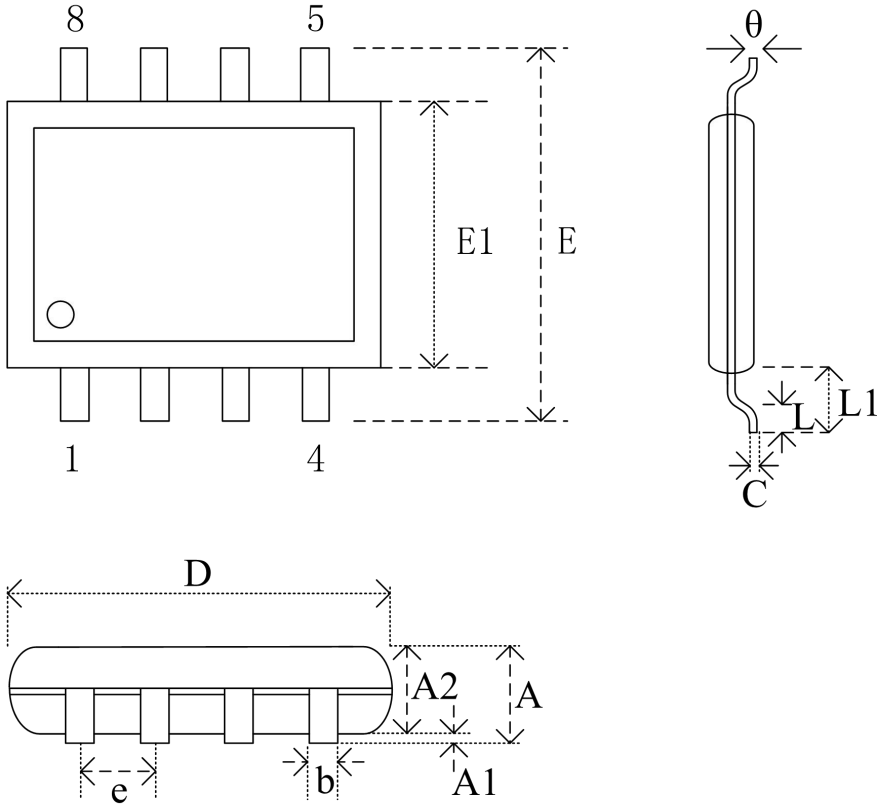
Dimensions

Symbol / Unit		A	A1	b	b1	c	D	Nd	e	E	D2	E2	L	h
mm	Min	0.70	0	0.35	0.25REF	0.18	4.90	3.81BSC	1.27BSC	5.90	3.90	3.30	0.50	0.30
	Nom	0.75	0.02	0.40		0.203	5.00			6.00	4.00	3.40	0.60	0.35
	Max	0.80	0.05	0.45		0.25	5.10			6.10	4.10	3.50	0.65	0.40

Note:

1. The exposed metal pad area on the bottom of the package is floating.

9.5 Package 8-Pin SOP8 150mil

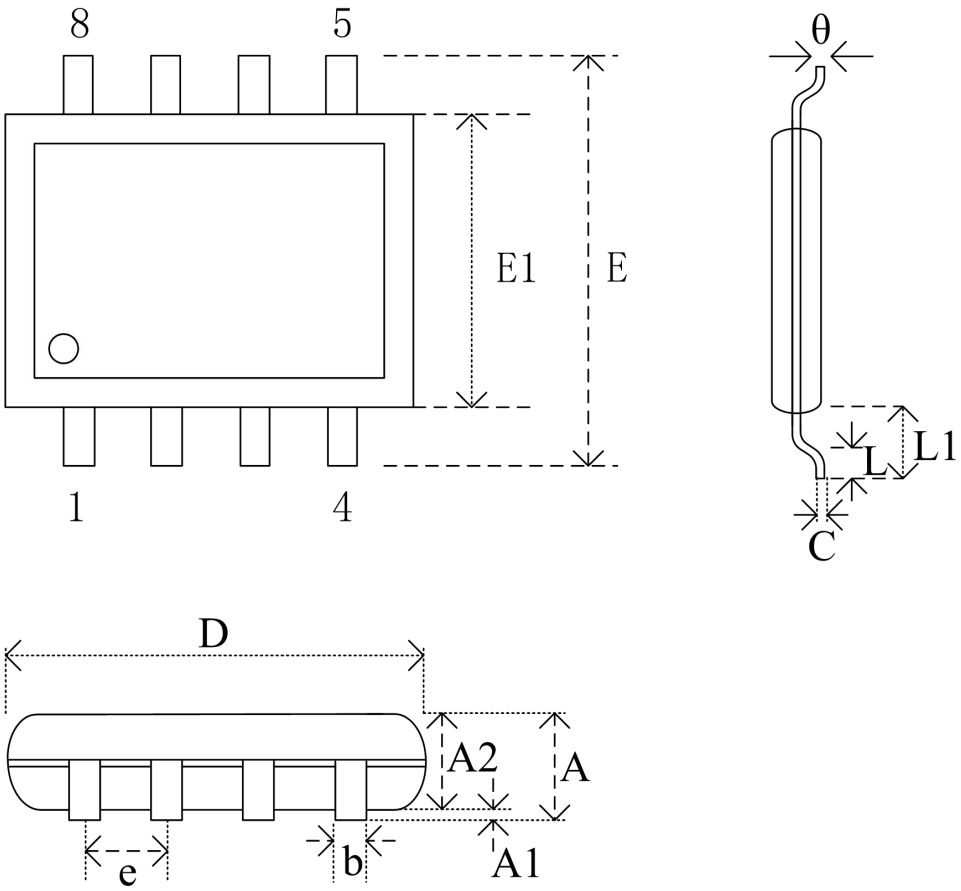


Dimensions

Symbol / Unit		A	A1	A2	b	C	*D	E	*E1	e	L	L1	θ
mm	Min	-	0.05	1.30	0.31	0.10	4.80	5.80	3.80	1.27BSC	0.40	1.05BSC	0°
	Nom	-	-	-	-	-	4.90	6.00	3.90		-		5°
	Max	1.75	0.25	1.55	0.50	0.25	5.00	6.20	4.00		1.00		8°

Note:
1、*D This size does not include burrs.
2、*E1 This size does not include burrs.

9.6 Package 8-Pin SOP8 208mil

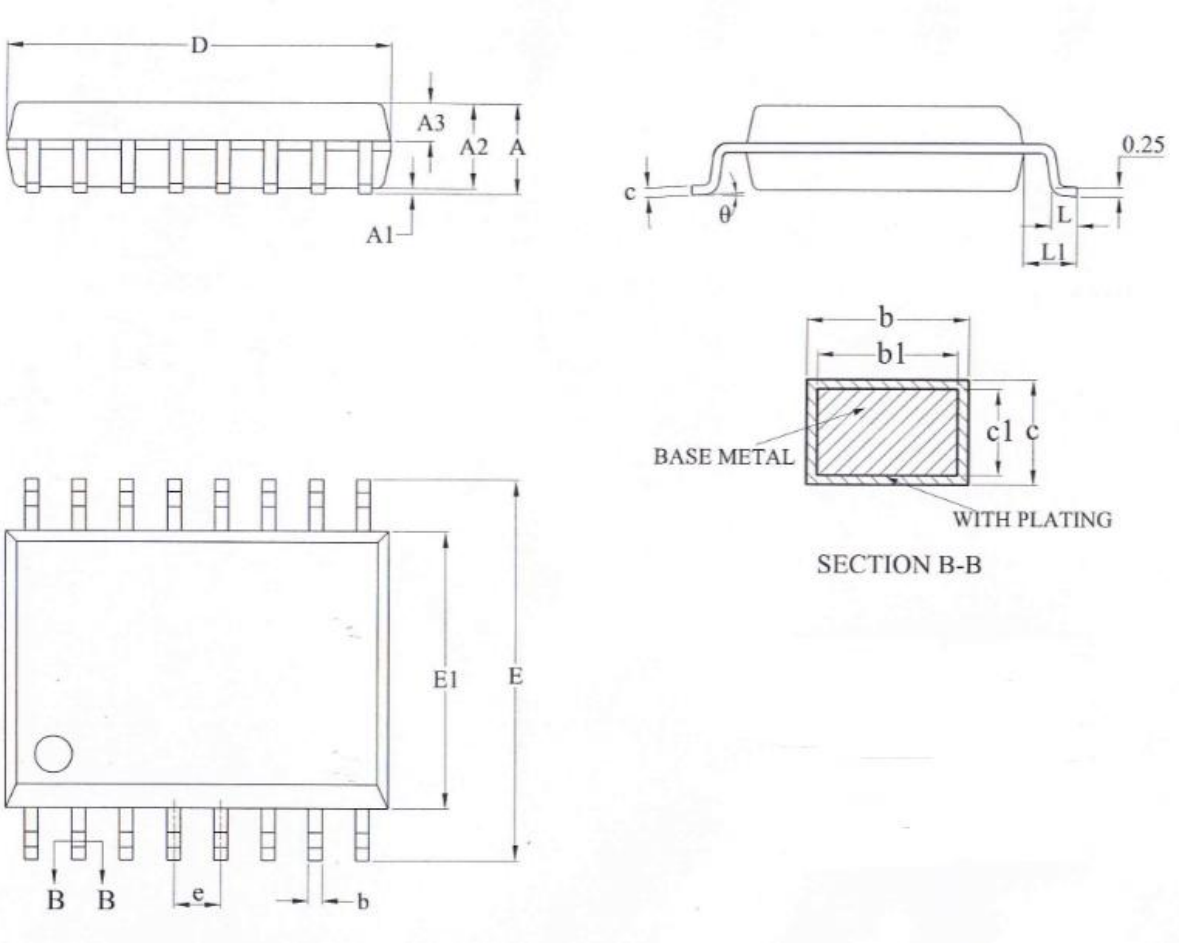


Dimensions

Symbol / Unit		A	A1	A2	b	C	*D	E	*E1	e	L	L1	θ
mm	Min	-	0.05	1.70	0.35	0.19	5.00	7.70	5.13	1.27BSC	0.50	1.31 REF.	0°
	Nom	-	0.15	1.80	-	-	-	7.90	-		0.65		5°
	Max	2.16	0.25	1.91	0.50	0.25	5.33	8.10	5.38		0.80		8°

Note:
1、*D This size does not include burrs.
2、*E1 This size does not include burrs.

9.7 Package 16-pin SOP16 300mil

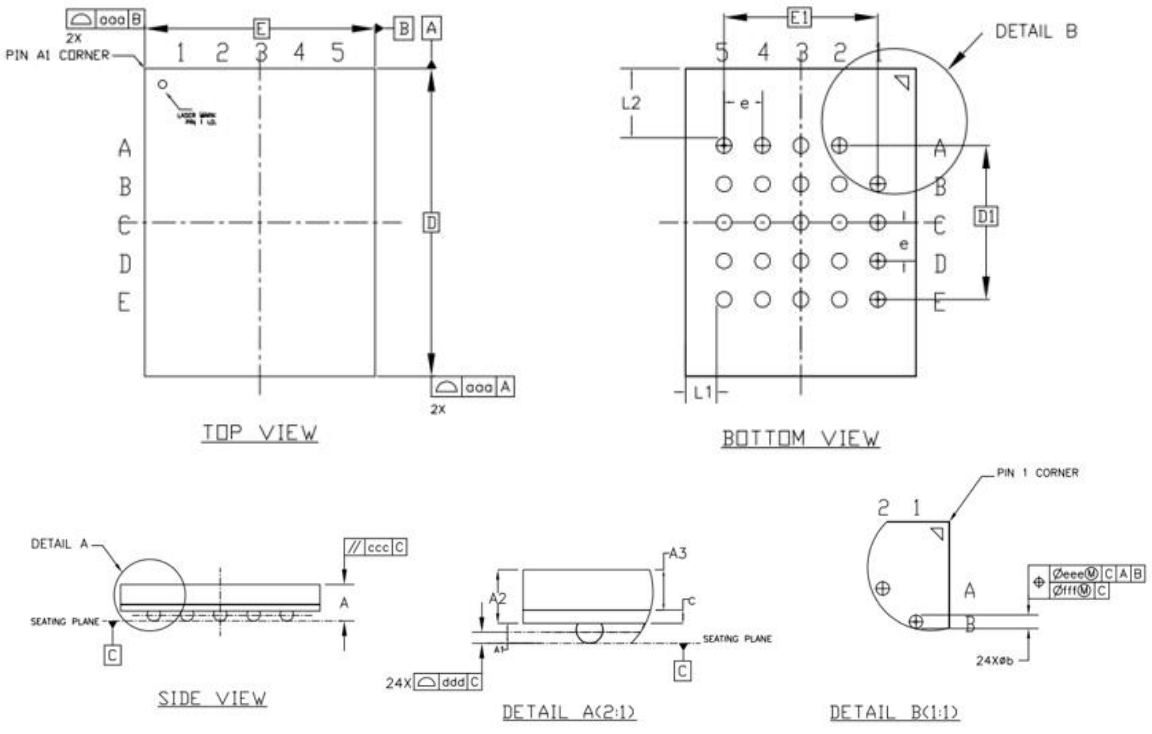


Dimensions

Symbol / Unit		A	A1	A2	A3	b	b1	c	c1	D*	E	E1*	e	L	L1	θ
mm	Min	-	0.10	2.05	0.97	0.31	0.34	0.25	0.24	10.20	10.10	7.40	1.27BSC	0.55	1.40REF	0°
	Nom	-	-	2.30	1.02	-	0.37	-	0.25	10.30	10.30	7.50		-		-
	Max	2.65	0.30	2.35	1.07	0.51	0.40	0.29	0.26	10.40	10.50	7.60		0.85		8°

Note:
1、*D This size does not include burrs.
2、*E1 This size does not include burrs.

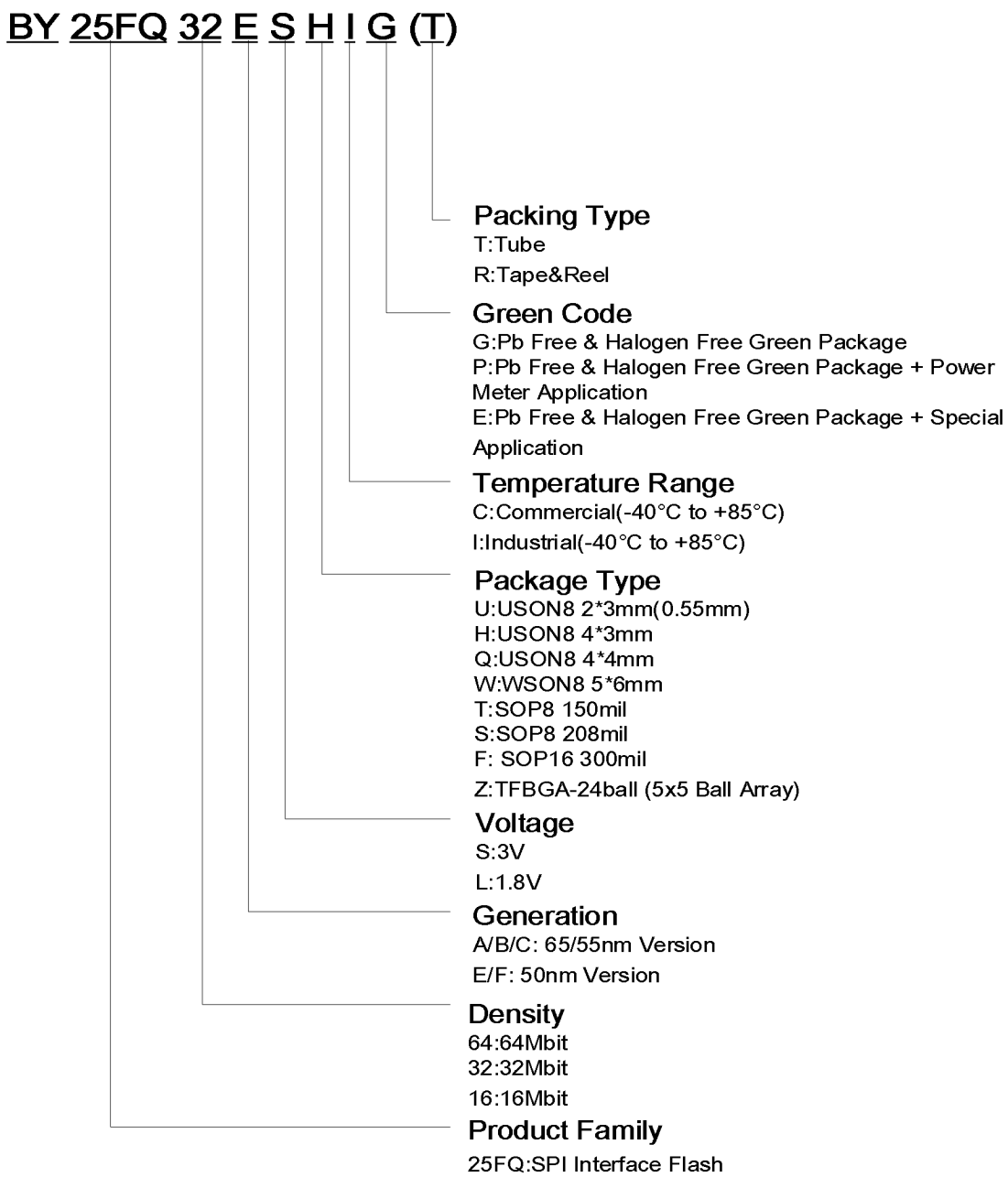
9.8 Package TFBGA-24ball (5x5 Ball Array)



Dimensions

Symbol / Unit		A	A1	A2	A3	c	D	D1	E	E1	e	b	L1	L2	aaa	ccc	ddd	eee	fff
mm	Min	1.02	0.25	0.75	0.55	0.17	7.90	3.90	5.90	3.90		0.35							
	Nom	1.10	0.30	0.80	0.60	0.20	8.00	4.00	6.00	4.00	1.00 BASIC	0.40	0.80 REF	1.80 REF	0.10	0.20	0.12	0.15	0.08
	Max	1.20	0.35	0.85	0.65	0.23	8.10	4.10	6.10	4.10		0.45							

10. ORDER INFORMATION



10.1 Valid part Numbers and Top Side Marking

The following table provides the valid part numbers for BY25FQ32ES SPI Flash Memory. Pls contact BY Technology for specific availability by density and package type.

For consumer and 85℃ industry application:

Package Type	Density	Product Number	Top Side Marking
U USON8 2*3mm (0.55mm)	32M-bit	BY25FQ32ESUIG	 FQ32ES UIYYWW
H USON8 4*3mm (0.50mm)	32M-bit	BY25FQ32ESHIG	 25FQ32ESHI YYWW
Q USON8 4*4mm (0.50mm)	32M-bit	BY25FQ32ESQIG	 25FQ32ESQ YYWW
W WSON8 5*6mm	32M-bit	BY25FQ32ESWIG	 25FQ32ESWI YYWW
T SOP8 150mil	32M-bit	BY25FQ32ESTIG	BYT 25FQ32ESTI YYWW
S SOP8 208mil	32M-bit	BY25FQ32ESSIG	BYT 25FQ32ESSI YYWW
F SOP16 300mil	32M-bit	BY25FQ32ESFIG	BYT 25FQ32ESFIG YYWW
Z TFBGA-24ball (5x5 Ball Array)	32M-bit	BY25FQ32ESZIG	 25FQ32ESZIG YYWW

10.2 Minimum Packing Quantity (MPQ)

Package Type	Packing Type	Qty for 1 Tube or Reel	Vacuum bag/ Inner Box	MPQ
USON8 2*3mm(0.55mm)	Tape&Reel (7inch)	3000ea/Reel	1Reel/Bag 10Bag/InnerBox	30,000
USON8 4*3mm	Tape&Reel (13inch)	3000ea/Reel	1Reel/Bag 1Bag/InnerBox	3,000
USON8 4*4mm	Tape&Reel (13inch)	3000ea/Reel	1Reel/Bag 1Bag/InnerBox	3,000
WSON8 5*6mm	Tape&Reel (13inch)	3000ea/Reel	1Reel/Bag 1Bag/InnerBox	3,000
SOP8 150mil	Tube	100ea/Tube	100Tubes/Bag 1Bag/InnerBox	10,000
	Tape&Reel (13inch, 12mm)	4000ea/Reel	1Reel/Bag 1Bags/InnerBox	4,000
SOP8 208mil	Tube	95ea/Tube	100Tubes/Bag 1Bag/InnerBox	9,500
	Tape&Reel (13inch, 16mm)	2000ea/Reel	1Reel/Bag 2Bags/InnerBox	4,000
SOP16 300mil	Tube	44ea/Tube	80Tubes/Bag 1Bag/InnerBox	3,520
	Tape&Reel (13inch)	1500ea/Reel	1Reel/Bag 1Bag/InnerBox	1500
TFBGA-24ball (5x5 Ball Array)	Tray	480ea/Tray	10+1 Trays/Bag 1Bag/InnerBox	4800

11. DOCUMENT CHANGE HISTORY

REVISION	CHANGE DESCRIPTION	CLAUSE	ORIGINATOR DATE
1.0	Initiate	/	Xingyue Huang Dongfu Yan 2025-5-23