DATASHEET

FOR

512K BIT SPI NOR FLASH

BY25D05AS

Features

- **Serial Peripheral Interface (SPI)**
  - Standard SPI: SCLK, /CS, SI, SO, /WP
  - Dual SPI: SCLK, /CS, IO0, IO1, /WP
- **Read**
  - Normal Read (Serial): 55MHz clock rate
  - Fast Read (Serial): 108MHz clock rate
  - Dual Read: 108MHz clock rate
- **Program**
  - Serial-input Page Program up to 256bytes
- **Erase**
  - Block erase (64/32 KB)
  - Sector erase (4 KB)
  - Chip erase
- **Program/Erase Speed**
  - Page Program time: 0.7ms typical
  - Sector Erase time: 100ms typical
  - Block Erase time: 0.3/0.5s typical
  - Chip Erase time: 0.5s typical
- **Flexible Architecture**
  - Sector of 4K-byte
  - Block of 32/64K-byte
- **Low Power Consumption**
  - 20mA maximum active current
  - 5uA maximum power down current
- **Software/Hardware Write Protection**
  - Enable/Disable protection with WP Pin
  - Write protect all/portion of memory via software
  - Top or Bottom, Sector or Block selection
- **Single Supply Voltage**
  - Full voltage range: 2.7~3.6V。
- **Temperature Range**
  - Commercial (0℃ to +70℃)
  - Industrial (-40℃ to +85℃)
- **Cycling Endurance/Data Retention**
  - Typical 100k Program-Erase cycles on any sector
  - Typical 20-year data retention

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1. Description

The BY25D05AS is 512K-bit Serial Peripheral Interface (SPI) Flash memory, and supports the Dual SPI: Serial Clock, Chip Select, Serial Data I/O0 (SI), I/O1 (SO). The Dual Output data is transferred with speed of 108Mbits/s. The device uses a single low voltage power supply, ranging from 2.7 Volt to 3.6 Volt.

Additionally, the device supports JEDEC standard manufacturer and device ID.

In order to meet environmental requirements, BY Technology offers an 8-pin SOP 150-mil, or 208mil,an 8-pin TSSOP 173-mil, an 8-pad USON 3x2-mm, and other special order packages, please contacts BY Technology for ordering information.

Figure 1. Logic diagram

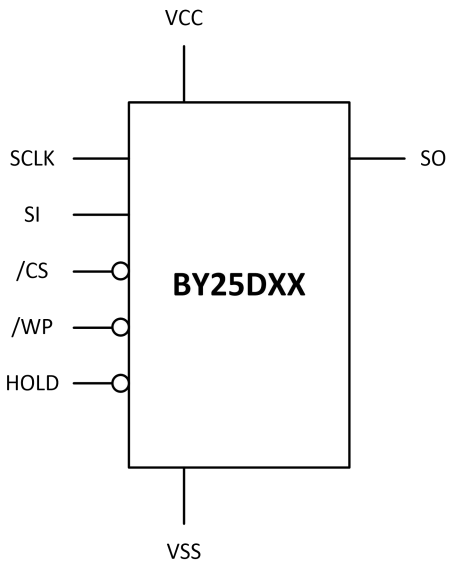


Figure 2. Pin Configuration SOP8 150/208mil, TSSOP 173mil

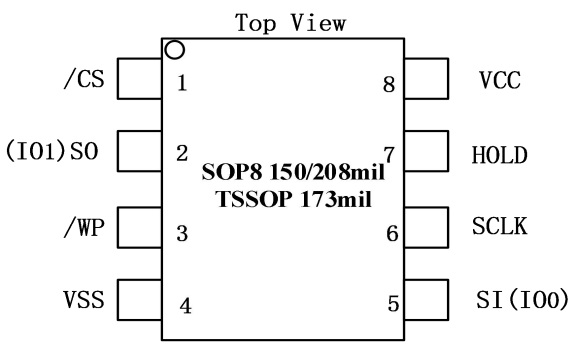
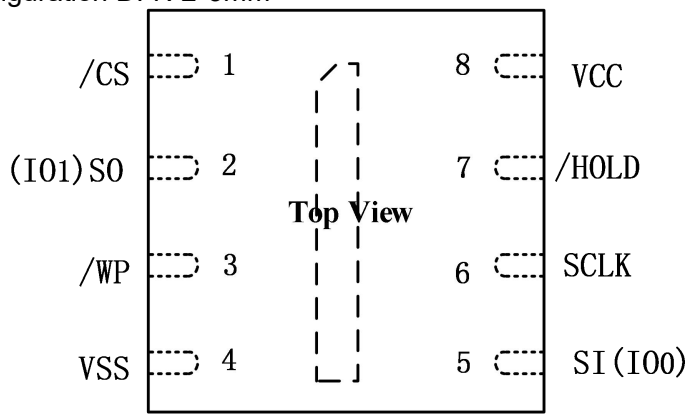


Figure 3. Pin Configuration DFN 2*3mm



2. Signal Description

During all operations, VCC must be held stable and within the specified valid range: VCC(min) to VCC(max).

All of the input and output signals must be held High or Low (according to voltages of VIH, VOH, VIL or VOL, see Section 8.6, DC Electrical Characteristics on *page 32*). These signals are described next.

Table 1. Signal Description

Pin Name	I/O	Description
/CS	I	Chip Select
SO (IO1)	I/O	Serial Output for single bit data Instructions. IO1 for Dual Instructions.
/WP	I	Write Protect in single bit
VSS		Ground
SI (IO0)	I/O	Serial Input for single bit data Instructions. IO0 for Dual Instructions.
SCLK	I	Serial Clock
HOLD		It must be higher than VIH
VCC		Core and I/O Power Supply

3. Block/Sector Addresses

Table 2. Block/Sector Addresses of BY25D05AS

Memory Density	Block(64k byte)	Block(32k byte)	Sector No.	Sector Size(KB)	Address range
512Kbit	Block 0	Half block 0	Sector 0	4	000000h-000FFFh
			:	:	:
			Sector 7	4	007000h-007FFFh
		Half block 1	Sector 8	4	008000h-008FFFh
			:	4	:
			Sector 15	4	00F000h-00FFFFh

Notes:
1. Block = Uniform Block, and the size is 64K bytes.
2. Half block = Half Uniform Block, and the size is 32k bytes.
3. Sector = Uniform Sector, and the size is 4K bytes.

4. SPI Operation

4.1 Standard SPI Instructions

The BY25D05AS features a serial peripheral interface on 4 signals bus: Serial Clock (SCLK), Chip Select (/CS), Serial Data Input (SI) and Serial Data Output (SO). Both SPI bus mode 0 and 3 are supported. Input data is latched on the rising edge of SCLK and data shifts out on the falling edge of SCLK.

4.2 Dual SPI Instructions

The BY25D05AS supports Dual SPI operation when using the “Dual Output Fast Read” (3BH) instructions. These instructions allow data to be transferred to or from the device at two times the rate of the standard SPI. When using the Dual SPI instruction the SI and SO pins become bidirectional I/O pins: IO0 and IO1.

5. Operation Features

5.1 Supply Voltage

5.1.1 Operating Supply Voltage

Prior to selecting the memory and issuing instructions to it, a valid and stable VCC voltage within the specified [VCC(min), VCC(max)] range must be applied (see operating ranges of *page 30*). In order to secure a stable DC supply voltage, it is recommended to decouple the VCC line with a suitable capacitor (usually of the order of 10 *nF* to 100 *nF*) close to the VCC/VSS package pins. This voltage must remain stable and valid until the end of the transmission of the instruction and, for a Write instruction, until the completion of the internal write cycle (tW).

5.1.2 Power-up Conditions

When the power supply is turned on, VCC rises continuously from VSS to VCC. During this time, the Chip Select (/CS) line is not allowed to float but should follow the VCC voltage, it is therefore recommended to connect the /CS line to VCC via a suitable pull-up resistor.

In addition, the Chip Select (/CS) input offers a built-in safety feature, as the /CS input is edge sensitive as well as level sensitive: after power-up, the device does not become selected until a falling edge has first been detected on Chip Select (/CS). This ensures that Chip Select (/CS) must have been High, prior to going Low to start the first operation.

5.1.3 Device Reset

In order to prevent inadvertent Write operations during power-up (continuous rise of VCC), a power on reset (POR) circuit is included. At Power-up, the device does not respond to any instruction until VCC has reached the power on reset threshold voltage (this threshold is lower than the minimum VCC operating voltage defined in operating ranges of *page 30*).

When VCC has passed the POR threshold, the device is reset.

5.1.4 Power-down

At Power-down (continuous decrease in VCC), as soon as VCC drops from the normal operating voltage to below the power on reset threshold voltage, the device stops responding to any instruction sent to it. During Power-down, the device must be deselected (Chip Select (/CS) should be allowed to follow the voltage applied on VCC) and in Standby Power mode (that is there should be no internal Write cycle in progress).

5.2 Active Power and Standby Power Modes

When Chip Select (/CS) is Low, the device is selected, and in the Active Power mode. The device consumes ICC.

When Chip Select (/CS) is High, the device is deselected. If a Write cycle is not currently in progress, the device then goes in to the Standby Power mode, and the device consumption drops to ICC1.

5.3 Status Register

Table 3. Status Register

S7	S6	S5	S4	S3	S2	S1	S0
SRP	Reserved	Reserved	BP2	BP1	BP0	WEL	WIP

The status and control bits of the Status Register are as follows:

WIP bit

The Write in Progress (WIP) bit indicates whether the memory is busy in program/erase/write status register progress. When WIP bit sets to 1, means the device is busy in program/erase/write status register progress, when WIP bit sets 0, means the device is not in program/erase/write status register progress.

WEL bit

The Write Enable Latch bit indicates the status of the internal Write Enable Latch. When set to 1 the internal Write Enable Latch is set, when set to 0 the internal Write Enable Latch is reset and no Write Status Register, Program or Erase instruction is accepted.

BP2, BP1, BP0 bits

The Block Protect (BP2, BP1, BP0) bits are non-volatile. They define the size of the area to be software protected against Program and Erase instructions. These bits are written with the Write Status Register instruction. When the Block Protect (BP2, BP1, BP0) bits are set to 1, the relevant memory area. Becomes protected against Page Program, Sector Erase and Block Erase instructions. The Block Protect (BP2, BP1, BP0) bits can be written provided that the Hardware Protected mode has not been set.

SRP bits

The Status Register Protect (SRP) bit operates in conjunction with the Write Protect (WP#) signal. The Status Register Write Protect (SRP) bit and Write Protect (WP#) signal set the device to the Hardware Protected mode. When the Status Register Protect (SRP) bit is set to 1, and Write Protect (WP#) is driven Low. In this mode, the non-volatile bits of the Status Register (SRP, BP2, BP1, BP0) become read-only bits and the Write Status Register (WRSR) instruction is not execution. The default value of SRP is 0.

5.3.1 Write Protect Features

1. Software Protection: The Block Protect (BP2, BP1, BP0) bits define the section of the memory array that can be read but not change.
2. Hardware Protection: /WP going low to protected the BP0~BP2 bits and SRP bits.
3. Deep Power-Down: In Deep Power-Down Mode, all instructions are ignored except the Release from deep Power-Down Mode instruction.
4. Write Enable: The Write Enable Latch (WEL) bit must be set prior to every Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register and Erase/Program Security Registers instruction.

5.4 Status Register Memory Protection

5.4.1.1 Protect Table

Table 4. BY25D05AS Status Register Memory Protection

Status Register Content			Memory Content			
BP2	**BP1**	**BP0**	**Blocks**	**Addresses**	**Density**	**Portion**
0	0	0	NONE	NONE	NONE	NONE
0	0	1	Sector 0 to29	000000H-00DFFFH	56KB	Lower14/16
0	1	0	Sector 0 to 27	000000H-00BFFFH	48KB	Lower 12/16
0	1	1	Sector 0 to 23	000000H-007FFFH	32KB	Lower 8/16
1	X	x	ALL	000000H-00FFFFH	64KB	ALL

6. Device Identification

Three legacy Instructions are supported to access device identification that can indicate the manufacturer, device type, and capacity (density). The returned data bytes provide the information as shown in the below table.

BY25D05AS ID Definition table

Operation Code	M7-M0	ID15-ID8	ID7-ID0
9FH	68	40	10
90H	68		05
ABH			05

7. Instructions Description

All instructions, addresses and data are shifted in and out of the device, beginning with the most significant bit on the first rising edge of SCLK after /CS is driven low. Then, the one byte instruction code must be shifted in to the device, most significant bit first on SI, each bit being latched on the rising edges of SCLK.

See *Table 5*, every instruction sequence starts with a one-byte instruction code. Depending on the instruction, this might be followed by address bytes, or by data bytes, or by both or none. /CS must be driven high after the last bit of the instruction sequence has been shifted in. For the instruction of Read, Fast Read, Read Status Register or Release from Deep Power Down, and Read Device ID, the shifted-in instruction sequence is followed by a data out sequence. /CS can be driven high after any bit of the data-out sequence is being shifted out.

For the instruction of Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register, Write Enable, Write Disable or Deep Power-Down instruction, /CS must be driven high exactly at a byte boundary, otherwise the instruction is rejected, and is not executed. That is /CS must drive high when the number of clock pulses after /CS being driven low is an exact multiple of eight. For Page Program, if at any time the input byte is not a full byte, nothing will happen and WEL will not be reset.

Table 5. Instruction Set Table

Instruction Name	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6
Write Enable	06H					
Write Disable	04H					
Read Status Register	05H	(S7-S0)				
Write Status Register	01H	(S7-S0)				
Read Data	03H	A23-A16	A15-A8	A7-A0	(D7-D0)	Next byte
Fast Read	0BH	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)
Dual Output Fast Read	3BH	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)(1)
Page Program	02H	A23-A16	A15-A8	A7-A0	(D7-D0)	Next byte
Sector Erase	20H	A23-A16	A15-A8	A7-A0		
Block Erase(32K)	52H	A23-A16	A15-A8	A7-A0		
Block Erase(64K)	D8H	A23-A16	A15-A8	A7-A0		
Chip Erase	C7/60H					
Deep Power-Down	B9H					
Release From Deep Power-Down, And Read Device ID	ABH	dummy	dummy	dummy	(ID7-ID0)	
Release From Deep Power-Down	ABH					
Manufacturer/ Device ID	90H	dummy	dummy	00H	(M7-M0)	(ID7-ID0)
JEDEC ID	9FH	(M7-M0)	(ID15-ID8)	(ID7-ID0)		

Notes:

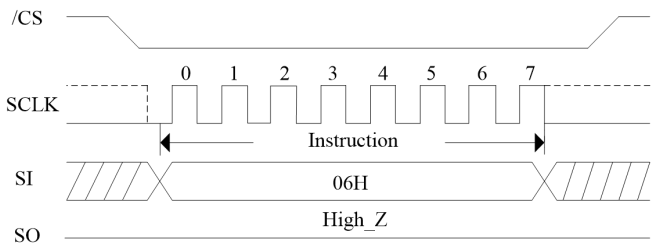
1. Dual Output data
   IO0 = (D6, D4, D2, D0)
   IO1 = (D7, D5, D3, D1)

7.1 Configuration and Status Instructions

7.1.1 Write Enable (06H)

See *Figure 4,* the Write Enable instruction is for setting the Write Enable Latch bit. The Write Enable Latch bit must be set prior to every Page Program, Sector Erase, Block Erase, Chip Erase and Write Status Register instruction. The Write Enable instruction sequence: /CS goes low sending the Write Enable instruction /CS goes high.

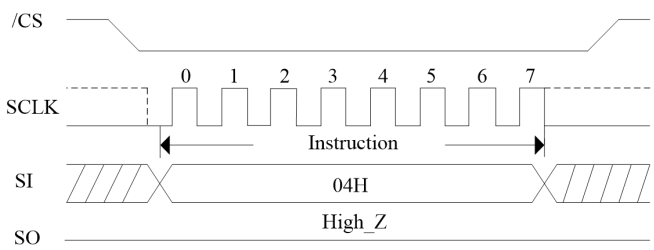
Figure 4. Write Enable Sequence Diagram



7.1.2 Write Disable (04H)

See *Figure 5,* the Write Disable instruction is for resetting the Write Enable Latch bit. The Write Disable instruction sequence: /CS goes low sending the Write Disable instruction /CS goes high. The WEL bit is reset by following condition: Power-up and upon completion of the Write Status Register, Page Program, Sector Erase, Block Erase and Chip Erase instructions.

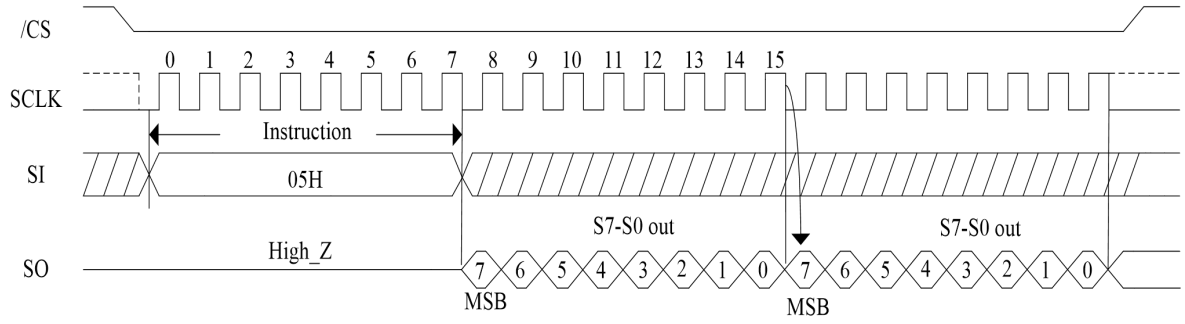
Figure 5. Write Disable Sequence Diagram



7.1.3 Read Status Register (05H)

See *Figure 6* the Read Status Register (RDSR) instruction is for reading the Status Register. The Status Register may be read at any time, even while a Program, Erase or Write Status Register cycle is in progress. When one of these cycles is in progress, it is recommended to check the Write in Progress (WIP) bit before sending a new instruction to the device. It is also possible to read the Status Register continuously. For instruction code “05H”, the SO will output Status Register bits S7~S0.

Figure 6. Read Status Register Sequence Diagram

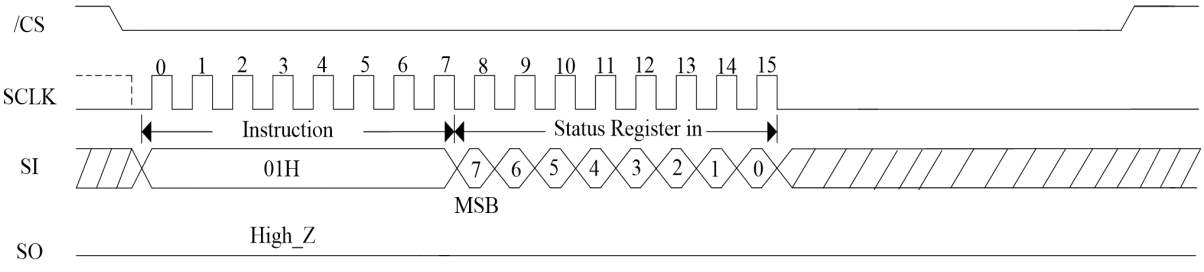


7.1.4 Write Status Register (01H)

See *Figure 7,* the Write Status Register instruction allows new values to be written to the Status Register. Before it can be accepted, a Write Enable instruction must previously have been executed. After the Write Enable instruction has been decoded and executed, the device sets the Write Enable Latch (WEL).

The Write Status Register instruction has no effect on S6, S5, S1 and S0 of the Status Register. S6 and S5 are always read as 0. /CS must be driven high after the eighth bit of the data byte has been latched in. If not, the Write Status Register instruction is not executed. As soon as Chip Select (CS#) is driven High, the self-timed Write Status Register cycle (the duration is tW) is initiated. While the Write Status Register cycle is in progress, reading Status Register to check the Write In Progress (WIP) bit is achievable. The Write In Progress (WIP) bit is 1 during the self-timed Write Status Register cycle, and turn to 0 on the completion of the Write Status Register. When the cycle is completed, the Write Enable Latch (WEL) is reset to 0. The Write Status Register (WRSR) instruction allows the user to change the values of the Block Protect (BP2, BP1, BP0) bits, which are utilized to define the size of the read-only area. The Write Status Register (WRSR) instruction also allows the user to set or reset the Status Register Protect (SRP) bit in accordance with the Write Protect (WP#) signal, by setting which the device can enter into Hardware Protected Mode (HPM). The Write Status Register (WRSR) instruction is not executed once enter into the Hardware Protected Mode (HPM).

Figure 7. Write Status Register Sequence Diagram

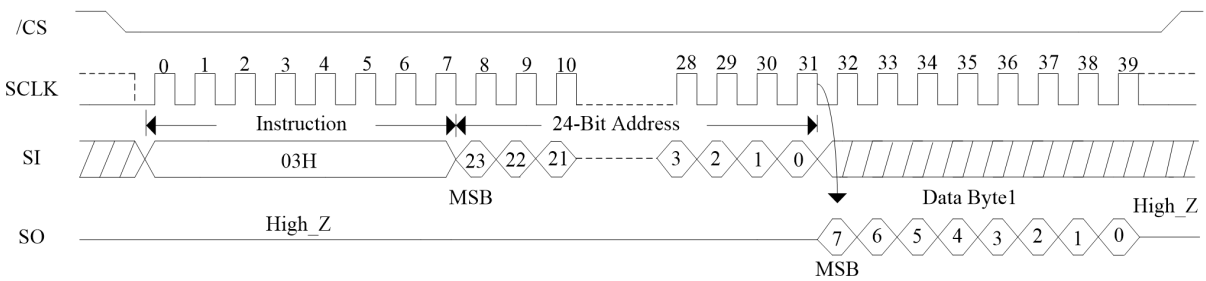


7.2 Read Instructions

7.2.1 Read Data (03H)

See *Figure 8,* the Read Data Bytes (READ) instruction is followed by a 3-byte address (A23-A0), each bit being latched-in during the rising edge of SCLK. Then the memory content, at that address, is shifted out on SO, each bit being shifted out, at a Max frequency fR, during the falling edge of SCLK. The address is automatically incremented to the next higher address after each byte of data is shifted out allowing for a continuous stream of data. This means that the entire memory can be accessed with a single command as long as the clock continues. The command is completed by driving /CS high. The whole memory can be read with a single Read Data Bytes (READ) instruction. Any Read Data Bytes (READ) instruction, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress. Normal read mode running up to 55MHz.

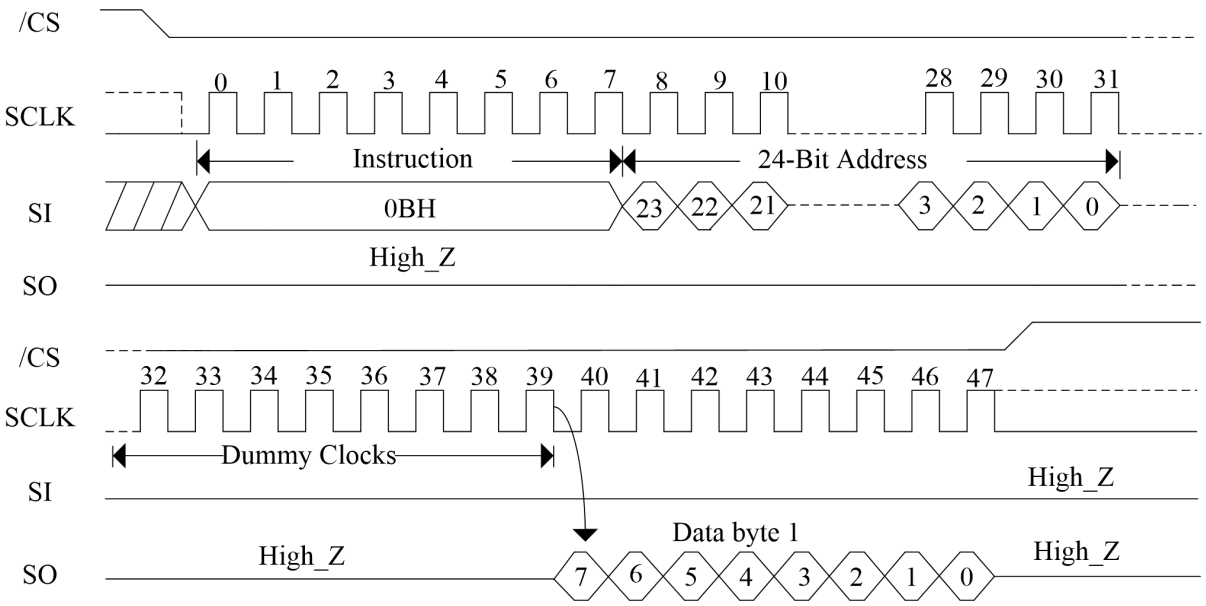
Figure 8. Read Data Bytes Sequence Diagram



7.2.2 Fast Read (0BH)

See *Figure 9,* the Read Data Bytes at Higher Speed (Fast Read) instruction is for quickly reading data out. It is followed by a 3-byte address (A23-A0) and a dummy byte, each bit being latched-in during the rising edge of SCLK. Then the memory content, at that address, is shifted out on SO, each bit being shifted out, at a Max frequency fc, during the falling edge of SCLK. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out.

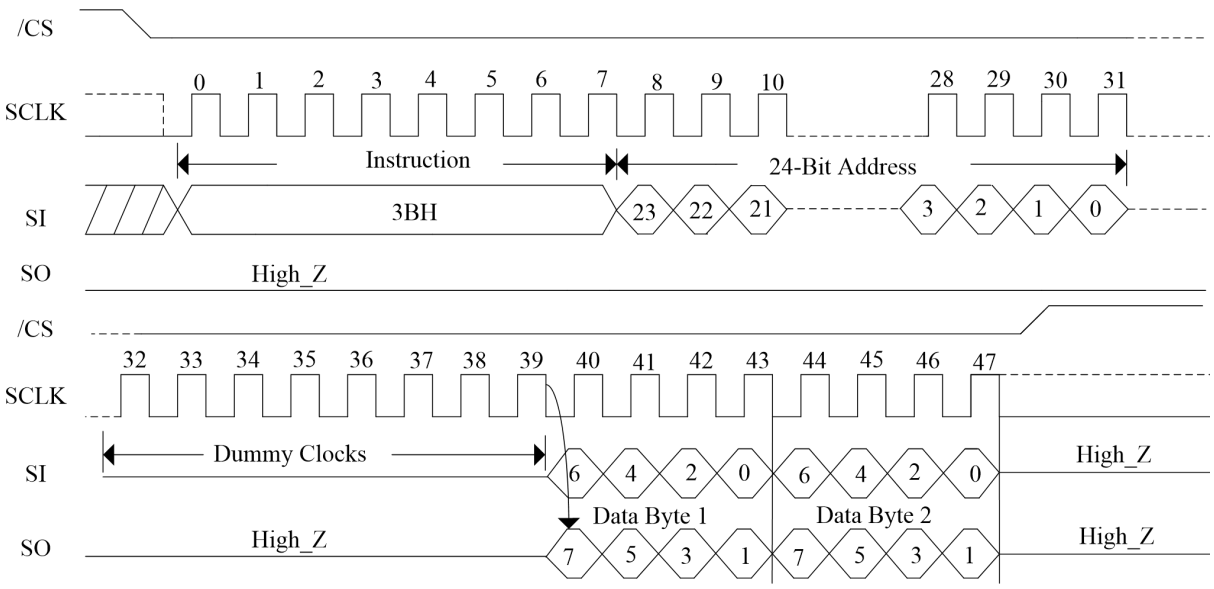
Figure 9. Fast Read Sequence Diagram



7.2.3 Dual Output Fast Read (3BH)

See *Figure 10,* the Dual Output Fast Read instruction is followed by 3-byte address (A23-A0) and a dummy byte, each bit being latched in during the rising edge of SCLK, then the memory contents are shifted out 2-bit per clock cycle from SI and SO. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out.

Figure 10. Dual Output Fast Read Sequence Diagram



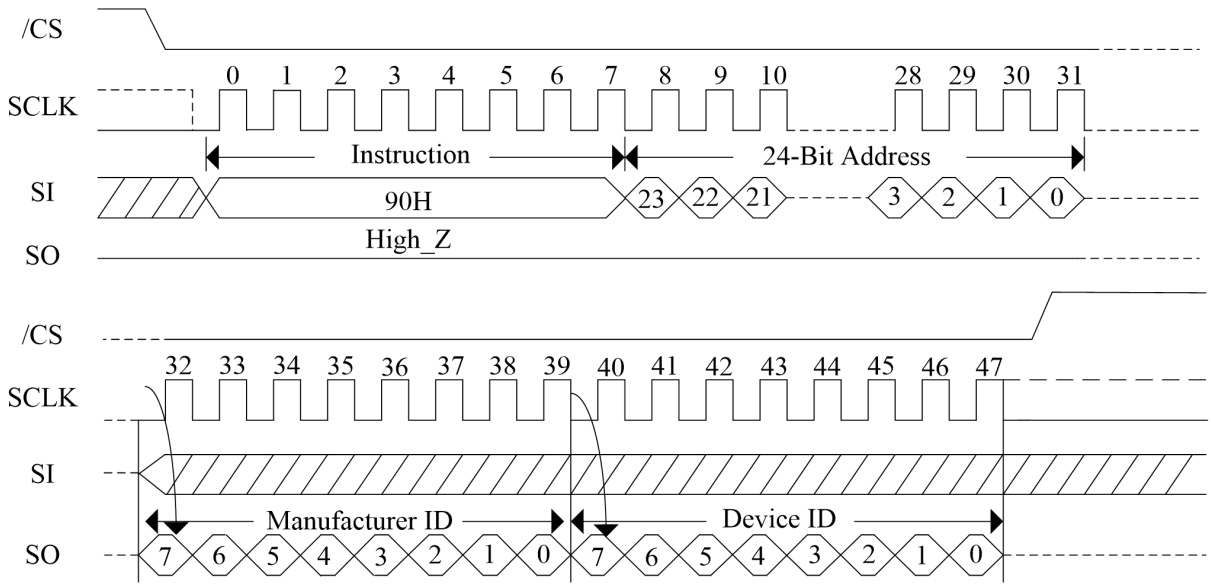
7.3 ID and Security Instructions

7.3.1 Read Manufacture ID/ Device ID (90H)

See *Figure 11,* the Read Manufacturer/Device ID instruction is an alternative to the Release from Power-Down/Device ID instruction that provides both the JEDEC assigned Manufacturer ID and the specific Device ID.

The instruction is initiated by driving the /CS pin low and shifting the instruction code “90H” followed by a 24-bit address (A23-A0) of 000000H. If the 24-bit address is initially set to 000001H, the Device ID will be read first.

Figure 11. Read Manufacture ID/ Device ID Sequence Diagram

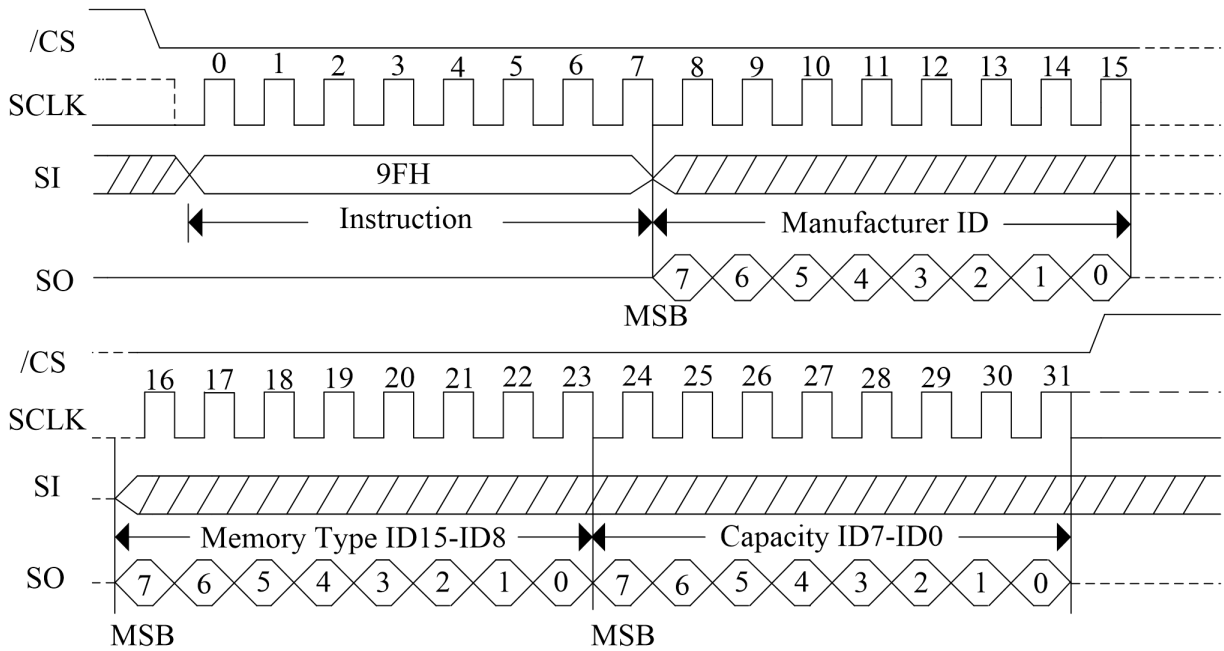


7.3.2 JEDEC ID (9FH)

The JEDEC ID instruction allows the 8-bit manufacturer identification to be read, followed by two bytes of device identification. The device identification indicates the memory type in the first byte, and the memory capacity of the device in the second byte. JEDEC ID instruction while an Erase or Program cycle is in progress, is not decoded, and has no effect on the cycle that is in progress. The JEDEC ID instruction should not be issued while the device is in Deep Power-Down Mode.

See *Figure 12,* he device is first selected by driving /CS to low. Then, the 8-bit instruction code for the instruction is shifted in. This is followed by the 24-bit device identification, stored in the memory, being shifted out on Serial Data Output, each bit being shifted out during the falling edge of Serial Clock. The JEDEC ID instruction is terminated by driving /CS to high at any time during data output. When /CS is driven high, the device is put in the Standby Mode. Once in the Standby Mode, the device waits to be selected, so that it can receive, decode and execute instructions.

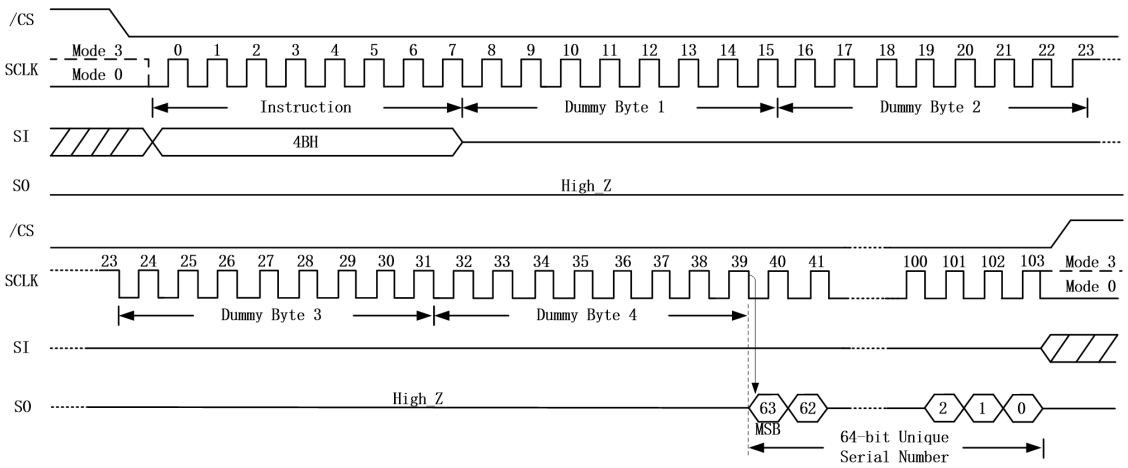
Figure 12. JEDEC ID Sequence Diagram



7.3.3 Read Unique ID Number (4Bh)

The Read Unique ID Number instruction accesses a factory-set read-only 64-bit number that is unique to each BY25D05AS device. The ID number can be used in conjunction with user software methods to help prevent copying or cloning of a system. The Read Unique ID instruction is initiated by driving the /CS pin low and shifting the instruction code “4Bh” followed by a four bytes of dummy clocks. After which, the 64-bit ID is shifted out on the falling edge of SCLK as shown in *Figure 13*.

Figure 13. Read Unique ID Sequence Diagram

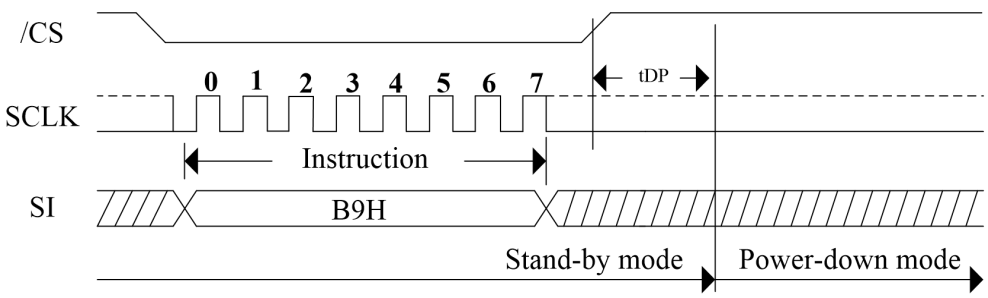


7.3.4 Deep Power-Down (B9H)

Although the standby current during normal operation is relatively low, standby current can be further reduced with the Deep Power-down instruction. The lower power consumption makes the Deep Power-down (DPD) instruction especially useful for battery powered applications (*see ICC1 and ICC2*). The instruction is initiated by driving the /CS pin low and shifting the instruction code "B9h" as shown in *Figure 14*.

The /CS pin must be driven high after the eighth bit has been latched. If this is not done the Deep Power down instruction will not be executed. After /CS is driven high, the power-down state will entered within the time duration of tDP. While in the power-down state only the Release from Deep Power-down / Device ID instruction, which restores the device to normal operation, will be recognized. All other Instructions are ignored. This includes the Read Status Register instruction, which is always available during normal operation. Ignoring all but one instruction also makes the Power Down state a useful condition for securing maximum write protection. The device always powers-up in the normal operation with the standby current of ICC1.

Figure 14. Deep Power-Down Sequence Diagram



7.3.5 Release from Deep Power-Down/Read Device ID (ABH)

The Release from Power-Down or Device ID instruction is a multi-purpose instruction. It can be used to release the device from the Power-Down state or obtain the devices electronic identification (ID) number.

See *Figure 15a,* to release the device from the Power-Down state, the instruction is issued by driving the /CS pin low, shifting the instruction code “ABH” and driving /CS high Release from Power-Down will take the time duration of tRES1 (See *AC Characteristics*) before the device will resume normal operation and other instruction are accepted. The /CS pin must remain high during the tRES1 time duration.

When used only to obtain the Device ID while not in the Power-Down state, the instruction is initiated by driving the /CS pin low and shifting the instruction code “ABH” followed by 3-dummy byte. The Device ID bits are then shifted out on the falling edge of SCLK with most significant bit (MSB) first as shown in *Figure 15b*. The Device ID value for the BY25D05AS is listed in Manufacturer and Device Identification table. The Device ID can be read continuously. The instruction is completed by driving /CS high.

When used to release the device from the Power-Down state and obtain the Device ID, the instruction is the same as previously described, and shown in *Figure 15b*, except that after /CS is driven high it must remain high for a time duration of tRES2 (See *AC Characteristics*). After this time duration the device will resume normal operation and other instruction will be accepted. If the Release from Power-Down/Device ID instruction is issued while an Erase, Program or Write cycle is in process (when WIP equal 1) the instruction is ignored and will not have any effects on the current cycle.

Figure 15a. Release Power-Down Sequence Diagram

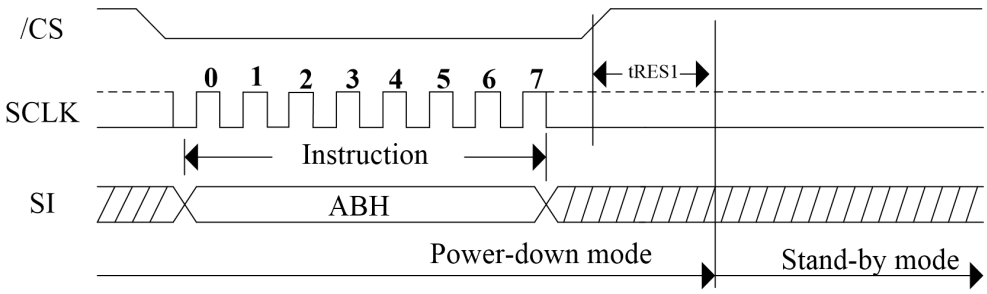
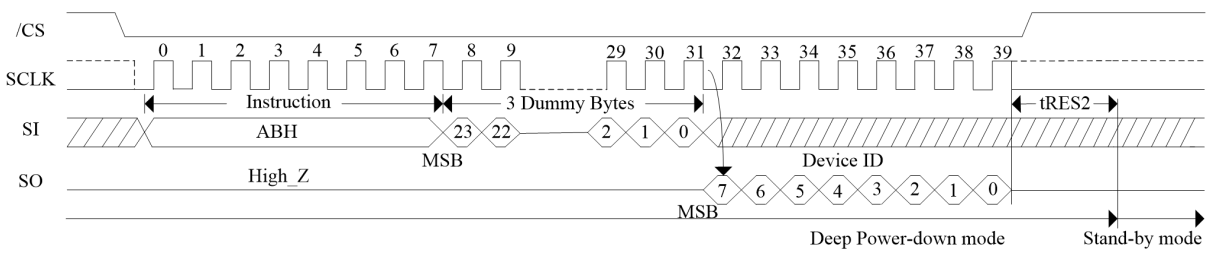


Figure 15b. Release Power-Down/Read Device ID Sequence Diagram



7.4 Program and Erase Instructions

7.4.1 Page Program (02H)

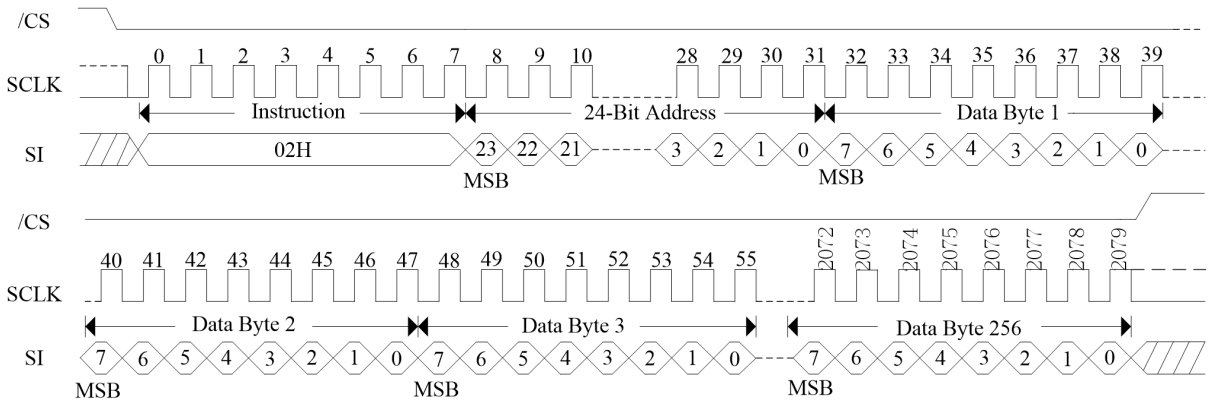
The Page Program instruction is for programming the memory. A Write Enable instruction must previously have been executed to set the Write Enable Latch bit before sending the Page Program instruction.

See *Figure 16,* the Page Program instruction is entered by driving /CS Low, followed by the instruction code, 3-byte address and at least one data byte on SI. If the 8 least significant address bits (A7-A0) are not all zero, all transmitted data that goes beyond the end of the current page are programmed from the start address of the same page (from the address whose 8 least significant bits (A7-A0) are all zero). /CS must be driven low for the entire duration of the sequence. The Page Program instruction sequence: /CS goes low sending Page Program instruction 3-byte address on SI at least 1 byte data on SI /CS goes high. If more than 256 bytes are sent to the device, previously latched data are discarded and the last 256 data bytes are guaranteed to be programmed correctly within the same page. If less than 256 data bytes are sent to device, they are correctly programmed at the requested addresses without having any effects on the other bytes of the same page. /CS must be driven high after the eighth bit of the last data byte has been latched in; otherwise the Page Program instruction is not executed.

As soon as /CS is driven high, the self-timed Page Program cycle (whose duration is tPP) is initiated. While the Page Program cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Page Program cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch bit is reset.

A Page Program instruction applied to a page which is protected by the Block Protect (BP2, BP1, BP0) bits is not executed.

Figure 16. Page Program Sequence Diagram

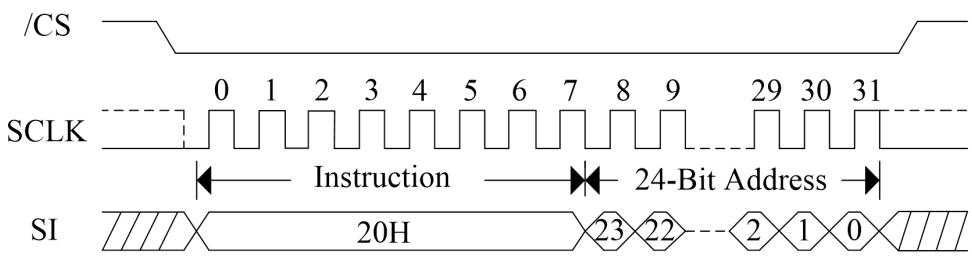


7.4.2 Sector Erase (20H)

The Sector Erase instruction is for erasing the all data of the chosen sector. A Write Enable instruction must previously have been executed to set the Write Enable Latch bit. The Sector Erase instruction is entered by driving /CS low, followed by the instruction code, and 3-address byte on SI. Any address inside the sector is a valid address for the Sector Erase instruction. /CS must be driven low for the entire duration of the sequence.

See *Figure 17,* The Sector Erase instruction sequence: /CS goes low sending 4KB Sector Erase instruction 3-byte address on SI /CS goes high. /CS must be driven high after the eighth bit of the last address byte has been latched in; otherwise the Sector Erase instruction is not executed. As soon as /CS is driven high, the self-timed Sector Erase cycle (whose duration is tSE) is initiated. While the Sector Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Sector Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch bit is reset. A Sector Erase instruction applied to a sector which is protected by the Block Protect (BP2, BP1, BP0) bits is not executed.

Figure 17. Sector Erase Sequence Diagram

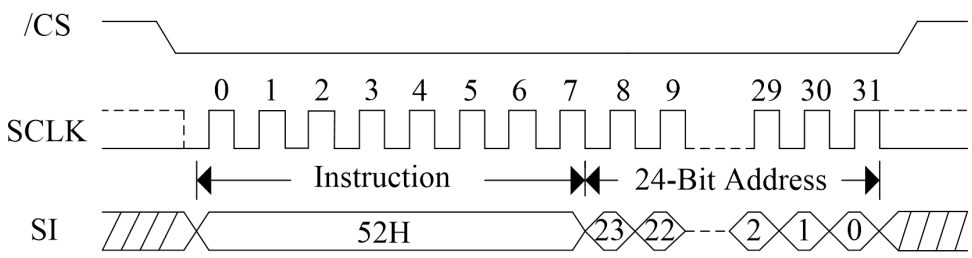


7.4.3 32KB Block Erase (52H)

The 32KB Block Erase instruction is for erasing the all data of the chosen block. A Write Enable instruction must previously have been executed to set the Write Enable Latch bit. The 32KB Block Erase instruction is entered by driving /CS low, followed by the instruction code, and 3-byte address on SI. Any address inside the block is a valid address for the 32KB Block Erase instruction. /CS must be driven low for the entire duration of the sequence.

See *Figure 18*, the 32KB Block Erase instruction sequence: /CS goes low sending 32KB Block Erase instruction 3-byte address on SI /CS goes high. /CS must be driven high after the eighth bit of the last address byte has been latched in; otherwise the 32KB Block Erase instruction is not executed. As soon as /CS is driven high, the self-timed Block Erase cycle (whose duration is tBE) is initiated. While the Block Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Block Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch bit is reset. A 32KB Block Erase instruction applied to a block which is protected by the Block Protect (BP2, BP1, BP0) bits is not executed.

Figure 18. 32KB Block Erase Sequence Diagram

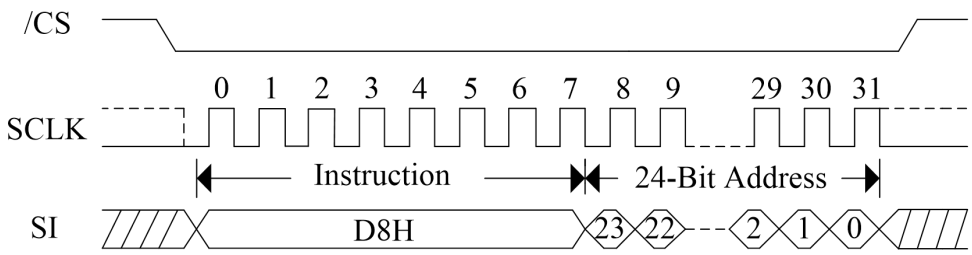


7.4.4 64KB Block Erase (D8H)

The 64KB Block Erase instruction is for erasing the all data of the chosen block. A Write Enable instruction must previously have been executed to set the Write Enable Latch bit. The 64KB Block Erase instruction is entered by driving /CS low, followed by the instruction code, and 3-byte address on SI. Any address inside the block is a valid address for the 64KB Block Erase instruction. /CS must be driven low for the entire duration of the sequence.

See *Figure 19*, the 64KB Block Erase instruction sequence: /CS goes low sending 64KB Block Erase instruction 3-byte address on SI /CS goes high. /CS must be driven high after the eighth bit of the last address byte has been latched in; otherwise the 64KB Block Erase instruction is not executed. As soon as /CS is driven high, the self-timed Block Erase cycle (whose duration is tBE) is initiated. While the Block Erase cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Block Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch bit is reset. A 64KB Block Erase instruction applied to a block which is protected by the Block Protect (BP2, BP1, BP0) bits is not executed.

Figure 19. 64KB Block Erase Sequence Diagram



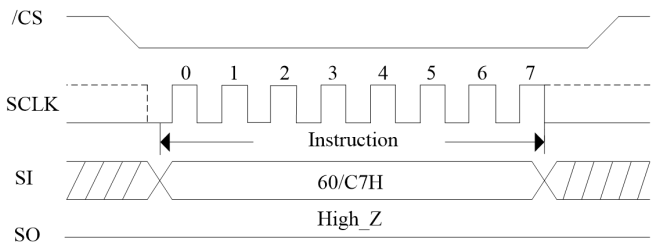
7.4.5 Chip Erase (60/C7H)

The Chip Erase instruction sets all memory within the device to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Chip Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the /CS pin low and shifting the instruction code “C7h” or “60h”. The Chip Erase instruction sequence is shown in *Figure 20.*

The /CS pin must be driven high after the eighth bit has been latched. If this is not done the Chip Erase instruction will not be executed. After /CS is driven high, the self-timed Chip Erase instruction will commence for a time duration of tCE. While the Chip Erase cycle is in progress, the Read Status Register instruction may still be accessed to check the status of the WIP bit.

The WIP bit is a 1 during the Chip Erase cycle and becomes a 0 when finished and the device is ready to accept other Instructions again. After the Chip Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Chip Erase instruction will not be executed if any page is protected by the Block Protect (BP2, BP1, and BP0) bits.

Figure 20. Chip Erase Sequence Diagram



8. Electrical Characteristics

8.1 Absolute Maximum Ratings

PARAMETERS	*SYMBOL*	CONDITIONS	RANGE	UNIT
Supply Voltage	VCC		–0.5 to 4	V
Voltage Applied to Any Pin	VIO	Relative to Ground	–0.5 to 4	V
Transient Voltage on any Pin	VIOT	<20nS Transient Relative to Ground	–2.0V to VCC+2.0V	V
Storage Temperature	TSTG		–65 to +150	°C
Electrostatic Discharge Voltage	VESD	Human Body Model(1)	–2000 to +2000	V

Notes:

1.JEDEC Std JESD22-A114A (C1=100pF, R1=1500 ohms, R2=500 ohms)

8.2 Operating Ranges

PARAMETER	*SYMBOL*	*CONDITIONS*	*SPEC*		*UNIT*
			MIN	*MAX*	
Supply Voltage	VCC		2.7	3.6	V
Temperature Operating	TA	Commercial	0	+70	°C
		Industrial	–40	+85	

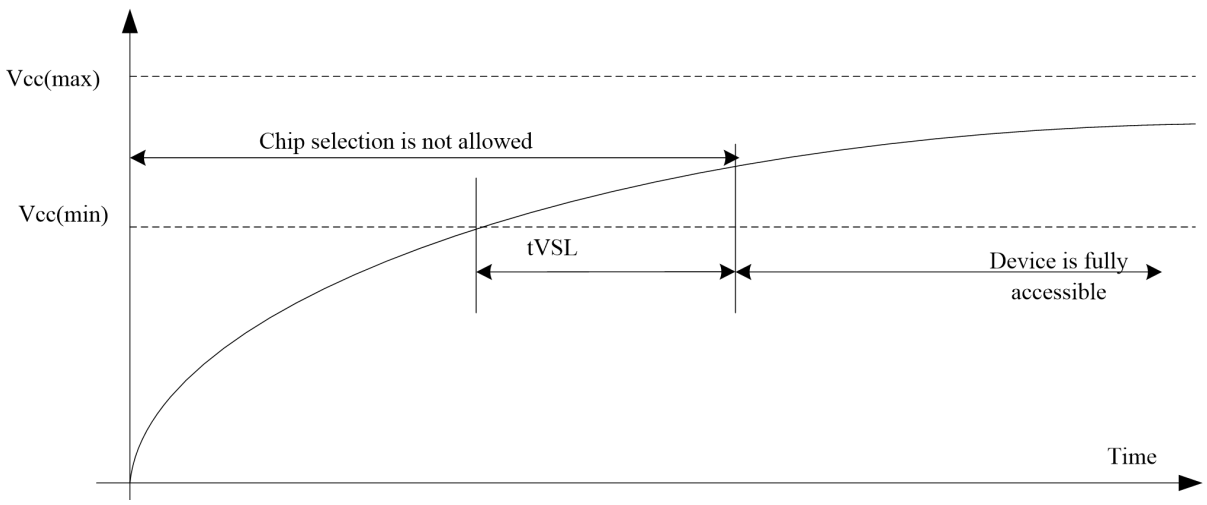
8.3 Latch Up Characteristics

Parameter	Min	Max
Input Voltage Respect To VSS On I/O Pins	-1.0V	VCC+1.0V
VCC Current	-100mA	100mA

8.4 Power-up Timing

Symbol	Parameter	Min	Max	Unit
tVSL	VCC(min) To /CS Low	300		us

Figure 21. Power-up Timing and Voltage Levels



8.5 DC Electrical Characteristics

(T= -40℃~85℃, VCC=2.7~3.6V)

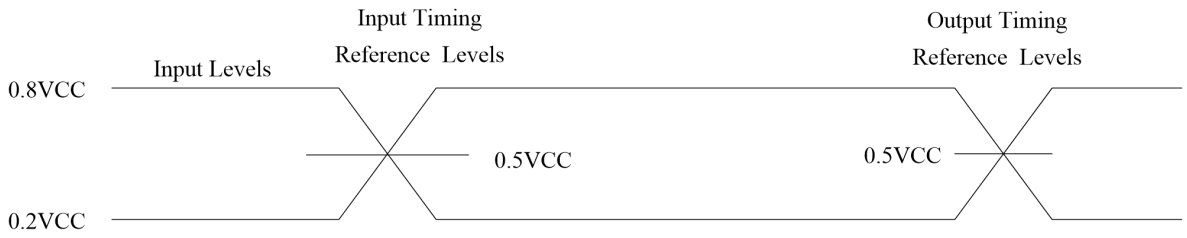
Symbol	Parameter	Test Condition	Min.	Typ	Max.	Unit.
ILI	Input Leakage Current				±2	μA
ILO	Output Leakage Current				±2	μA
ICC1	Standby Current	/CS=VCC, VIN=VCC or VSS		13	25	μA
ICC2	Deep Power-Down Current	/CS=VCC, VIN=VCC or VSS		2	5	μA
ICC3	Operation Current:(Read)	SCLK=0.1VCC/0.9VCC(1) at 108MHz, Q=Open(*1,*2,*4 I/O)		13	18	mA
ICC4	Operating Current(PP)	/CS=VCC			15	mA
ICC5	Operating Current(WRSR)	/CS=VCC			5	mA
ICC6	Operating Current(Sector Erase)	/CS=VCC			20	mA
ICC7	Operating Current(Block Erase)	/CS=VCC			20	mA
ICC8	Operating Current (Chip Erase)	/CS=VCC			20	mA
VIL	Input Low Voltage		-0.5		0.2VCC	V
VIH	Input High Voltage		0.8VCC		VCC+0.4	V
VOL	Output Low Voltage	IOL =100μA			0.4	V
VOH	Output High Voltage	IOH =-100μA	VCC-0.2			V

Note:
(1) ICC3 is measured with ATE loading

8.6 AC Measurement Conditions

Symbol	Parameter	Min	Tpy	Max	Unit	Conditions
CL	Load Capacitance			30	pF	
TR, TF	Input Rise And Fall time			5	ns	
VIN	Input Pause Voltage	0.2VCC to 0.8VCC			V	
IN	Input Timing Reference Voltage	0.5VCC			V	
OUT	Output Timing Reference Voltage	0.5VCC			V	

Figure 22. AC Measurement I/O Waveform



8.7 AC Electrical Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit.
fc	Clock frequency for all instructions, except Read Data(03H)	DC.		108	MHz
fR	Clock freq. Read Data instruction(03H)	DC.		55	MHz
tCLH	Serial Clock High Time	4			ns
tCLL	Serial Clock Low Time	4			ns
tCLCH	Serial Clock Rise Time (Slew Rate)	0.1(1)			V/ns
tCHCL	Serial Clock Fall Time (Slew Rate)	0.1(1)			V/ns
tSLCH	/CS Active Setup Time	5			ns
tCHSH	/CS Active Hold Time	5			ns
tSHCH	/CS Not Active Setup Time	5			ns
tCHSL	/CS Not Active Hold Time	5			ns

Symbol	Parameter	Min.	Typ.	Max.	Unit.
tSHSL	/CS High Time（read/write）	20			ns
tSHQZ	Output Disable Time			6	ns
tCLQX	Output Hold Time	0			ns
tDVCH	Data In Setup Time	2			ns
tCHDX	Data In Hold Time	2			ns
tCLQV	Clock Low To Output Valid			7	ns
tWHSL	Write Protect Setup Time Before /CS Low	20			ns
tSHWL	Write Protect Hold Time After /CS High	100			ns
tDP	/CS High To Deep Power-Down Mode			0.1	μs
tRES1	/CS High To Standby Mode Without Electronic Signature Read			3	μs
tRES2	/CS High To Standby Mode With Electronic Signature Read			1.5	μs
tW	Write Status Register Cycle Time		10	15	ms
tPP	Page Programming Time		0.7	2.4	ms
tSE	Sector Erase Time		100	300	ms
tBE	Block Erase Time(32K Bytes/64K Bytes)		0.3/0.5	0.6/1.0	s
tCE	Chip Erase Time		0.5	1.0	s

Note:

1. Tested with clock frequency lower than 50 MHz.

Figure 23. Serial Input Timing

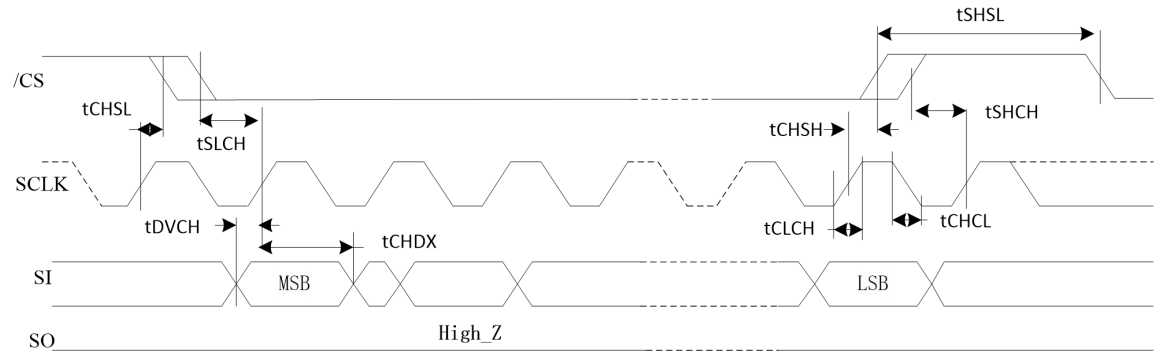
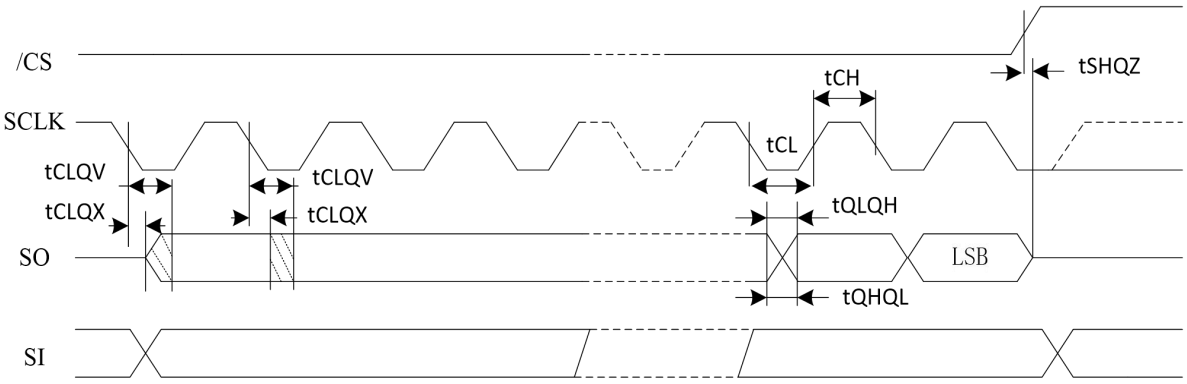
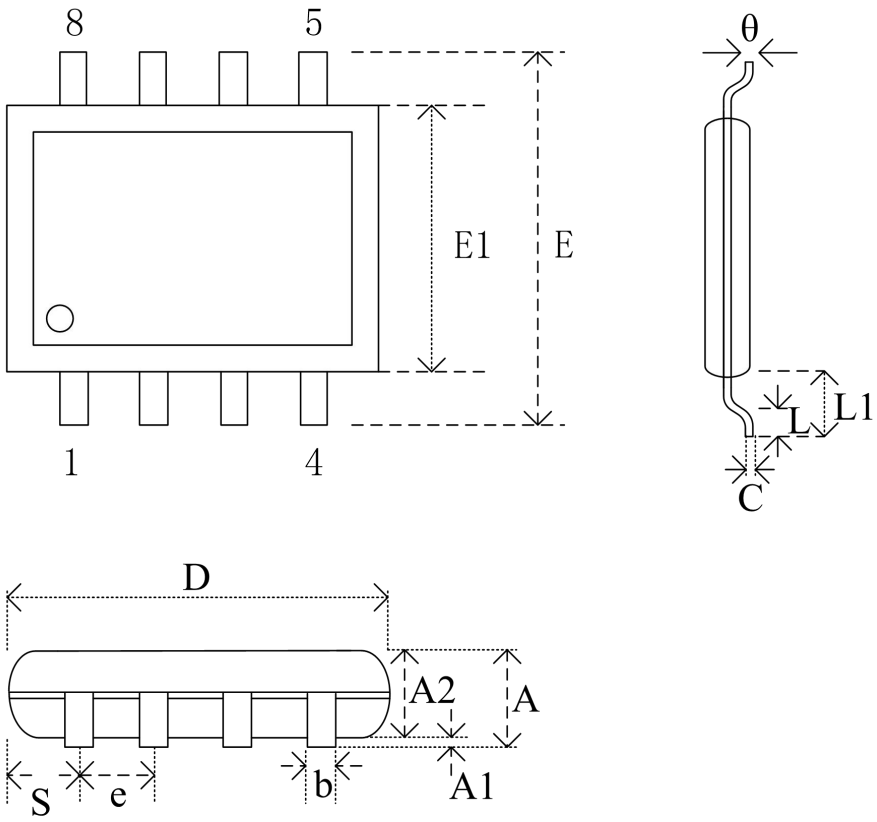


Figure 24. Output Timing



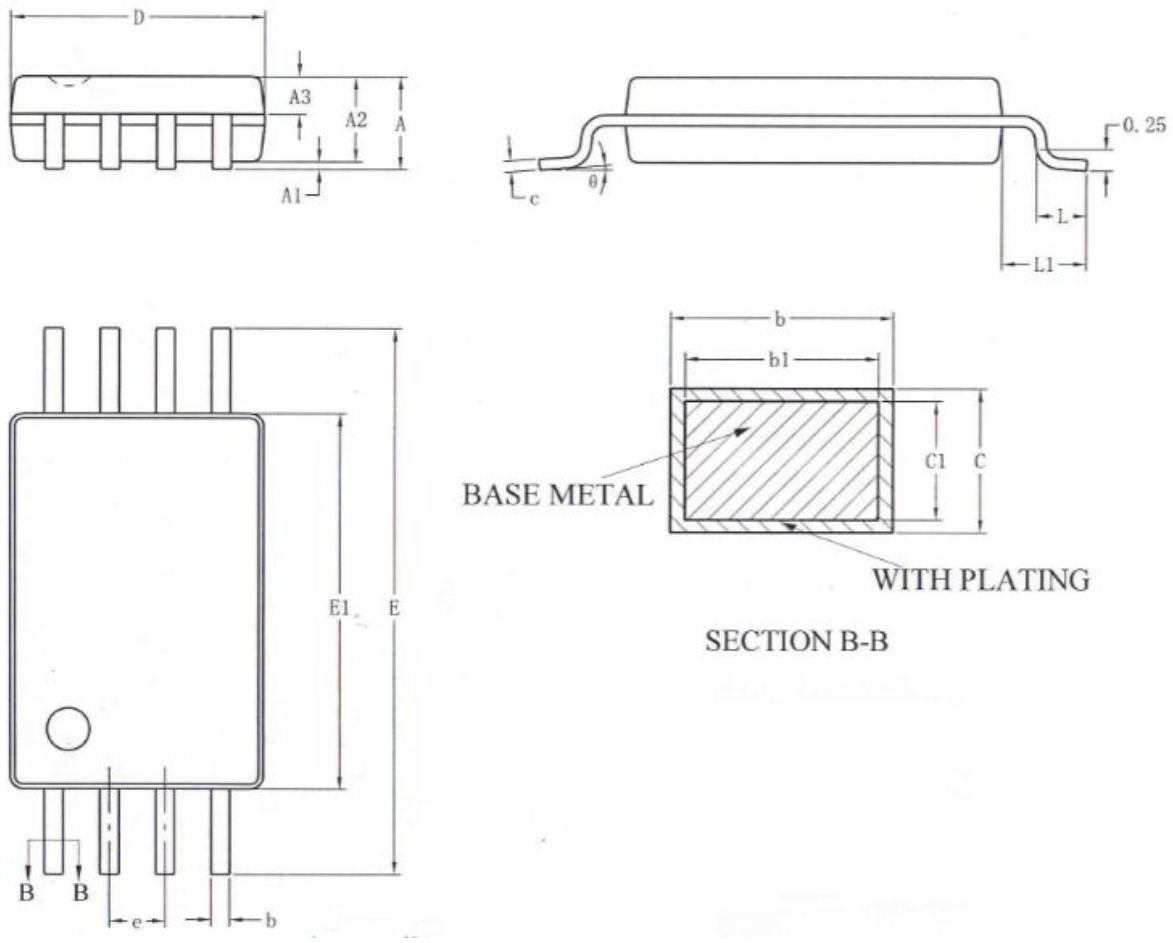
9. Package Information

9.1 Package 8-Pin SOP 150-mil



Symbol / Unit		A	A1	A2	b	C	D	E	E1	e	L	L1	S	θ
mm	Min	-	0.10	1.30	0.39	0.20	4.80	5.80	3.80	1.27	0.50	1.05	0.41	0
	Nom	-	-	1.40	-	-	4.90	6.00	3.90		-		0.54	5
	Max	1.75	0.225	1.50	0.47	0.24	5.00	6.20	4.00		0.80		0.67	8

9.2 Package 8-Pin TSSOP 173-mil

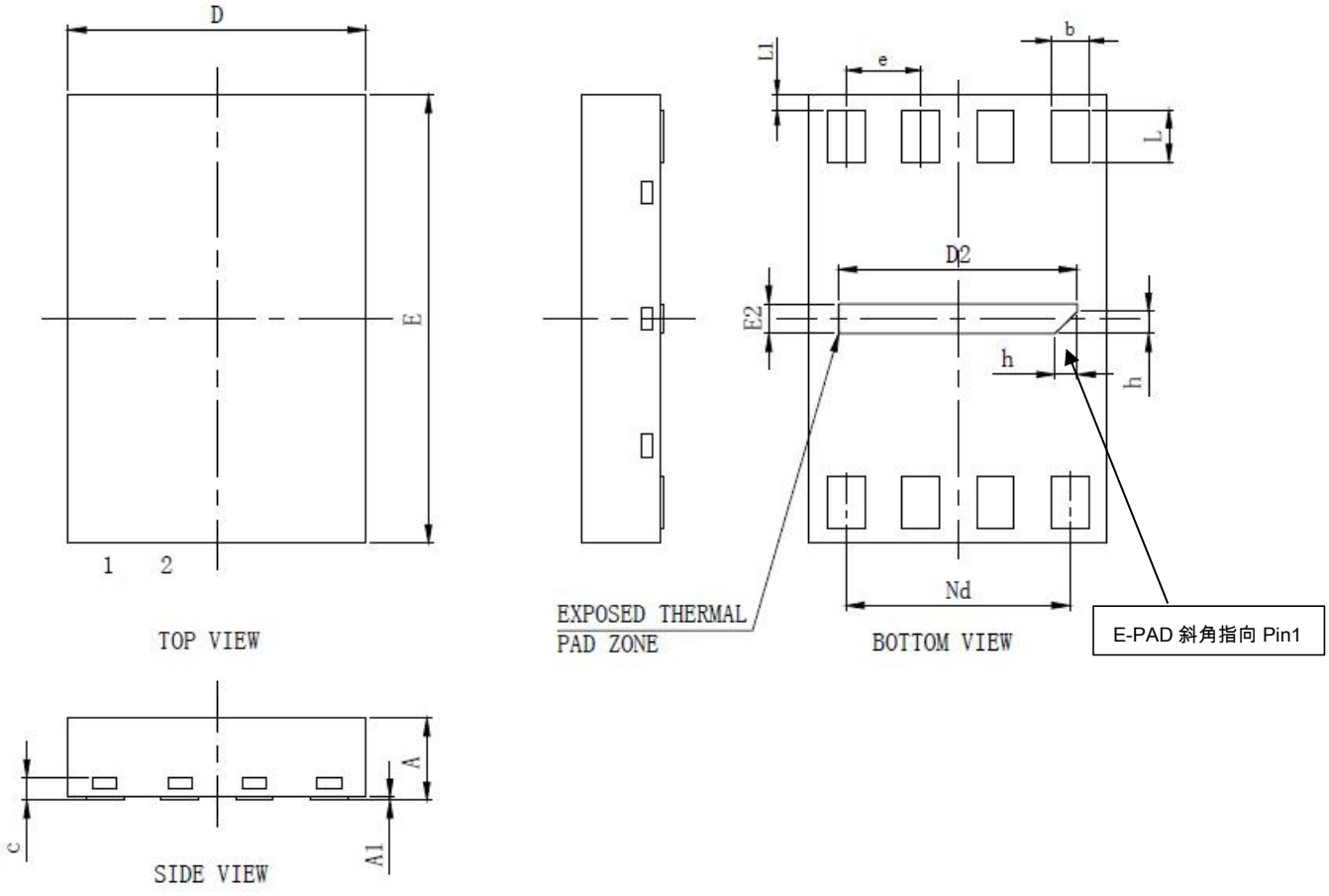


Dimensions

Symbol / Unit		A	A1	A2	A3	b	b1	c	c1	D	E	E1	e	L	L1	θ
mm	Min	-	0.05	0.90	0.39	0.20	0.19	0.13	0.12	2.90	6.20	4.30	0.65	0.45	1.00	0
	Nom	-	-	1.00	0.44	-	0.22	-	0.13	3.00	6.40	4.40		-		-
	Max	1.20	0.15	1.05	0.49	0.28	0.25	0.17	0.14	3.10	6.60	4.50		0.75		8

Note:
1、The exposed metal pad area on the bottom of the package is floating.

9.3 Package USON8 (2*3mm)

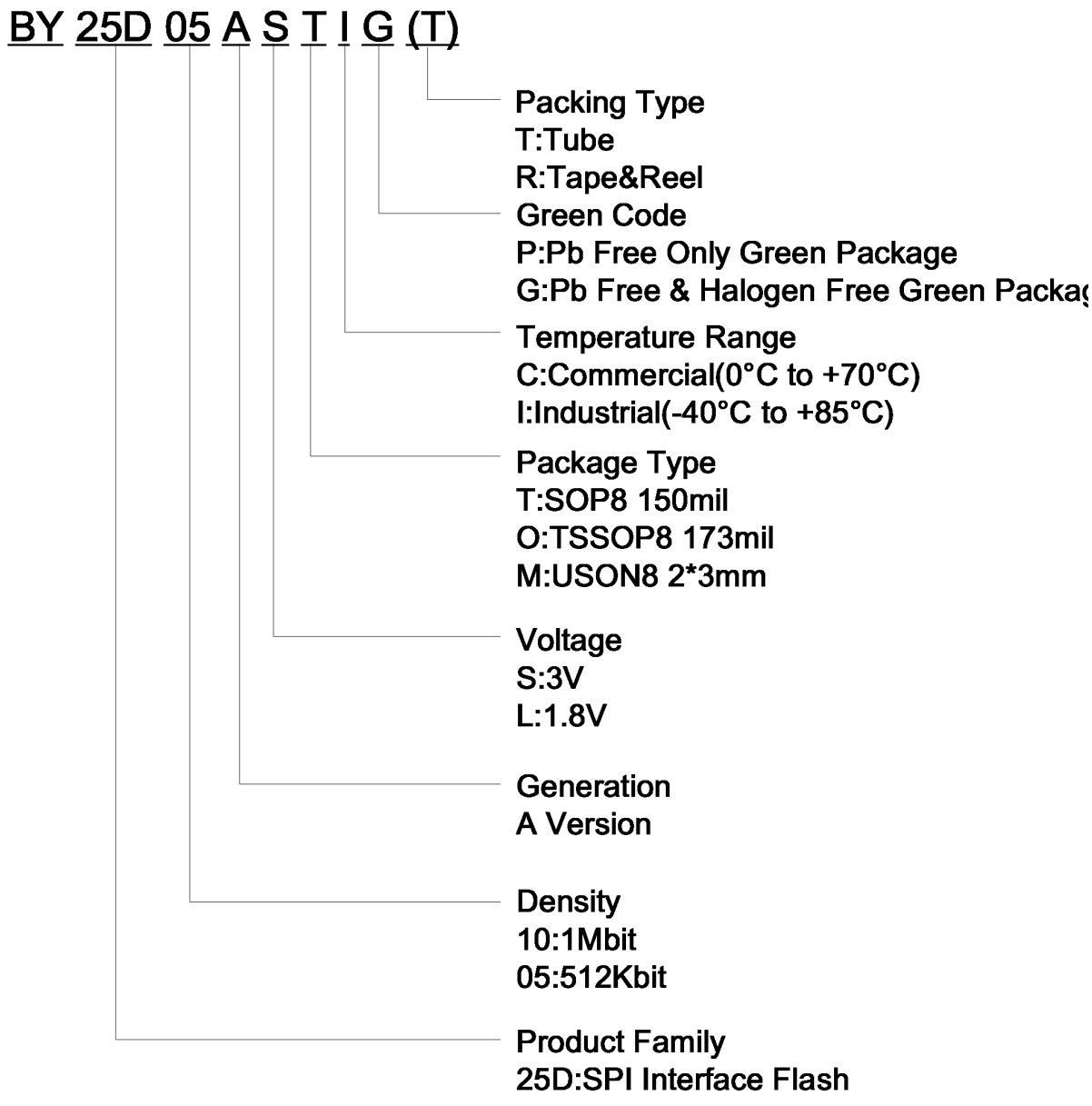


Dimensions

Symbol / Unit		A	A1	b	c	D	D2	e	Nd	E	E2	L	L1	h
mm	Min	0.45	0	0.20	0.10	1.90	1.50	0.50BSC	1.50BSC	2.90	0.10	0.30	0.05	0.05
	Nom	0.50	0.02	0.25	0.15	2.00	1.60			3.00	0.20	0.35	0.10	0.15
	Max	0.55	0.05	0.30	0.20	2.10	1.70			3.10	0.30	0.40	0.15	0.25

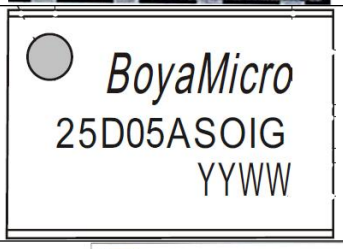
Note:
1、The exposed metal pad area on the bottom of the package is floating.

10. Order Information



10.1 Valid part Numbers and Top Side Marking

The following table provides the valid part numbers for BY25D05AS SPI Flash Memory. Pls contact BY Technology for specific availability by density and package type.

Package Type	Density	Product Number	Top Side Marking
T SOP8 150mil	512K-bit	BY25D05ASTIG	
O TSSOP8 173mil	512K-bit	BY25D05ASOIG	
M USON8 2*3mm	512K-bit	BY25D05ASMIG	

10.2 Minimum Packing Quantity (MPQ)

Package Type	Packing Type	Qty for 1 Tube or Reel	Vacuum bag/ Inner Box	MPQ
SOP8 150mil	Tube	100ea/Tube	100Tubes/Bag 1Bag/InnerBox	10,000
	Tape&Reel	4000ea/Reel	1Reel/Bag 1Bags/InnerBox	4,000
TSSOP8 173mil	Tube	100ea/Tube	120Tubes/Bag 1Bag/InnerBox	12,000
	Tape&Reel	5000ea/Reel	1Reel/Bag 1Bag/InnerBox	5,000
USON8 2*3mm	Tape&Reel	3000ea/Reel	1Reel/Bag 10Bags/InnerBox	30,000

11. Document Change History

REVISION	CHANGE DESCRIPTION	CLAUSE	ORIGINATOR DATE
1.0	Initiate	/	Zuohuan Yu 2014-3-5
1.1	Update max. fast/dual read clock frequency from 80MHz to 108MHz	/	Zuohuan Yu 2015-10-14
1.2	Update Protect Table	/	Zuohuan Yu 2017.1.18
1.3	Update Power-up Timing	/	Zuohuan Yu 2017.2.7
1.4	Update TTSOP-8 Packing Diagram	/	Zuohuan Yu 2017.2.22
1.5	Remove FPP(F2H) Instruction& Add Read Unique ID Number(4BH) Instruction	/	Zuohuan Yu 2017.4.13
1.6	Update AC Measurement Conditions,Serial Input&output Timing	/	Zuohuan Yu 2017.5.2
1.7	Add valid part numbers&Top Side Marking introduction	/	Zuohuan Yu 2017.8.5
1.8	update USON8 2*3mm package spec	/	Zuohuan Yu 2019.2.27
1.9	Modify data Retention and Endurance	/	Zuohuan Yu 2020.7.21
2.0	Update the logo and abbreviation	/	Zuohuan Yu 2023-4-6
2.1	Add the note of the DFN package	/	Zuohuan Yu 2023-07-21